PHILIPS

Data handbook

Electronic components and materials

Components and materials

Part 7 September 1971

# Circuit blocks

# COMPONENTS AND MATERIALS

**Part 7** **September 1971**



**For comprehensive contents list see back**

# DATA HANDBOOK SYSTEM

To provide you with a comprehensive source of information on electronic components, subassemblies and materials, our Data Handbook System is made up of three series of handbooks, each comprising several parts.
The three series, identified by the colours noted, are:

**ELECTRON TUBES** (9 parts) BLUE

**SEMICONDUCTORS AND INTEGRATED CIRCUITS** (5 parts) RED

**COMPONENTS AND MATERIALS** (7 parts) GREEN

The several parts contain all pertinent data available at the time of publication, and each is revised and reissued annually; the contents of each series are summarized on the following pages.
We have made every effort to ensure that each series is as accurate, comprehensive and up-to-date as possible, and we hope you will find it to be a valuable source of reference. Where ratings or specifications quoted differ from those published in the preceding edition they will be pointed out by arrows. You will understand that we can not guarantee that all products listed in any one edition of the handbook will remain available, or that their specifications will not be changed, before the next edition is published. If you need confirmation that the pusblished data about any of our products are the latest available, may we ask that you contact our representative. He is at your service and will be glad to answer your inquiries.

May 1971

# ELECTRON TUBES (BLUE SERIES)

This series consists of the following parts, issued on the dates indicated.

**Part 1** — **January 1971**

Transmitting tubes (Tetrodes, Pentodes)
Associated accessories

**Part 2** — **March 1971**

Tubes for microwave equipment

**Part 3** — **March 1970**

Special Quality tubes
Miscellaneous devices

**Part 4** — **April 1971**

Receiving tubes

**Part 5** — **May 1971**

Cathode-ray tubes
Photo tubes
Camera tubes
Photoconductive devices
Associated accessories

**Part 6** — **June 1971**

Photomultipliers tubes
Channel electron multipliers
Scintillators
Photoscintillators
Radiation counter tubes
Semiconductor radiation detectors
Neutron generator tubes
Photo diodes
Associated accessories

**Part 7** — **July 1971**

Voltage stabilizing and reference tubes
Counter, selector, and indicator tubes
Trigger tubes
Switching diodes
Thyratrons
Ignitrons
Industrial rectifying tubes
High-voltage rectifying tubes

**Part 8** — **August 1971**

T.V. Picture tubes

**Part 9** — **January 1971**

Transmitting tubes (Triodes)
Tubes for R.F. heating (Triodes)
Associated accessories

August 1971

# SEMICONDUCTORS AND INTEGRATED CIRCUITS (RED SERIES)

This series consists of the following parts, issued on the dates indicated.

**Part 1 Diodes and Thyristors** — **September 1971**

General
Signal diodes
Variable capacitance diodes
Voltage regulator diodes
Rectifier diodes
Thyristors, diacs, triacs
Rectifier stacks
Accessories
Heatsinks

**Part 2 Low frequency; Deflection** — **October 1970**

General
Low frequency transistors (low power)
Low frequency power transistors
Deflection transistors
Accessories

**Part 3 High frequency; Switching** — **November 1970**

General
High frequency transistors
Switching transistors
Accessories

**Part 4 Special types** — **December 1970**

General
Transmitting transistors
Microwave devices
Field effect transistors
Dual transistors
Microminiature devices for thick- and thin-film circuits
Beam lead devices for thick- and thin-film circuits
Photo devices
Accessories

**Part 5 Integrated Circuits** — **March 1971**

General
Digital integrated circuits
  DTL (FC family)
  TTL (FJ family)
  MOS (FD family)
Linear integrated circuits

# COMPONENTS AND MATERIALS (GREEN SERIES)

This series consists of the following parts, issued on the dates indicated.

## Part 1 Circuit Blocks, Input/Output Devices, Electro-mechanical Components *), Peripheral Devices

**October 1971**

Circuit blocks 40-Series
Counter modules 50-Series
Norbits 60-Series, 61-Series
Circuit blocks 90-Series
Input/output devices
Electro-mechanical components *)
Peripheral devices

## Part 2 Resistors, Capacitors

**December 1970**

Fixed resistors
Variable resistors
Non-linear resistors
Ceramic capacitors
Polyester, polycarbonate, polystyrene, paper capacitors
Electrolytic capacitors
Variable capacitors

## Part 3 Radio, Audio, Television

**February 1971**

FM tuners
Coils * *)
Piezoelectric ceramic resonators and filters
Loudspeakers
Audio and mains transformers
Television tuners
Components for black and white television
Components for colour television
Deflection assemblies for camera tubes

## Part 4 Magnetic Materials, Piezoelectric Ceramics

**April 1971**

Ferrites for radio, audio and television
Small coils, assemblies and assembling parts
Ferroxcube potcores and square cores
Ferroxcube transformer cores
Piezoxide
Permanent magnet materials

## Part 5 Memory Products, Magnetic Heads, Quartz Crystals, Microwave Devices, Variable Transformers

**June 1971**

Ferrite memory cores
Matrix planes, matrix stacks
Complete memories
Magnetic heads
Quartz crystal units, crystal filters
Isolators, circulators
Variable mains transformers

## Part 6 Electric Motors and Accessories, Timing and Control Devices

**August 1971**

Stepper motors
Small synchronous motors
Asynchronous motors
Small d.c. motors
Tachogenerators and servomotors
Indicators for built-in test equipment

## Part 7 Circuit Blocks

**September 1971**

Circuit blocks 100kHz Series
Circuit blocks 1-Series
Circuit blocks 10-Series
Circuit blocks for ferrite core memory drive

*) From October 1971 published in Part 1 instead of Part 5.
* *) Also included (under "Small coils, etc.") in Part 4.

**Technology relating to the products described in this publication is shared by the following companies.**

**Argentina**
FAPESA I.y.C.
Melincué 2594
Tel. 50-9941/8155
BUENOS AIRES

**Australia**
Philips Industries Ltd.
Miniwatt Electronics Division
20, Herbert St.
Tel. 43-2171
ARTARMON, N.S.W.

**Austria**
WIVEG
Zieglergasse 6
Tel. 93 26 22
A1072 VIENNA

**Belgium**
M.B.L.E.
80, rue des Deux Gares
Tel. 23 00 00
1070 BRUSSELS

**Brazil**
IBRAPE S.A.
Av. Paulista 2073-S/Loja
Tel. 278-1111
SAO PAULO

**Canada**
Philips Electron Devices
116, Vanderhoof Ave.
Tel. 425-5161
TORONTO 17, Ontario

**Chile**
Philips Chilena S.A.
Av. Santa Maria 0760
Tel. 39-40 01
SANTIAGO

**Colombia**
SADAPE S.A.
Calle 19, No.5-51
Tel. 422-175
BOGOTA D.E. 1

**Denmark**
Miniwatt A/S
Emdrupvej 115A
Tel. (01) 69 16 22
DK-2400 KØBENHAVN NV

**Finland**
Oy Philips A.B.
Elcoma Division
Kaivokatu 8
Tel. 10 915
HELSINKI 10

**France**
R.T.C.
La Radiotechnique-Compelec
Avenue Ledru Rollin 130
Tel. 357-69-30
PARIS 11

**Germany**
VALVO G.m.b.H.
Valvo Haus
Burchardstrasse 19,
Tel. (0411) 3296-1
2 HAMBURG 1

**Greece**
Philips S.A. Hellénique
Elcoma Division
52, Av. Syngrou
Tel. 915.311
ATHENS

**Hong Kong**
Philips Hong Kong Ltd.
Components Dept.
St. George's Building 21st Fl.
Tel. K-42 82 05
HONG KONG

**India**
INBELEC Div. of
Philips India Ltd.
Band Box House
254-D, Dr. Annie Besant Road
Tel. 45 33 86, 45 64 20, 45 29 86
Worli, Bombay 18 (WB)

**Indonesia**
P.T. Philips-Ralin Electronics
Elcoma Division
Djalan Gadjah Mada 18
Tel. 44 163
DJAKARTA

**Ireland**
Philips Electrical (Ireland) Ltd.
Newstead, Clonskeagh
Tel. 69 33 55
DUBLIN 14

**Italy**
Philips S.p.A.
Sezione Elcoma
Piazza IV Novembre 3
Tel. 69 94
MILANO

**Japan**
NIHON PHILIPS
32nd Fl., World Trade Center Bldg.
5, 3-chome, Shiba Hamamatsu-cho
Minato-ku,
Tel. (435) 5204-5
TOKYO

**Mexico**
Electrónica S.A. de C.V.
Varsovia No.36
Tel. 5-33-11-80
MEXICO 6, D.F.

**Netherlands**
Philips Nederland N.V.
Afd. Elonco
Boschdijk, VB
Tel. (040) 43 33 33
EINDHOVEN

**New Zealand**
EDAC Ltd.
70-72 Kingsford Smith Street
Tel. 873 159
WELLINGTON

**Norway**
Electronica A/S
Middelthunsgate 27
Tel. 46 39 70
OSLO 3

**Peru**
CADESA
Jr. Ilo, No. 216
Appartado 10132
Tel. 27 7317
LIMA

**Portugal**
Philips Portuguesa S.A.R.L.
Rua Joaquim Antonio de Aguiar 66
Tel. 68 31 21/9
LISBOA

**South Africa**
EDAC (PTY) Ltd.
South Park Lane
New Doornfontein
Tel. 24/6701-2
JOHANNESBURG

**Spain**
COPRESA S.A.
Balmes 22
Tel. 232 66 80
BARCELONA 7

**Sweden**
ELCOMA A.B.
Lidingövägen 50
Tel. 08/67 97 80
10250 STOCKHOLM 27

**Switzerland**
Philips A.G.
Edenstrasse 20
Tel. 051/44 22 11
CH-8027 ZUERICH

**Taiwan**
Philips Taiwan Ltd.
San Min Building, 3rd Fl.
57-1, Chung Shan N. Road
Section 2
Tel. 553 101
TAIPEI

**Turkey**
Turk Philips Ticaret A.S.
EMET Department
Gümüssuyu Cad. 78-80
Tel. 45.32.50
Beyoglu, ISTANBUL

**United Kingdom**
Mullard Ltd.
Mullard House
Torrington Place
Tel. 01-580 6633
LONDON WC1E 7HD

**United States**

**Amperex Electronic Corp.**
Electron Tubes Div.
Tel. 516 WE 1-6200
HICKSVILLE N.Y.

Sem. and Microcircuits Div.
Tel. 401-762-9000
SLATERSVILLE R.I. 02876

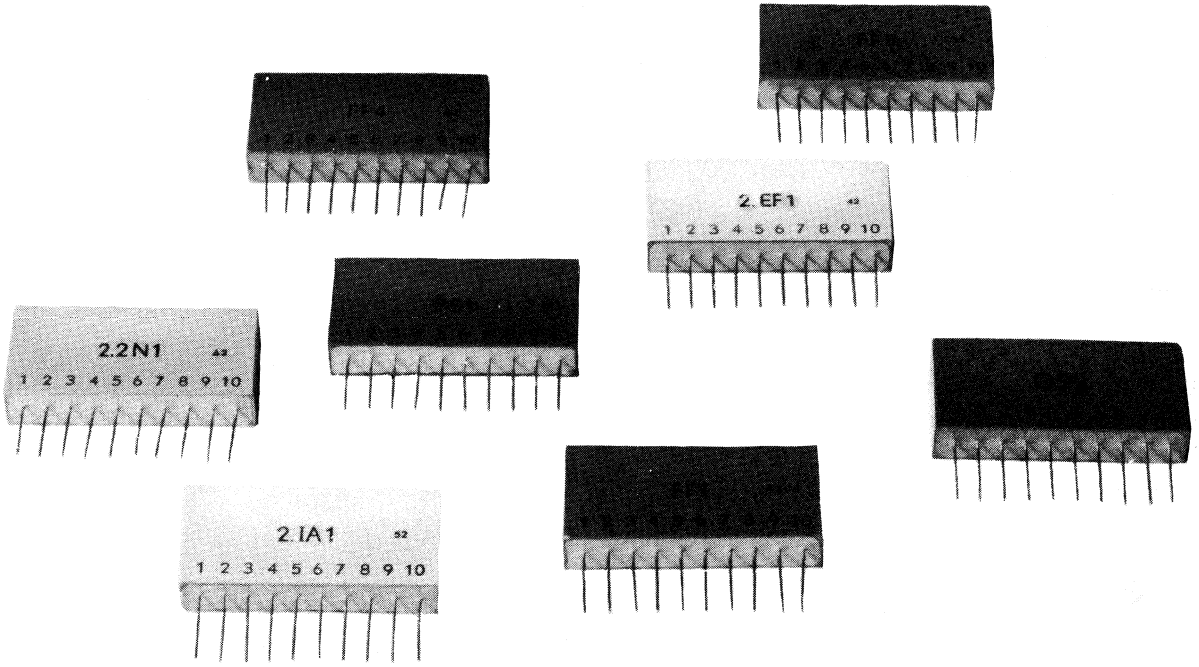
Electronic Components Div.
Tel. 516-234-7000
HAUPPAUGE N.Y.

**Ferroxcube Corp.**
(Memory Products)
P.O. Box 359
Tel. (914) 246-2811
SAUGERTIES, N.Y. 12477

**Uruguay**
Luzilectron S.A.
Rondeau 1567, piso 5
Tel. 9 43 21
MONTEVIDEO

**Venezuela**
C.A. Philips Venezolana
Elcoma Department
Colinas de Bello Monte
Tel. 72.01.51
CARACAS

# Circuit blocks
# 100 kHz Series




RZ 17383-1

# INTRODUCTION

A circuit block is a small encapsulated unit containing a basic electronic circuit, designed to accept and operate upon a specific type of input signal and to produce a specific type of electrical output. A number of different blocks can be combined to form larger parts of an electronic digital system.

In this series the following units and assembled panels are available:

| description | colour | abbreviation | catalog number | page |
|---|---|---|---|---|
| Flip-flop | red | FF1 | 2722 001 00001 | A57 |
| Flip-flop | red | FF2 | 2722 001 00011 | A61 |
| Flip-flop | red | FF3 | 2722 001 00021 | A65 |
| Flip-flop | red | FF4 | 2722 001 00031 | A69 |
| Dual 3-input negative gate | orange | 2.3N1 | 2722 001 01001 | A73 |
| Dual 2-input negative gate | orange | 2.2N1 | 2722 001 01011 | A75 |
| Dual 3-input positive gate | orange | 2.3P1 | 2722 001 02001 | A77 |
| Dual 2-input positive gate | orange | 2.2P1 | 2722 001 02011 | A79 |
| Dual pulse logic | orange | 2.PL1 | 2722 001 03001 | A81 |
| Dual pulse logic | orange | 2.PL2 | 2722 001 03011 | A85 |
| Emitter follower/inverter amplifier | yellow | EF1/IA1 | 2722 001 07001 | A89 |
| Dual emitter follower | yellow | 2.EF1 | 2722 001 05001 | A91 |
| Dual inverter amplifier | yellow | 2.IA1 | 2722 001 06001 | A95 |
| Dual emitter follower | yellow | 2.EF2 | 2722 001 05011 | A99 |
| Dual inverter amplifier | yellow | 2.IA2 | 2722 001 06011 | A103 |
| Dual gate inverter | yellow | 2.GI1 | 2722 001 08001 | B31 |
| Pulse shaper | green | PS1 | 2722 001 11001 | A107 |
| Pulse shaper | green | PS2 | 2722 001 11011 | A111 |
| Positive reset unit | blue | PR1 | 2722 001 22001 | A117 |
| One-shot multivibrator | green | OS1 | 2722 001 10001 | A121 |
| One-shot multivibrator | green | OS2 | 2722 001 10011 | A125 |
| Pulse driver | green | PD1 | 2722 001 13011 | A131 |
| Printed-wiring board for PD1 | | PDA1 | 4322 026 34710 | A181 |
| Power amplifier | - | PA1 | 2722 032 00011 | A137 |
| Printed-wiring board for PA1 | | PAA1 | 4322 026 33630 | A179 |
| Decade counter | - | DC1 | 2722 009 00001 | A141 |
| Dual decade counter | - | 2.DCA2 | 2722 009 00011 | A147 |
| Reversible counter | - | BCA1 | 2722 009 00021 | A153 |
| Decade counter and numerical indicator tube driver assembly | | DCA3 | 2722 009 00031 | A159 |
| Dual numerical indicator tube driver assembly | | 2.ID1 | 2722 009 05001 | A167 |

A number of static input and output devices can be used in conjunction with 100 kHz circuit blocks, see chapter "INPUT/OUTPUT DEVICES"

For power supplies, printed-wiring boards, etc. see section "ACCESSORIES FOR CIRCUIT BLOCKS 100 kHz SERIES"

## ADVANTAGES OF CIRCUIT BLOCKS

Some of the outstanding advantages of circuit blocks are:

- saving of time and effort in the development and manufacture of electronic equipment;
- saving of handling, mounting and testing costs in manufacture;
- high and constant quality level;
- simplification of stock-keeping and ordering;
- rationalisation through standardised units.

## FIELDS OF APPLICATION

Circuit blocks can in general be used in all digital data-handling equipment, such as for:

- signalling;
- computing;
- controlling;
- measuring and testing;
- data handling;
- laboratory uses.

For detailed design and application information section "Some Practical Circuits", should be consulted.

# CONSTRUCTION

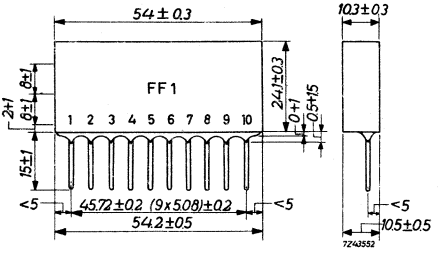



Fig. 1 Dimensional drawing of the circuit block

The dimensions of all 100 kHz circuit blocks are approximately 54 mm x 24 mm x 11 mm (see fig. 1). Out of one side of 54 mm x 11 mm emerge ten wire terminals of 0.7 mm diameter and 15 mm length. The distances between the wires are 5.08 mm (0.2 in) in accordance with the I.E.C. standard hole grid for printed-wiring boards.

The blocks are colour-coded, a different colour being used for each group of functions.

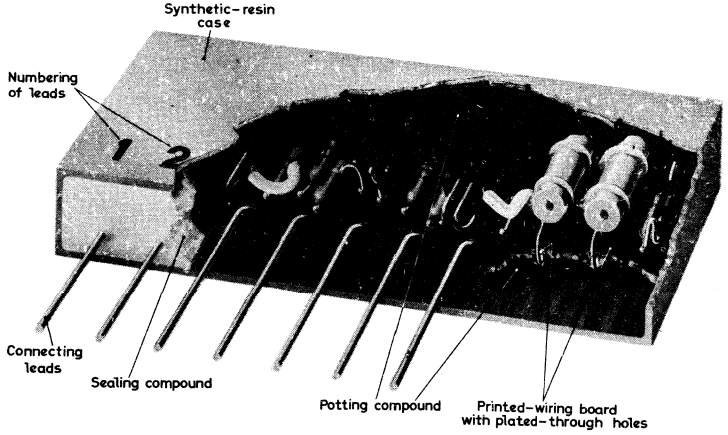



Fig. 2 Cut-away view of a circuit block

The construction of a 100 kHz circuit block can easily be seen in the cut-away view of Fig. 2.

The electronic components, of which the circuit is made up (transistors, diodes, resistors, capacitors) are mounted on a printed-wiring board. This board is provided with plated-through holes to ensure reliable joints due to the large contact area of soldered contacts. The connecting leads are also mounted on the printed-wiring board.

Protection against mechanical shock and vibration is provided by the resilient potting compound, whilst atmospheric influences are excluded by the sealing compound, by which the synthetic resin case is hermetically closed.

For the sake of reference the connecting leads are numbered 1 to 10.

# DESIGN CONSIDERATIONS AND RELIABILITY

The main problem in the design of electronic equipment is to attain an optimum level of reliability. The effective functional reliability of an electronic apparatus is - once a given circuit has been determined - exclusively dependent on the stability of the characteristics of the circuit components during their lives.

Though the drift of the characteristics of the present-day components has already been brought down to a very low value, the circuit has to be designed so as to be capable of accepting the still remaining drift. This factor and the nominal spread in the component values determines the total spread to be reckoned with during life.

A very safe design can be achieved by adopting the so-called "worst-case design" principle, in which these total spreads in their most unfavourable combination are taken as a design basis. As far as systematic failures are concerned, these considerations lead to a very safe circuit.

Generally, the performance of a circuit, designed on this basis, is rather poor, however, because of the extreme tolerance combinations that have been taken into account. On the other side, the probability that these extreme combinations occur is practically nil, the probability of "survival" of the circuit element being completely dependent on sudden failures, which are mostly of a non-systematic and catastrophic nature.

The choice of the components in the circuit blocks, the provisions taken in the manufacture of these components, as well as the special protective measures lead to a strong reduction of such sudden failures. Furthermore, a very safe electronic design procedure is followed, applying all available knowledge on the specific statistic behaviour of the components. In this way units with a high standard of reliability, a long life and a high electronic performance are obtained.

It stands to reason that a good performance of the circuit blocks can only be guaranteed, if the user, in his turn, sticks to the operating conditions given by the manufacturer. These operating conditions and guarantee, which apply to all types of circuit block, are given below.

## CHARACTERISTICS

Besides passive network elements (resistors, capacitors), only semiconductor devices are incorporated in the circuit blocks, viz. transistors, Ge-diodes and Si-diodes. As a result the inherent advantages of these semiconductors are reflected in the properties of the circuit blocks, such as low supply voltages and small power dissipation.

The standard supply voltage of the circuit blocks is +6 V and/or −6 V, so that no special measures with respect to insulation and protection need be taken.

The power dissipation of the blocks is so small (20 to 100 mW) that no special precautions are necessary with regard to cooling.

The 100 kHz circuit blocks are guaranteed to work properly at the maximum speed of operation under maximum load conditions as given in the Data sheets in the temperature range of −20 °C to +60 °C (−4 °F to +140 °F).
For storage the temperature limits of −25 °C and +75 °C must not be exceeded.

Though the circuit blocks function reliably at any combination of the margins given with respect to supply voltage and ambient temperature, the maximum operational safety margin and the maximum life can be expected by operating the units as closely as possible to the given nominal values of +6 V and −6 V for the supply voltages and 25 °C (77 °F) for the ambient temperature.

Apart from some output devices the circuit blocks are designed for an operational speed of 100 kHz. Because of the large safety margin that has already been taken into account, no further speed-derating is necessary.

# TEST SPECIFICATIONS

Before and during manufacture samples of circuit blocks are regularly subjected to the following tests.

(1) Shock test and vibration test according to method 202A and 201A of MIL-STD-202, terminals tested on strength, tests on mounting, soldering, lacquer and coding.

(2) corrosion test (salt haze), according to method 101A of MIL-STD-202 (condition B, 48 hours).

(3) temperature cycling test, according to method 102A of MIL-STD-202 (5 cycles from −25 °C to +65 °C).

(4) dip test, according to method 104A of MIL-STD-202 (2 cycles 65 °C/20 °C, condition B, NaCl).

(5) accelerated humidity test, according to method 106A of MIL-STD-202 (10 cycles 65 °C).

(6) Long-term humidity test (units not operating), according to I.E.C.68, C IV (40 °C, relative humidity: 90% to 95%, duration longer than 2000 hours, functional marginal measurements after 250, 1000 etc. hours).

(7) as item 6, but units operating under the most unfavourable electrical conditions.

(8) long-term test at max. temperature (60 °C), units operating under the most unfavourable electrical conditions. Duration and measurements as item 6.

# THE DESIGN OF A CIRCUIT WITH CIRCUIT BLOCKS

## BLOCK DIAGRAM

The growing complexity of the electronic system of to-day calls for a simple logical unambiguous way of representation in the system circuit diagram. Effective use is made of a block diagram, in which each symbol represents a specific unit function, which may represent a system component of different complexity. Such a block in the diagram may denote, for instance, anything between a complete production plant and a small basic electronic function, such as a flip-flop, a gate circuit etc. The latter can be considered as basic subassemblies for electronic systems. The circuit blocks belong to this category, each type representing a single functional element or a combination of two of such elements.

## BASIC LOGIC SYMBOLS

When a logic circuit is to be designed, whether it should be equipped with circuit blocks or any other elements, it may be useful to make up a block diagram without paying any attention to the technical set-up for the time being. In such a block diagram use can be made of symbols of purely functional elements, some of which are shown in Fig.3.

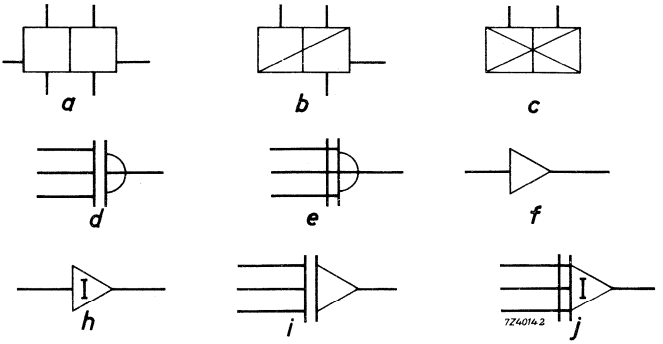



Fig.3. Symbols for logic circuits

a. bi-stable multivibrator (flip-flop)
b. mono-stable multivibrator (one-shot)
c. a-stable multivibrator
d. and-gate
e. or-gate
f. non-inverting amplifier (emitter-follower)
h. inverter
i. and-gate with emitter follower
j. or-gate with inverter

From the symbols in Fig.3 only the and-gate, the or-gate and the inverter perform a purely logic function. According to the Boolean algebra the relations between the output signal and the input signal of these elements are as follows:

AND-gate: (Fig.3d) : $P = A \,.\, B \,.\, C \,. \ldots\ldots\ldots . N$
OR-gate: (Fig.3e) : $P = A + B + C + \ldots\ldots\ldots + N$
Inverter (Fig.3h) : $P = \overline{A}$ ($\overline{A}$ = "NOT A")

A, B, C etc. can attain the values "0" (no signal) and "1" (signal). It should be remembered, that in terms of Boolean algebra $1 + 1 = 1$, so that the value of P in the OR-gate can never exceed 1. The action of the inverter is such, that an input signal "0" produces an output signal "1", or the reverse ($\overline{0} = 1$, $\overline{1} = 0$).

## VOLTAGE LEVELS AND SIGNAL VALUES

In a binary system two discrete states can be distinguished, to which the logical values "0" and "1" are assigned. In electronic circuits these values are commonly allocated to the output voltage(s) of a flip-flop, which, in the case of circuit blocks, are approximately 0 V and 0.7 $V_N$ or more negative ($V_N$ being the negative supply voltage).
Since it is immaterial, whether one of these voltage levels is indicated by "0" or "1", or vice versa, they are denoted by "negative low" (approx. 0 V) and "negative high" (0.7 $V_N$ or more negative).

## COMBINATION OF LOGIC SYMBOLS

When Boolean functions of a more complex character than those of the AND-gate, the OR-gate or the inverter are dealt with, combinations of these elements must be used. As an example the function $P = \overline{A \,.\, (B + C)}$ will be considered. This function is performed by the following logic circuit (Fig.4).

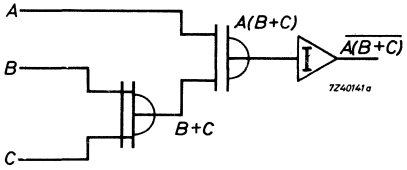



Fig.4. Logic circuit for obtaining the function $P = \overline{A \,.\, (B + C)}$.

In some cases, and specially when a particular arrangement cannot be used for technical reasons, another arrangement can be found by converting the function into an equivalent function, whereby the rules of Boolean algebra may come in useful. The function $P = \overline{A \,.\, (B + C)}$ can be converted into the function $P = \overline{A} + \overline{B} \,.\, \overline{C}$, which corresponds to the logic circuit of Fig.5. From the table below, in which all combinations of A, B and C are considered, it can easily be seen that the functions $P = \overline{A \,.\, (B + C)}$ and $P = \overline{A} + \overline{B} \,.\, \overline{C}$ are equivalent.

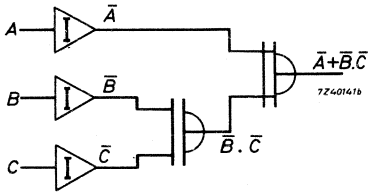



Fig.5. Logic circuit for obtaining the function $P = \overline{A} + \overline{B} \cdot \overline{C}$.

Table

| A | B | C | $\overline{A}$ | $\overline{B}$ | $\overline{C}$ | B + C | $\overline{B} \cdot \overline{C}$ | A(B + C) | $\overline{A(B+C)}$ | $\overline{A} + \overline{B} \cdot \overline{C}$ |
|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | 1 | 1 |
| 1 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 1 |
| 0 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 1 |
| 0 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 1 |
| 1 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 1 |
| 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 |
| 1 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 |

RULES OF BOOLEAN ALGEBRA

The equations given below can be used advantageously to simplify and convert logic functions. They can easily be verified by making up tables as shown above.

$A + 0 = A$
$A + 1 = 1$
$A + A = A$
$A + \overline{A} = 1$
$A + A \cdot B = A$
$A + \overline{A} \cdot B = A + B$
$A \cdot (B + C) = A \cdot B + A \cdot C$

$A \cdot 0 = 0$
$A \cdot 1 = A$
$A \cdot A = A$
$A \cdot \overline{A} = 0$
$A \cdot (A + B) = A$
$A \cdot (\overline{A} + B) = A \cdot B$
$(A + B) \cdot (A + C) = A + B \cdot C$

$(A + B) \cdot (C + D) = \overline{\overline{A} \cdot \overline{B} + \overline{C} \cdot \overline{D}}$

$(A \cdot B) + (C \cdot D) = \overline{(\overline{A} + \overline{B}) \cdot (\overline{C} + \overline{D})}$

$A + B + C + \ldots\ldots\ldots\ldots + N = \overline{\overline{A} \cdot \overline{B} \cdot \overline{C} \ldots\ldots\ldots \cdot \overline{N}}$

$A \cdot B \cdot C \cdot \ldots\ldots\ldots\ldots \cdot N = \overline{\overline{A} + \overline{B} + \overline{C} \ldots\ldots\ldots + \overline{N}}$

$\overline{A} + \overline{B} + \overline{C} + \ldots\ldots\ldots\ldots + \overline{N} = \overline{A \cdot B \cdot C \ldots\ldots\ldots \cdot N}$

$\overline{A} \cdot \overline{B} \cdot \overline{C} \cdot \ldots\ldots\ldots\ldots \cdot \overline{N} = \overline{A + B + C \ldots\ldots\ldots + N}$

## SYMBOLS FOR CIRCUIT BLOCKS

After the block diagram with logic symbols has been made up, the logic symbols should be translated into circuit blocks. To this end a wiring diagram is made in which the logic symbols are replaced by symbols representing the corresponding circuit blocks. The latter symbols, recommended for this purpose, are given in the Data Sheets of the circuit blocks. Each of these symbols consists of a rectangle, in which the type of circuit block and the connections are indicated (Fig.6). Since also the reference numbers of the connecting leads are indicated in the symbol, the equipment can be constructed directly from the circuit block diagram.

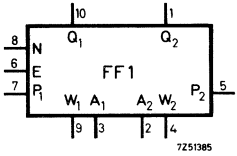



Fig.6. Typical symbol of a circuit block (FF1).

In Fig.7 an example is given of how logic symbols can be combined so as to obtain an arrangement that can be built up from circuit blocks. In this figure the convention "negative low" = "0" and "negative high" = "1" has been adopted, which involves, that the AND-operation is performed by an N-gate and the OR-operation by a P-gate (see under "Gates" in section "Operational Notes").

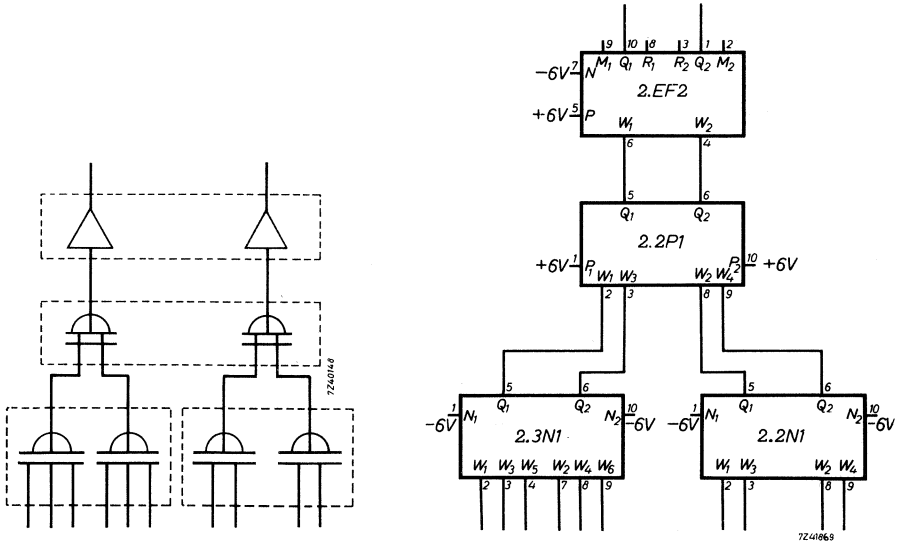



Fig.7. Translation of logic functional symbols into circuit block symbols.

## THE LOADING TABLE

Since the loadability of circuit blocks is limited, they may not be arranged arbitrarily. A circuit block diagram, made up from a diagram with logic symbols, should be carefully checked on the basis of the Loading Table.
From this table the number of units that can be driven by any other unit can be taken. When a unit has output terminals with different loadability these data are given separately.

It may be noted that the Loading Table is made up for combinations of units under supply voltage tolerances of ± 5%, whilst part of the earlier types of blocks (see data sheets) allow for a supply voltage tolerance of ± 10%.
The gain in performance obtained at those reduced tolerances has been taken into account in the table. In those cases where a proper functioning is assured a pulse rise time of 0.7 μs has also been calculated with, though 0.4 μs has been prescribed earlier. The result is an overall improvement in loadability in the Loading Table compared with earlier publications.

In the case of amplifier units, the output data are dependent on the input driving signal; for these units the loadability is given for different preceding units or preceding chain of units.

The EF 2 is especially suited to drive a common-emitter stage; for this combination the loadability is also given.

The number of negative gates (N 1) which can be driven by any other unit at a "negative low" output level, depends, due to diode leakage current, on the number of other gate inputs which are at a "negative high" level. In this Loading Table the assumption is made that three other inputs of each driven gate are at a "negative high" level.

If not indicated separately in the Loading Table all N and P terminals of each unit are connected to $V_N$ respectively $V_P$.

The general set-up of the Loading Table is elucidated in the diagram given below.

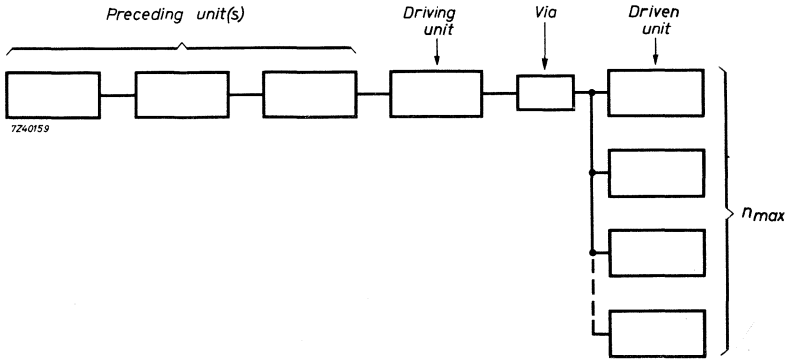



Fig.8. Diagram to explain the Loading Table.

If a specific combination of circuit blocks appears to be inadmissible, it should be rearranged into a permissible combination. Boolean algebra can be used for this purpose.

In some cases a loading, differing slightly from that given in the Loading Table, may be possible.
In this case it must be carefully checked, whether the input signal requirements of the driven units do not exceed the given corresponding output data of the driving unit. It also should be considered that the limiting values of the input signals of the driven unit are never exceeded.
This concerns the values of voltage levels, currents and switching times, which can be derived from the data sheets.

# SOME PRACTICAL CIRCUITS

In this section some practical examples are given for the application of 100 kHz circuit blocks. Since most circuit blocks comprise twin units or two separate functional units in certain cases only half the symbol is given.

For the sake of simplicity the supply lines are not drawn in many of the figures given below. Normally the N terminals are connected to the −6 V supply, the P terminals to the +6 V supply and the E terminals to earth (common to both supply voltages). If a supply terminal should not be connected to the corresponding supply line this is indicated by "n.c." (not connected).

In the applications given the following convention is adopted:

"negative low" = binary "0"
"negative high" = binary "1".

According to this convention a Negative gate (2.3N1 or 2.2N1) is employed to perform the logical AND operation and a Positive gate (2.3P1 or 2.2P1) to perform the logical OR operation (see Operational Notes).

SCALERS

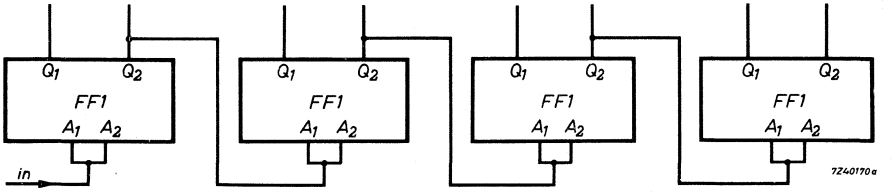



Fig.9. Scaler of 16 (Binary counter with 4 flip-flops)

Below some scalers are given in which pulse feed-back is applied to obtain a dividend that is not a power of 2.

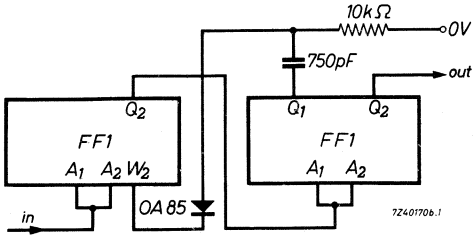



Fig.10. Scaler of 3

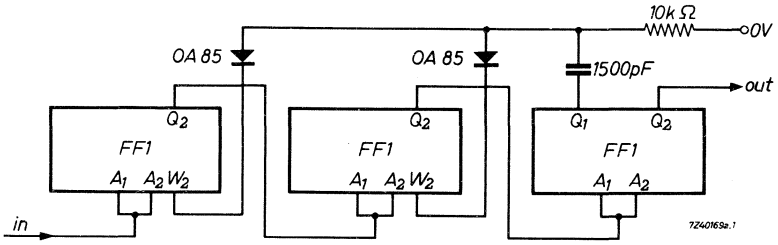



Fig.11. Scaler of 5

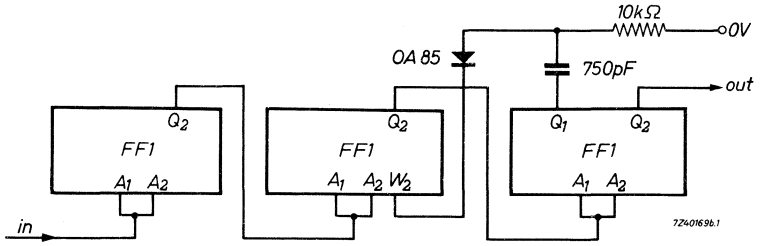



Fig.12. Scaler of 6

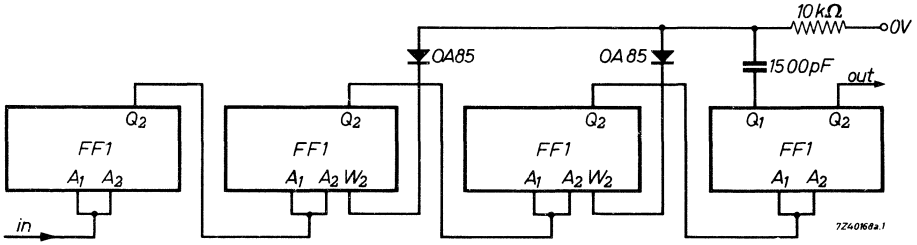



Fig.13. Scaler of 10 (decimal counter)

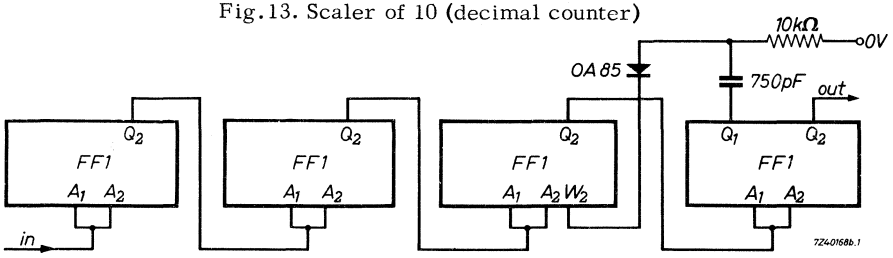



Fig.14. Scaler of 12

Apart from the above mentioned pulse feedback principle also an intermediate gate can be used to skip a number of positions in order to attain scalers of dividends that are no powers of 2. The advantages of this type of circuit is that spurious pulses, as occurring at the output of the scaler with pulse feedback, are avoided. An example of a decimal counter designed on this principle is given below.

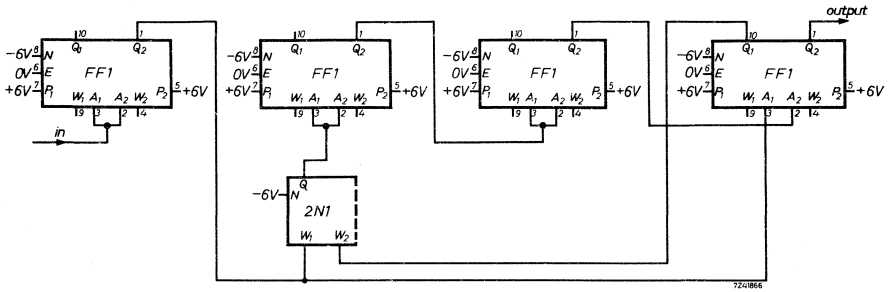



Fig.15. Decimal counter, maximum speed 60 kHz

For a speed of 100 kHz the resistor in the 2N1 block must be shunted externally by a 12 kΩ ±5% resistor or the 2N1 must be replaced by a circuit block 2.IA1, connected to perform the same gate function.

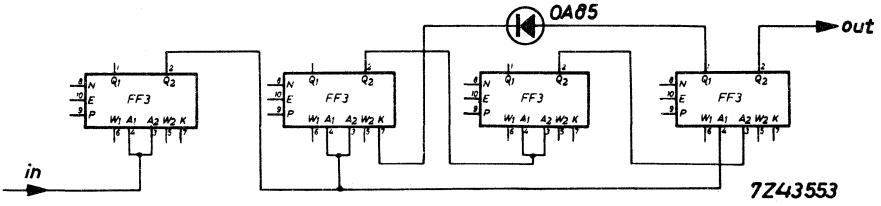



Fig.16. Decimal counter, maximum speed 100 kHz

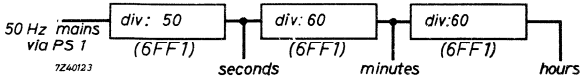



Fig.17. Time code frequency divider

## MULTIPLE INPUT GATES

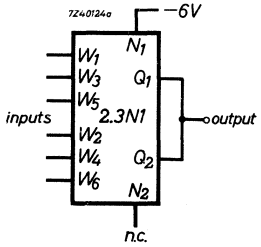



Fig.18. 6-input N-gate composed of one 2.3N1

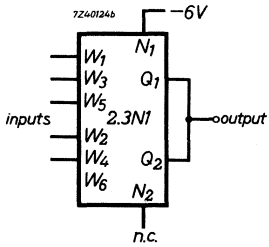



Fig.19. 5-input N-gate composed of one 2.3N1

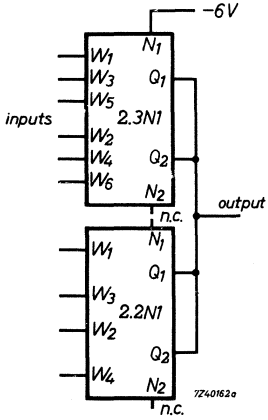



Fig.20. 10-input N-gate composed of one 2.3N1 and one 2.2N1

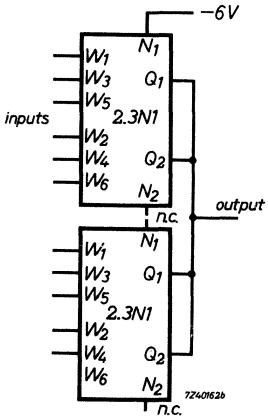



Fig.21. 11-input N-gate composed of two 2.3N1's

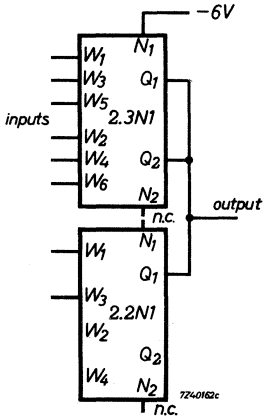



Fig.22. 8-input N-gate composed of one 2.3N1 and half a 2.2N1.

BINARY TO DECIMAL CONVERTER

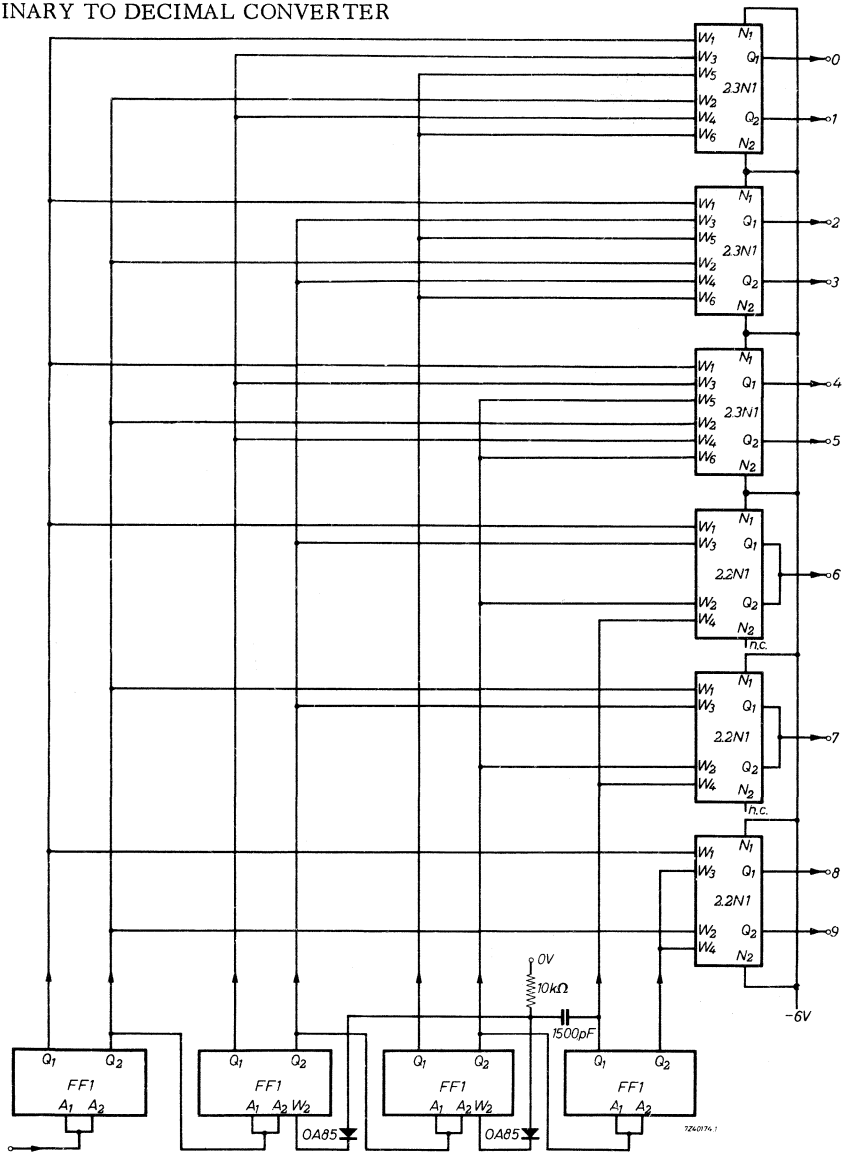



Fig.23. A count of n in the decimal counter produces a "1" signal at the output n at the right. All N, E and P terminals of the flip-flops should be connected to the corresponding supply lines.

PRESET COUNTERS

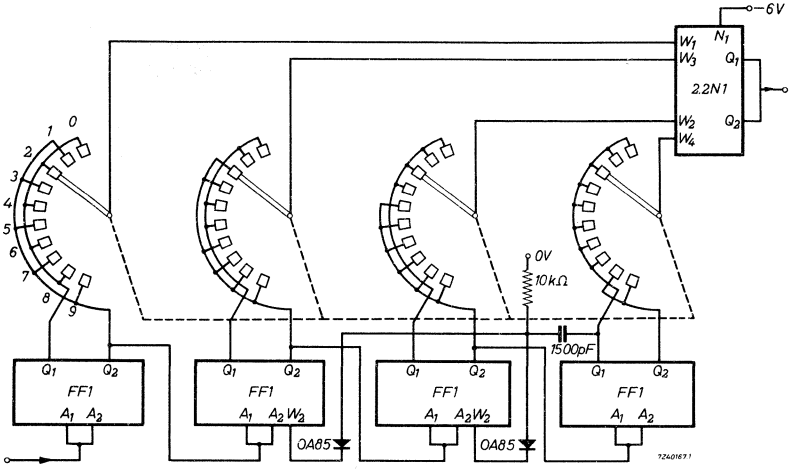



Fig.24. General purpose circuit. An output voltage is produced when the decimal counter stores the number chosen by means of the 10-position 4-wafer switch. The circuit may also be used for the determination of a time interval by counting cycles of an alternating voltage, e.g. the mains.

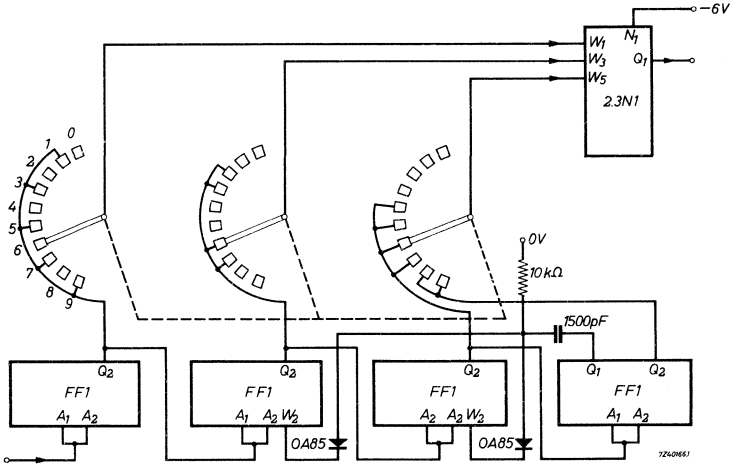



Fig.25. Simplified circuit for special applications. An output signal is produced when the decimal counter has reached the number chosen by means of the 10-position 3-wafer switch. When this number is exceeded the output signal may stay or recur. This phenomenon makes the circuit only useful for those applications in which these spurious signals do not interfere.

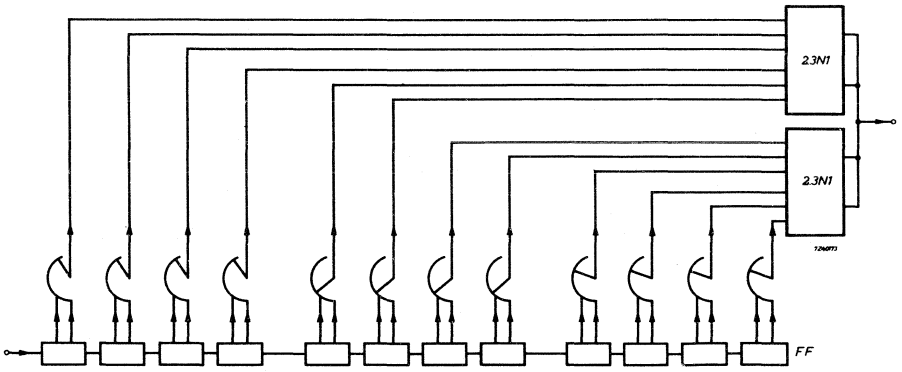



Fig.26. When the counter consists of several decades, it may be preselected by as many 10-position switches. The gates are combined to one gate. The circuit may also be of the 3-wafer switch type, as shown in Fig.19.

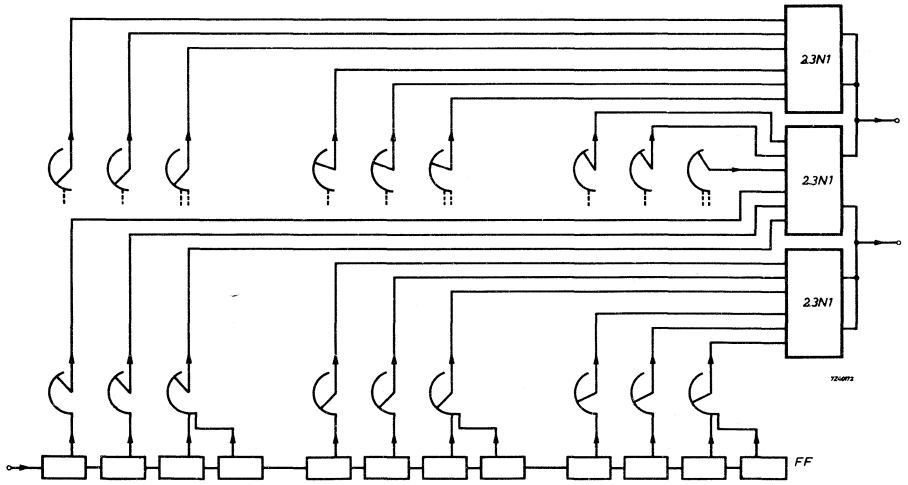



Fig.27. Preset counter with multiple programmes. More than one set of switches and gates may be connected to the same counter. Every output gives a signal when the counter has reached the number set by its associated switches. The switches may be of the 3 or 4-wafer type.

## SHIFT REGISTERS

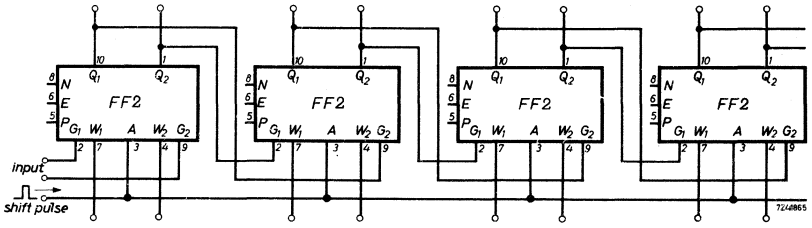



Fig.28. Shift register

Binary information, applied to the input terminals in complementary form, is shifted bit after bit into the register by means of the shift pulse. Set or Reset signals can be applied in parallel to the corresponding W terminals in the usual way (see Set and Reset circuits).

The outputs of the last FF2 can be connected crosswise to the gate inputs of the first ($Q_1$ to $G_2$ and $Q_2$ to $G_1$). A given information stored in the register will now circulate through it by means of the clock pulse.

By connecting the outputs of the last FF2 directly to the gate inputs of the first ($Q_1$ to $G_1$ and $Q_2$ to $G_2$) scalers can be made which can very easily be decoded and preset; with 5 FF2's, e.g. a decimal counter can be made.

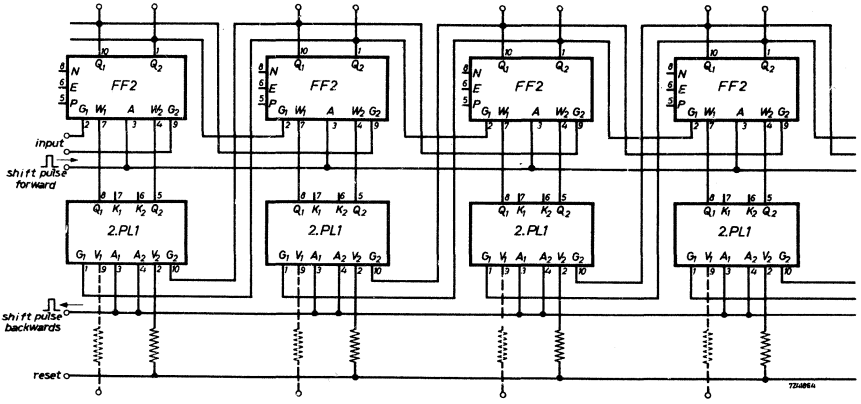



Fig.29. Bi-directional shift register

The circuit of Fig.28 can easily be converted into a bi-directional shift register by adding additional input pulse gates as incorporated in the unit 2.PL1. The information in the register can be shifted in both directions dependent on the input to which the shift pulse is applied. In the same way bi-directional decimal counters can be made according to the principle as indicated above.

The diodes, incorporated in the 2.PL1 (inputs $V_1$ and $V_2$) can be used for negative Set or Reset signals.

DRIVE CIRCUITS FOR SHIFT REGISTERS

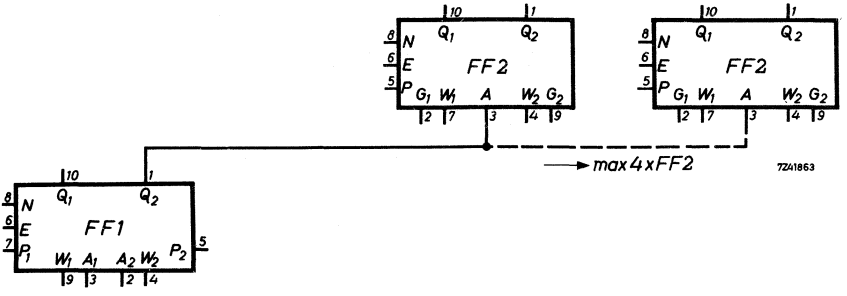



Fig.30

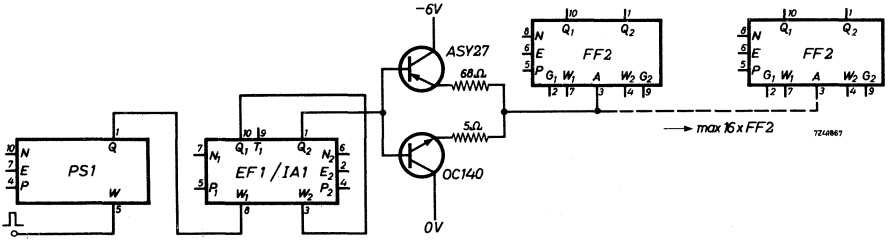



Fig.31

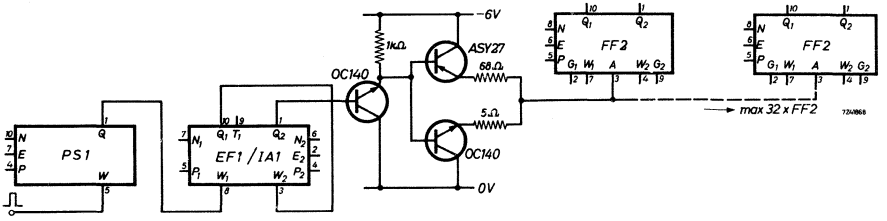



Fig.32

## SET AND RESET CIRCUITS

A system in which flip-flops are used, often requires a means for setting or resetting. This can be realised as indicated in the figures below.

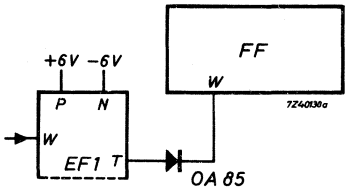



Fig.33

| | |
|---|---|
| Input signal for resetting: | "0" (negative low) |
| Driving unit: | FF1, FF2, IA1, IA2, PS1 or OS1 |
| Maximum number of flip-flops: | 1 |

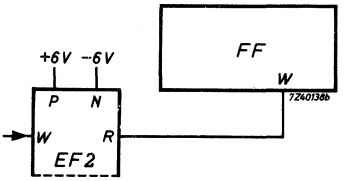



Fig.34

| | |
|---|---|
| Input signal for resetting: | "1" (negative high) |
| Driving unit: | N-gate or N-P gate sequence |
| Maximum number of flip-flops: | 1 |

A simple circuit for resetting flip-flops by a flip-flop FF1 is given in the figure below.

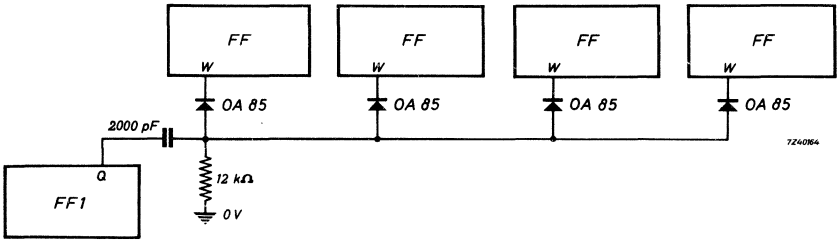



Fig.35

Resetting takes place on a positive voltage step at the Q terminal of the drving flip-flop.

When a large number of flip-flops has to be controlled, the following arrangement can be used.

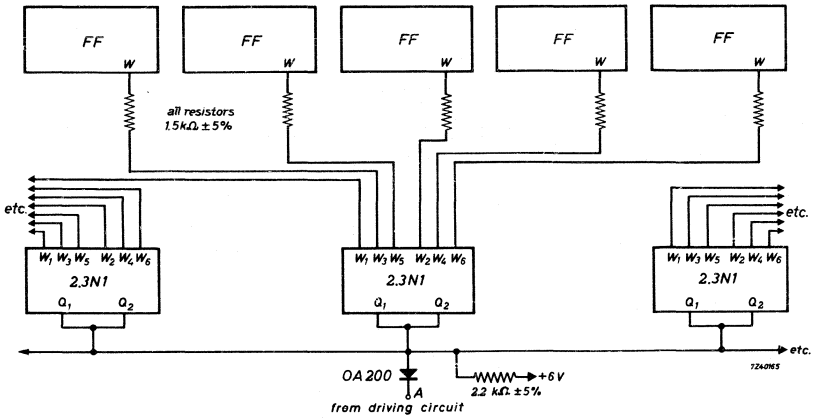



Fig.36

The circuit of Fig.36 can be driven by one of the circuits given below.

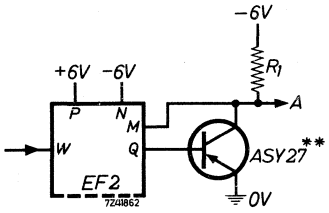



Fig.37

| Input signal for resetting: | "0" (negative low) | | |
|---|---|---|---|
| Driving unit | FF1, FF2, IA1, IA2, PS1 or OS1 | N1 | N1-P1 |
| Value of resistor $R_1$ in Ω ±5 % [1]) | 82 | 150 (82) | 330 (200) |
| Max. number of flip-flops[1]) | 32 | 15 (32) | 5 (10) |

[1]) The values between brackets apply to the circuit without the anti-bottoming connection (EF2-M terminal to collector ASY27). Consequently this circuit is for low speed operation only.

**) See Fig.45.

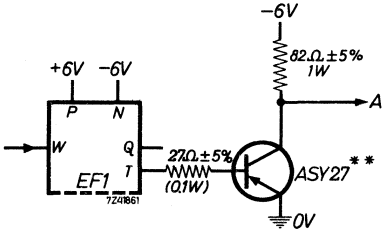



Fig.38. (Low speed operation only)

Input signal for resetting: "0" (negative low)
Driving unit: FF1, FF2, IA1, IA2, OS1 or PS1
Maximum number of flip-flops: 32

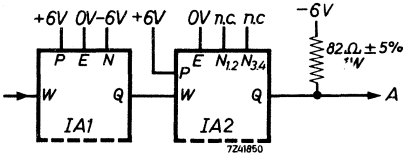



Fig.39

Input signal for resetting: "1" (negative high)
Driving unit: FF1, FF2, IA1, IA2, OS1 or PS1
Maximum number of flip-flops: 32

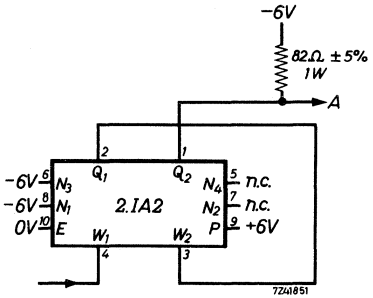



Fig.40

Input signal for resetting: "1" (negative high)
Driving unit: N1, N1-P1, IA1, IA2 or PS1
Maximum number of flip-flops: 32

**) See Fig.45

## AMPLIFIER CIRCUITS FOR GATE SIGNALS

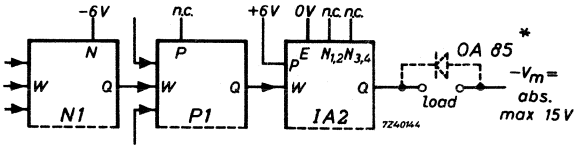



Fig.41. $I_{load}$ = max. 5.5 mA

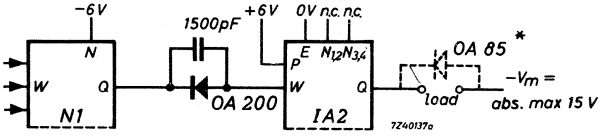



Fig.42. $I_{load}$ = max. 5.5 mA

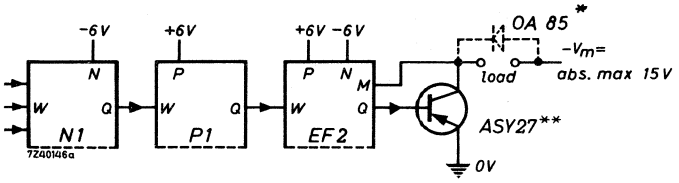



Fig.43. $I_{load}$ = max. 13 (29) mA [1])

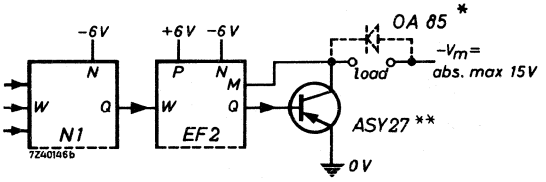



Fig.44. $I_{load}$ = max. 35 (50) mA [1])

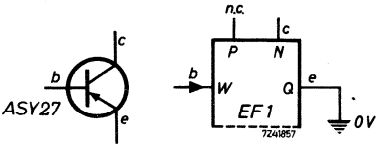



Fig.45. In the circuits given the transistor ASY27 can be replaced by the EF1 circuit.

---

[1]) The values between brackets apply to the circuit without the anti-bottoming connection (EF2-M terminal to collector ASY27). Consequently this circuit is for low speed operation only.

*) In case of inductive load.

**) See Fig.45.

AMPLIFIER CIRCUITS

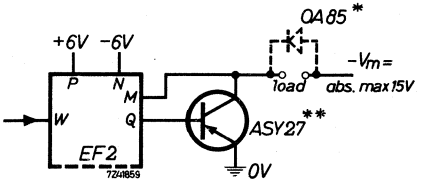



Fig.46

Driving circuit: FF1, FF2, IA1, IA2, OS1 or PS1
$I_{load}$: max. 70 (85) mA [1])

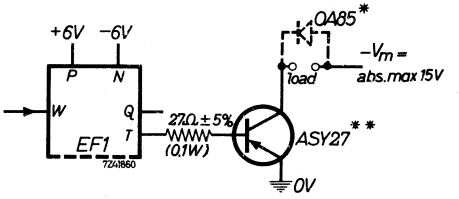



Fig.47

Driving circuit: FF1, FF2, IA1, IA2, OS1 or PS1
$I_{load}$: max. 85 mA

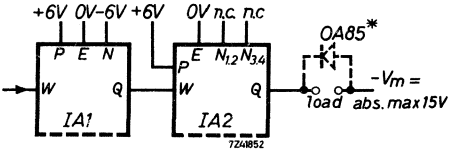



Fig.48

Driving circuit: FF1, FF2, IA1, IA2, OS1 or PS1
$I_{load}$: max. 85 mA

---

[1]) The values between brackets apply to the circuit without the anti-bottoming connection (EF2-M terminal to collector ASY27). Consequently this circuit is for low speed operation only).

*) In case of inductive load.

**) See Fig.45.

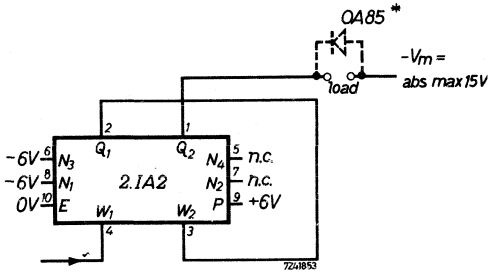



Fig.49

Driving circuit: N1, N1-P1, IA1, IA2, PS1
Iload: max. 70 mA

POWER AMPLIFIER CIRCUITS

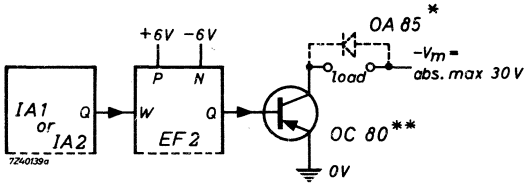



Fig.50. $I_{load}$ = max. 250 mA

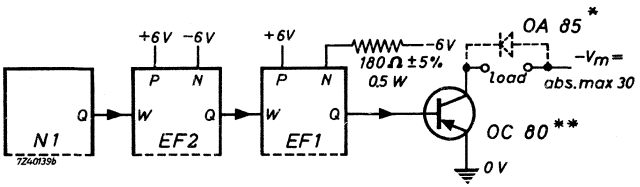



Fig.51. $I_{load}$ = max. 300 mA

*) In case of inductive load
**) The transistors have to be mounted on a heatsink (see relevant transistor data).

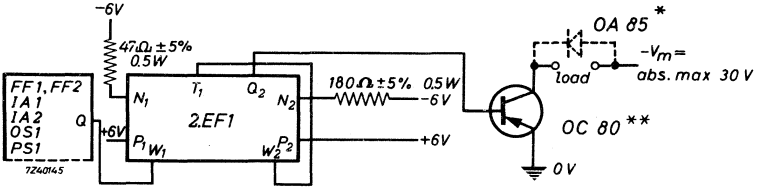



Fig.52. $I_{load}$ = max. 300 mA

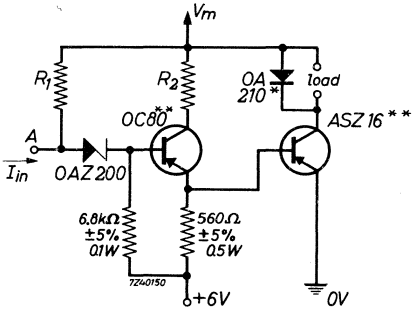



Fig.53

| | | | |
|---|---|---|---|
| Voltage | $-V_m$ | 12 V ±15 % | 24 V ±15 % |
| Resistors | $R_1$ | 470 Ω ± 5 %, 1 W | 2.4 kΩ ± 5 %, 0.5 W |
| | $R_2$ | 68 Ω ± 5 %, 5 W | 150 Ω ± 5 %, 10 W |
| Input current | $-I_{in}$ | min. 35 mA | min. 13.5 mA |
| Load current | $I_{load}$ | max. 2.6 A | max. 2.6 A |
| Driving circuits | | Fig.44 to 49 | Fig.43 to 49 |

If there is a preference to use an output transistor ASZ17 or ASZ18 instead of the ASZ16, the stated maximum load current $I_{load}$ has to be multiplied by 0.6.

*) To be used in case of inductive load.

**) The transistors have to be mounted on a heatsink (see relevant transistor data).

## PHOTO-ELECTRIC PICK-UPS

With a circuit block PS1 very simple photo-electric pick-ups can be made. For the output data of the circuits given below see the PS1 data sheet.

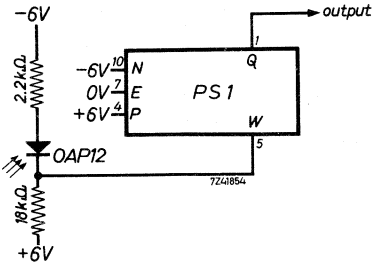



Fig.54

Switching level: min. 13000 Lux (this lighting level can be achieved with a lens-end incandescent lamp of 2.2 V; 0.25 A)

Max. ambient temperature: 60 °C

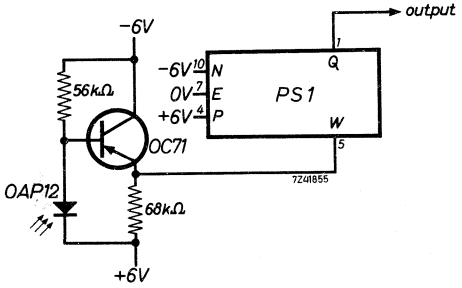



Fig.55

Switching level: min. 3000 Lux (this lighting level can be achieved with a lens-end incandescent lamp of 2.2 V; 0.25 A)

Max. ambient temperature: 60 °C (only if the OAP12 and OC71 have been matched for proper leakage current compensation).

## OSCILLATOR CIRCUITS

With a circuit block PS1 it is possible to make square wave oscillator circuits as given in the figures below.

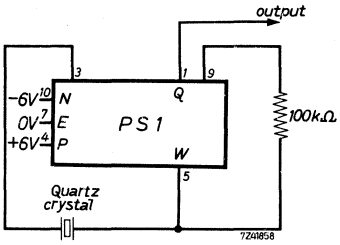



Fig.56. Crystal controlled oscillator circuit. For the output data of this circuit see the PS1 data sheet.

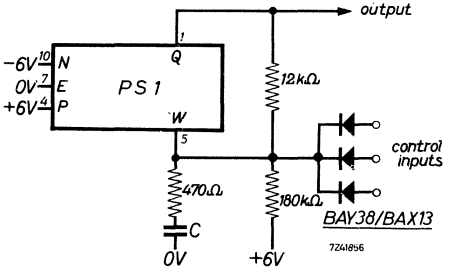



Fig.57. Relaxation oscillator circuit. The oscillator may be controlled by more control signals as indicated in the figure. A "0" (negative low) level on one of these inputs stops the oscillator.

| | | | | | |
|---|---|---|---|---|---|
| For a capacitor value | C = 2500 pF | f | = approx. | 100 | kHz |
| | C = 250 μF | f | = approx. | 1 | Hz |

Output data:

| | | | | | |
|---|---|---|---|---|---|
| Output level "negative low" | Voltage | $-V_Q$ | max. | 0.2 | V |
| | Load current | $-I_Q$ | max. | 1.2 | mA |
| Output level "negative high" | Voltage | $-V_Q$ | max. | -0.7 | $V_N$ |
| | Load current | $I_Q$ | max. | 0.3 | mA |

For further data see PS1 data sheet.

# OPERATIONAL NOTES

This chapter contains some general and specific remarks on the application of circuit blocks.

## FLIP-FLOP

### D.C. input signal

The flip-flops FF1, FF2, FF3 and FF4 can be set or reset on the W terminals by a negative or positive d.c. level. Attention should be paid to the W inputs being directly connected to the transistor base. When driven by a low-impedance source (e.g. the direct output of an emitter-follower or the negative power supply line) the transistor may be seriously overdriven and hence destroyed. The maximum permissible input current should therefore never be exceeded.

If the memory property of the flip-flop has to be maintained, the driving source should have a one-way action on the flip-flop; the source should therefore be connected to the W terminal by means of a series diode (see p. A26: SET AND RESET CIRCUITS). In order to attain a correct cut-off voltage level for this diode, the emitter-follower units EF1 and EF2, which can be used as driving sources for the flip-flop, are provided with a tapped output. The voltage level on the tap has the required value if the emitter-follower is driven by a "0" (negative low) signal.
The EF2 circuit block comprises the series diode ($M_1$ and $M_2$ output terminals).

### Cascading of flip-flops

With n cascaded flip-flops FF1 or FF3 it is possible to construct frequency dividers with a dividend of $2^n$. When such a chain of flip-flops is used for counting, the total counting capacity amounts to $2^n$ as well.
By using a pulse feedback or gating principle it is possible to skip a given number of counts, so that with n flip-flops any dividend up to $2^n$ can be obtained. When a dividend of N is required, the minimum number of flip-flops (n) can be derived from:

$$2^{n-1} < N \leq 2^n.$$

Pulse feedback is required when $N \neq 2^n$, so that $2^n$ N positions are skipped. The value of $2^n - N$ gives the indication to which flip-flop in the series the feedback should be applied. In Figs. 11 to 15 a few examples of FF1 counters are given. The feedback pulse is supplied to the preceding flip-flops via a pulse gate circuit.

The value of the capacitor in this circuit is determined by the number of flip-flops to which the feedback pulse has to be supplied, viz. approximately 500 pF per flip-flop.
Care should be taken, that the maximum permissible capacitive load of the flip-flop that supplies the feedback pulse is not exceeded. The maximum capacitive loading of the FF1 is 2000 pF. For both Q terminals together when the FF1 is loaded during the negative as well as the positive transient of the pulse. If a 1500 pF series capacitor is used in the feedback path, 500 pF is left for external loading on that terminal (equivalent to another flip-flop). If more than four feedback paths are required, the signal may also be taken from one of the preceding flip-flops.
A disadvantage of this type of counter is that a spurious pulse occurs at the outputs of the flip-flops to which the feedback pulse is applied (see e.g. the output levels of the DC1 as given in the corresponding Data Sheet). If the occurrence of this pulse is not wanted an intermediate gate can be used as indicated in Fig.15.
In Fig. 16b a similar type of decade counter is given, but now equipped with flip-flop FF3. With this FF3 however the intermediate gate has been built in the unit itself. The gate condition derived from the $4^{th}$ flip-flop is connected to the extended gate terminal of the $2^{nd}$ FF3 via a diode.

Shift registers

The flip-flops FF2 and FF4 are in principle equivalent to the FF1 and FF3 circuits respectively, with the exception that the built-in input pulse gates can be controlled externally. In this way the switching of the unit, upon reception of a positive going voltage step on its A input is determined by the d.c. levels applied to its G inputs. Thus the binary information presented to the G inputs can be shifted into the flip-flops by the voltage step on A.
The pulse gates are opened by a "negative low" level and closed by a "negative high" level on the corresponding G input.
It is to be noted that for proper working the $G_1$ and $G_2$ terminals may not be at a "negative low" level simultaneously.
The units 2.PL1 and 2.PL2 (Dual Pulse Logic) contain the input gate circuitry of the normal flip-flop FF1 and FF2, and FF3 and FF4 respectively. In this way it is possible by connecting these units to an FF1 and FF3 respectively to obtain a second A input on this unit. In combination with FF2's and FF4's respectively bi-directional shift registers can be made.
In the figures 28 and 29 examples are given of a uni- and a bi-directional shift register.

## GATES

### General

As mentioned before, it is immaterial which binary level is denoted by the logic value "0" or by "1", since it has no influence whatsoever on the logic design of a circuit. However, confusion may arise when gate circuits are discussed. Many designers use the words AND and OR for the basic logic functions as well as for the electronic circuits that perform these specific logic operations. The notations AND and OR should, however, be restricted to logic operations, since one gate circuit can perform both the AND and OR operation, dependent on the designation of "0" and "1" to the voltage levels used.
For the above reasons the circuit blocks comprising gate circuits are denoted by "NEGATIVE GATE" and "POSITIVE GATE". The negative gate performs the AND operation on "negative high" signals and the OR operation on "negative low" signals, whilst the positive gate performs the OR operation on a "negative high" signal and the AND operation on a "negative low" signal (see Table below).

| Signal value "1" assigned to: | Logic operation performed by | |
|---|---|---|
| | Positive gate | Negative gate |
| "Negative high" level | OR | AND |
| "Negative low" level | AND | OR |

### Gate Sequence: Always negative gate - positive gate

Technically it is only possible to drive a positive (P) gate by a negative (N) gate. In the system where the "negative high" signal corresponds to binary "1", the AND-OR sequence is therefore allowed only. This means that every OR-AND combination in the logic diagram should be converted into an AND-OR combination. An example of such a conversion was already given on page A12. It may be convenient to remember that an AND-gate is an OR-gate for the signal of opposite polarity and vice versa. At the outputs of a flip-flop a signal and its complement are simultaneously present, so that no inverter need be used when the signal is taken from a flip-flop.

### Cascading of gates: no more than two

Cascading of more than two gates must generally be avoided. This is due to a large increase of the load on the driving unit when gates are connected in cascade, so that the signal level shift (signal loss) may amount to impracticable values.
An N-N or P-P gate sequence is generally not allowed; such a sequence can, however, always be replaced by one multiple N or P gate respectively.

After a signal has passed an N-gate or an N-P gate sequence, it must be restored by an inverter amplifier IA2, an emitter-follower EF2 or a pulse shaper PS1.

Gates with multiple inputs

In many cases gates with more than three inputs may be required. Such a gate may be composed of any number of 2- or 3-input gates. The following rules should then be observed:

1. Interconnect the Q-outputs.
2. Connect the negative supply N only once for the whole gate, leaving the other terminals $N_1$ or $N_2$ floating.
3. If the newly composed gate would have more inputs than actually necessary leave the unused inputs floating.
4. A P-gate driven by an N-gate may have 25 inputs at maximum.
5. When part of the number of inputs of an N-gate are at "0" level and the other inputs at "1" level, the supply of the leakage currents of the diodes that are cut-off is distributed over the inputs at zero level. (The maximum of this leakage current is 40 $\mu$A for every input in the "1" position.) This may give rise to a considerable increase of the load at these inputs. (See also the corresponding Data Sheets.)

Examples of multiple-input gates are given in Figs. 18 to 22.

Positive gates

The rules given above under 1, 2 and 3 for N-gates also apply to P-gates. It must be noted, however, that, unlike the N-gate, the P-gate may load the driving stage at both binary levels.
The terminals $P_1$ or $P_2$ of the P-gate may be left floating when the following stage is already equipped with a resistor from the input to the positive supply voltage. This is the case with the inverter-amplifiers IA1 and IA2.
When a P-gate is driven by an N-gate, the number of P-gate inputs may not exceed 25. On the other hand, an N-gate may be loaded by only one P-gate.

More than one gate driven by more than one flip-flop

The Loading Table indicates the number of gates with which the other circuit blocks may be loaded. It should be remembered, however, that an N-gate only presents a "load" if it produces a "negative low" signal at its output. When several gate inputs carry a "negative low" signal simultaneously, the load is divided among the driving sources. When a number of gates is driven by a number of flip-flops, it may therefore be allowed to connect each flip-flop to a number of gates greatly exceeding that given in the Loading Table. That is because the

effective loading may be far less than the actual number of gates. This must be checked carefully for every possible state of the circuit.
The same applies, as a matter of course, for other driving sources.

Voltage levels in gate circuits

Due to the voltage drop across the diodes of the gates, a voltage level shift will occur in every gate, so that the signal, after having passed one or more gates, is no longer in agreement with the level standards of the input signals. In the Loading Table this effect has already been taken into account. When a combination of gates that is not covered by the Loading Table must be used, the following information should be borne in mind:

1. A germanium diode in an N-gate causes a level shift of −0.1 V to −0.5 V [1].
2. A silicon diode in a P-gate causes a level shift of +0.4 V to +1.0 V [1].
3. A common emitter stage needs −0.2 V to −0.4 V on its base for the conducting state and approximately +0.2 V for its cut-off state [1].
4. The collector-voltage level of a conducting common emitter stage ("0" output) has to be taken as −0.05 V to −0.2 V [1].

Current in gate circuits

Since the forward resistance of a conducting diode and the input impedance of a common emitter transistor, when driven into the conducting state, is very low, a strong gate current may occur, which may overload or damage the circuit elements.
On the other hand, the generator impedance of an "open" gate is high, resulting sometimes in too low an available driving current for a given stage. When applying other combinations, such as given in the examples below or in the Loading Table, these points have therefore to be investigated.

ONE-SHOT MULTIVIBRATORS OS1 AND OS2

The one-shot multivibrator OS1 is intended to produce a pulse of definite length for providing a time delay. Both a positive- and a negative-going pulse are available at the outputs. It should be noted that at the $Q_2$ terminal the maximum permissible load current is appreciably lower than that at the $Q_1$ terminal, whilst the rise time of the pulse at the $Q_2$ terminal is higher than that at the $Q_1$ terminal.

[1]) Related to the type of semiconductor as used in the circuit blocks and dependent on the current flowing through the diodes. In calculations on the levels the most unfavourable limit of the values given has to be applied.

It is not recommended to use the OS1 for delays that exceed the values given in the graph (see Data Sheets), i.e. longer than 1 ms, since in this case the OS1 is more sensitive to spurious signals induced on the supply line. Moreover, the use of electrolytic capacitors would be required, which are less stable during life and may show a considerable leakage current. For long delays it is therefore recommended to use a frequency divider fed from a fixed frequency, such as the a.c. mains.
When the OS1 is used for long delays the negative supply line should be bypassed close to the unit by a large capacitor.
The one-shot multivibrator OS2 has considerable advantages above the OS1 in particular with respect to the maximum permissible load current on both Q-terminals whilst the rise time of the pulses derived from $Q_1$- and $Q_2$-terminal are equal (see Data Sheets).

## TRANSIENTS AND DELAY TIMES

Although all circuit blocks function properly in any permitted sequence at frequencies up to 100 kHz, practical considerations may cause a reduction of this speed. This may happen when the total delay in a chain of cascaded circuits is too long for the specific application. It must be examined on the basis of the switching times and delay times as given in the Data Sheets.

As a typical example an 8-stage binary counter with flip-flops FF1 will be considered. From the Data Sheet it follows, that in this counter a total delay of $8.(t_{rd} + t_r) = 8.8\ \mu s$ occurs. If the output signal of the $8^{th}$ flip-flop should coincide with the input pulse of the counter for at least $2\ \mu s$, it is required for this input pulse to have a duration of minimum $8.8\ \mu s + 2\ \mu s = 10.8 \mu s$. This requirement reduces the maximum operational frequency in the application at issue to approximately 46 kHz.

The transients in a loaded switching circuit can be calculated from the output data given in the Data Sheets.
The intrinsic switching times given in these data always apply to the unloaded condition. Generally they remain unaffected under conditions of resistive loading, whereas a capacitive load increases the switching times.

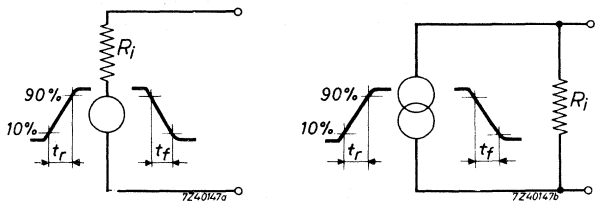



Fig. 58 Equivalent diagrams of active circuit blocks

The actual switching time of a loaded circuit can easily be calculated from the equivalent diagrams shown in Fig. 58. The unit can be represented by a step voltage or current source in combination with the internal (output) impedance of the unit. The value of this output impedance is given in the Data Sheet of the unit under consideration. The total rise time and fall time of the output voltage are approximately equal to:

$$t_{r\ tot} = \sqrt{t_r^2 + (2.2\ \tau)^2} \text{ and } t_{f\ tot} = \sqrt{t_f^2 + (2.2\ \tau)^2}$$

in which:

$t_r$ = the intrinsic rise time of the unit,
$t_f$ = the intrinsic fall time of the unit,
$\tau$ = the time constant of the load and internal resistance of the unit.

When the load consists of the parallel circuit of a resistive part $R_l$ and a capacitive part $C_l$ (which will mostly be the case):

$$\tau_l = \frac{R_l \cdot R_i}{R_l + R_i} \cdot C_l,$$

in which $R_i$ is the internal resistance of the unit.

# ELECTRICAL INTERFERENCE AND APPROPRIATE COUNTER-MEASURES

## Introduction

In industrial applications of transistorized electronic equipment sometimes troubles are encountered caused by interfering signals.
In designing equipment in which circuit blocks containing transistorized circuits are applied it is very important to pay due attention to the various possible sources of interference.
Interfering signals, mostly present during a short interval, can temporarily disturb the regular signals. In sequential circuits e.g. a one-shot multivibrator or flip-flop circuit (with a memory function), the interfering signal may be stored as a piece of information. In industrial equipment with transistor circuits interference is often produced by the switching of electro-magnetic loads, such as: relays, clutches, electro-magnetic valves, motors, transformers, welding apparatus, etc..
In almost all cases, however, these interference problems can be fully overcome by observing a number of simple design rules.
Most of these rules refer to the circuit lay-out, the wiring etc., so that they can only be applied efficiently and in the most effective way, when they have been duly accounted for at the outset of the development. Any correction afterwards is costly, time consuming and often even impossible.

## Transistors versus Tubes and Relays in Control Equipment with respect to Interference

Relay systems which operate at a very high power level are by nature very insensitive to interference.
In electronic control circuits a much lower signal power level is applied which consequently can be easily upset by interfering signals that are caused by external stray fields. In such cases special precautions are required.
It is not generally recognised that thermionic tube and transistor equipment behave quite differently in this respect.
In tube circuitry with higher voltage levels mostly higher interference levels are allowed. Because of the rather high impedance of the signal lines most interference is of capacitive nature, a capacitive screening of the signal lines is in many cases sufficient.
Transistor circuitry mostly operates at a much lower voltage level and has a lower impedance. Here a relatively higher sensitivity to magnetic stray interferences can be found. In these circuits a simple capacitive screening only solves a small part of the problems.

The sections below contain a survey of various kinds of interference and indications as to their elimination or reduction.

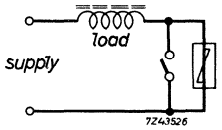
Essentially there are two principal rules to be borne in mind:
A. eliminate the sources of interference or reduce their effect
B. make the circuit itself insensitive to the remaining interference signals to the highest possible degree.

The latter rule is most important because:
- during design and development the future working circumstances are often not known,
- a complete suppression of interference is mostly not possible.

## A. SUMMARY OF POSSIBLE INTERFERENCE SOURCES AND COUNTER-MEASURES

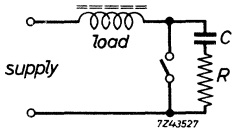
1. Spark extinction at switch contacts of motors and peak voltage suppression at inductive loads.

1.1 Bridging the contacts by means of a voltage-dependent resistor (VDR).



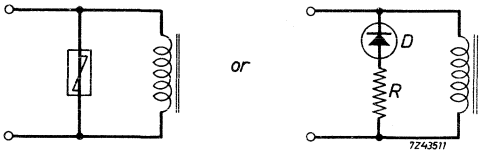

The peak voltage and the resulting arcing between the contacts will be reduced.

1.2 Bridging the contacts by means of a capacitor/resistor combination.




The capacitor reduces the voltage when the contact is opened. The resistor reduces the discharge current of the capacitor, when the contact is closed.

1.3 Bridging the load itself by a voltage dependent resistor or diode-resistor combination.




2. Dust on (or contamination of) the electro-magnetic power contacts.

A proper dust sealing solves this problem.

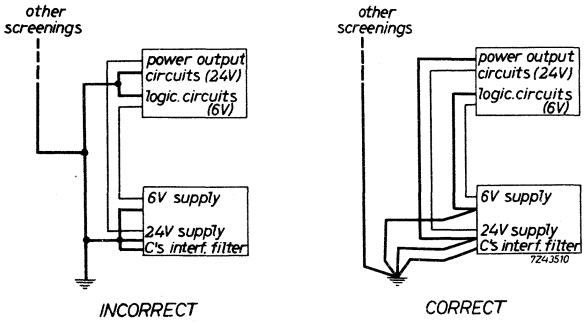
3. Incorrect positioning of possible interference sources.

Keep components and/or units which can act as interference sources, separated from the circuits that are sensitive to interference. Further improvements can be obtained by placing a metal shielding between these parts of the equipment.

4. Interference caused by improper wiring.

4.1 Wiring of earth lines

The principle is that the earth lines of the two supplies should be kept as far apart as possible. This holds in particular for the earth line of power transistors. The drive currents of these transistors, which are also sent through the earth lines, are rather high and can cause voltage differences.

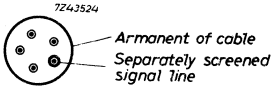



To reduce the chance of interference it is preferable to keep the length of earth lines as short as possible and to use wire of adequate diameter.
All earth lines must be connected separately to one common earth point on which also the chassis and other screenings are earthed.

4.2 Wiring that forms the connection to electro-magnetic loads, and leads that carry large currents, must be kept separated from the signal leads, which may transfer the interfering signals to the circuits that are sensitive to interference.

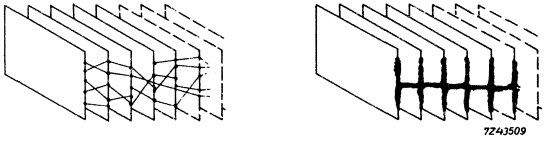
4.3 Signal carrying lines should be kept as short as possible and loops avoided. As screening material of these lines iron or steel must be used, a steel-armoured cable is very suitable for this purpose.

Furthermore it is preferable to screen signal lines, which are connected to triggered circuits, from other lines in this cable.




The earthing of the steel sheath as well as that of the separate line screening must be done at the common earth point of the chassis.

4.4 Decrease the wiring area
Example: wiring of a bank of printed-wiring connectors.

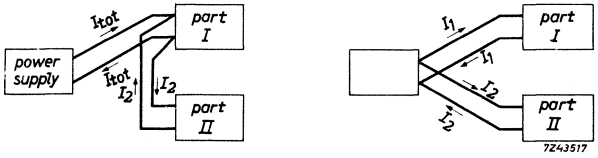



INCORRECT CORRECT

However, the wiring connected to inductive loads (drive lines for relays etc. or generally high pulse current lines) must be kept apart, with their own earth return.

5. Common impedance of two or more parts of an equipment.

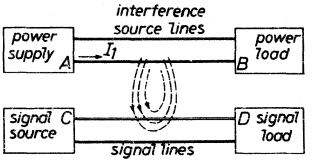
If, for instance, two parts of an equipment are connected to the same power supply, a reduction of the common impedance can be obtained by using separate supply lines.

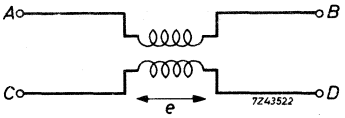



INCORRECT CORRECT

Further reduction can be achieved by using:
- a stabilised power supply (low internal impedance)
- separate power supplies for each part of the equipment.

6. Electro-magnetic coupling between signal and/or supply lines.

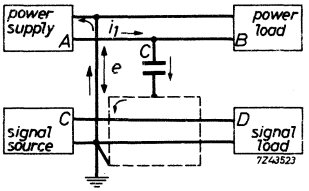



$$e = M\frac{di}{dt}$$

This coupling can be reduced by the following measures:
- reduce the magnetic field by twisting the interference source lines;
- cancel the induced voltage by twisting the signal lines;
- reduce the coupling magnetic field by increasing the distance between interference source lines A-B and signal C-D;
- reduce the coupled magnetic field by a shield of a ferromagnetic material;
- reduce the coupled magnetic field by decreasing the length of the interfering lines;
- choose circuit parameters in order to:
  decrease signal load impedance
  decrease magnitude and frequency of interfering currents;
- cancel the induced voltage by crossing the wires at right angles.

7. Electro-static coupling




$$i = C\frac{de}{dt}$$

This coupling can be reduced by the following measures:
- use an electrically conductive shield as shown in the figure. The capacitance C short-circuits the leakage current to earth, by-passing lead CD;
- increase the distance between the wires;
- decrease the dielectric constant of medium between wires;
- decrease the diameter of the conductors;
- decrease the length of the wires.

## B. MEASURES TO REDUCE OR ELIMINATE INDUCED INTERFERENCES

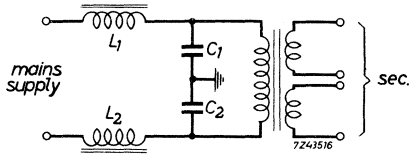
It should be noticed that induced interfering pulses may upset the functioning of systems by entering the logic circuits via:

1 the mains supply
2 induction on the low-voltage supply lines to the circuitry (included earth lines)
3 induction on lines which transmit the driving signals.

Generally, it is of great importance to place the transistor circuitry in a well-earthed metal case or frame. Metal sheet with a thickness of 1 mm will serve the purpose. The material must have a proper permeability to ensure sufficient magnetic screening, e.g. iron or steel (not aluminium).

Interference, which is introduced via the ways 1, 2 or 3 can be suppressed by:

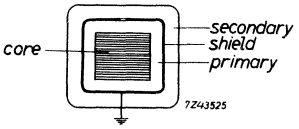
1.1 A filter in the primary of the mains transformer.



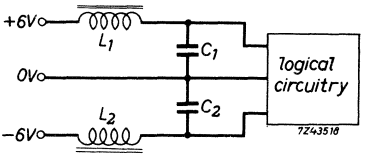

$L_1 = L_2 = 10$ mH
$C_1 = C_2 = 12$ kpf/700 V

When this is still inconclusive, a third capacitor can be connected in parallel with the primary of the transformer.

1.2 An electrostatic shield between primary and secondary of the mains transformer. This shield consists of a layer of copper foil which is connected to earth.



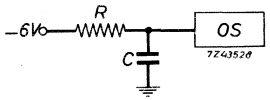

2.1 A filter in the low voltage supply lines of the logical circuitry.




$L_1 = L_2 = 510$ $\mu$H/0.5 $\Omega$
$C_1 = C_2 = 100$ $\mu$F

Care should be taken that only the low-level logical circuits are supplied via this filter, as otherwise the current variations will become excessive.

2.2 It is sometimes necessary to use an extra filter in the −6 V supply line close to the circuits, that are sensitive to interference, e.g. the one-shot multivibrator OS.

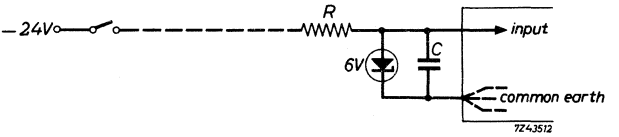


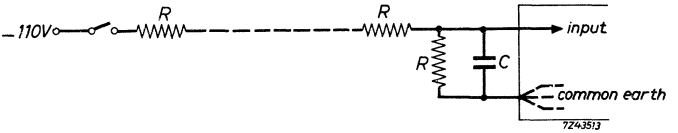

R = 47 Ω
C = 100 μF

3. If signals are to be transmitted from one part of the equipment to another the following rules must be observed:
   - improve the signal-to-noise (interference) level on the line by raising the voltage level of the signal;
   - apply low-pass filters at all equipment inputs, cutting off signals of a frequency higher than the maximum signal frequency;
   - prefer "level" (d.c.) signal transmission to pulse transmission (interference is often intermittent and of short duration).

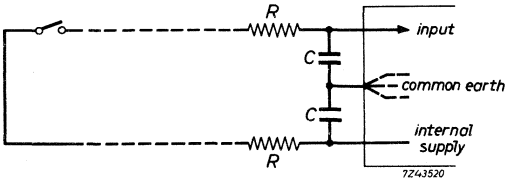
   A few circuits are given below:

3.1 Electro-mechanical contact, external supply:



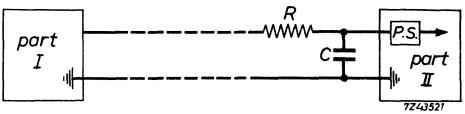




3.2 External contact, supply from the equipment:




Note: apply this filtering particularly when the supply, common to the transistor circuits, is used for the line as well. Choose the resistors such that overloading the power supply or transistorized circuitry at short-circuit conditions of the line is avoided.

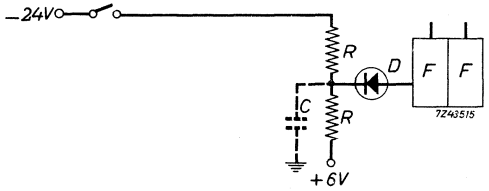
3.3 Transmission of lower-speed timing signals between equipment parts:



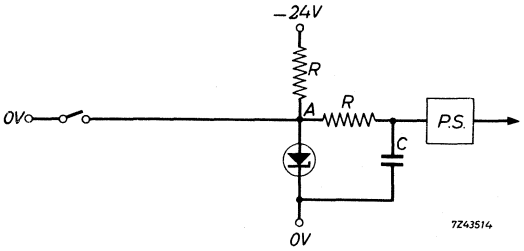

After the RC-network has been passed, the signal form is restored by a pulse shaper.
Note the delay in pulse transmission caused by the RC-network.

3.4 Remote setting of a flip-flop from a negative voltage source.

When the switch is open, the diode is non-conducting, because of the +6 V threshold voltage.
The diode remains blocked for positive interference pulses, whereas for negative pulses to become effective the amplitude must be at least comparable with the threshold voltage.

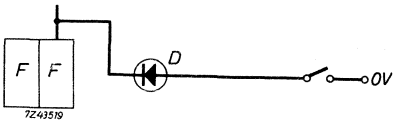



3.5 An almost similar effect can be obtained with the following circuit, intended for driving pulse shapers or inverters.




The voltage at point A will be −6 V when the switch is open. Negative interference pulses will not influence the state of the pulse shaper; positive pulses are short-circuited by the conducting Zener diode. When the switch is closed, point A will become 0 V, so that the pulse shaper is caused to change its state.

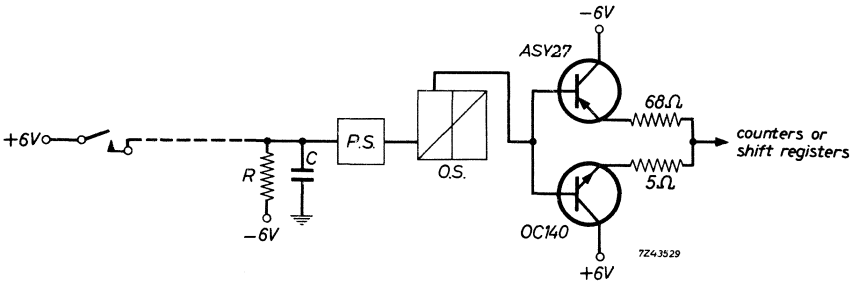
3.6 Remote setting of a flip-flop from a voltage of 0 V.




By closing the switch, the flip-flop is forced to change its state. This method has the advantage, that switch and line are not connected to the sensitive, high-impedance base input.

3.7 Avoidance of contact bouncing

When a shift register or counter must be operated by an electro-mechanical contact, it is essential that the contact bouncing should be avoided. This can be done by means of a one-shot multivibrator of which the pulse has the required characteristics.
To reduce the time in which interference can be induced (switch open) a break contact is used. The one-shot multivibrator operates every time the switch is opened.



# LOADING TABLE

If not indicated separately the N and P terminal(s) of each unit are connected to $V_N$ respectively $V_P$. ($V_N$ = −6 V ±5 %, $V_P$ = +6 V ±5 %.)

| preceding unit or preceding chain of units | | driving unit | | via | maximum number of driven units | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | FF1 | | FF2 | | | FF3 | | |
| | | type | out-put | | W | A | W | A | G | W | A1 or A2 | A1 + A2 |
| | | FF1 | Q | | 1[1] | 4[9] | 1[1] | 4[9] | 2[10] | 1[1] | 2[10] | 2[10] |
| | | FF2 | Q | | 1[1] | 1[10] | 1[1] | 1[10] | 2[10] | 1[1] | 1[10] | 1[10] |
| | | FF3 | Q | | 1[1] | 5[9] | 1[1] | 5[9] | 2[10] | 1[1] | 3[10] | 3[10] |
| | | FF4 | Q | | 1[1] | 5[9] | 1[1] | 5[9] | 2[10] | 1[1] | 3[10] | 3[10] |
| | IA1 | N1 | Q | | 0 | 4[4])3] | 0 | 4[4])3] | 0 | 0 | 2[3] | 1[3] |
| | FF1[10] OS1[b] | | | | 0 | 4[4] | 0 | 4[4] | 0 | 0 | 2 | 1 |
| PS1 | IA2 | | | | | | | | | | | |
| | FF2[10] | | | | 0 | 1[4] | 0 | 1[4] | 0 | 0 | 1 | 1 |
| | PS1 | | | | 0 | 2[4] | 0 | 2[4] | 0 | 0 | 1 | 0 |
| | FF3[10] FF4[10] | | | | 0 | 5[4] | 0 | 5[4] | 0 | 0 | 3 | 2 |
| | OS2[d] | | | | 0 | 6 | 0 | 6 | 0 | 0 | 6 | 5 |
| | OS2[e] | | | | 0 | 5 | 0 | 5 | 0 | 0 | 5 | 3 |
| | N1 | P1 | Q | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | EF1 | Q | | 4[1] | | 4[1] | | 0 | 3[1] | 0 | 0 |
| | | | T | | 1[6] | | 1[6] | | 0 | 1[6] | 0 | 0 |
| | | IA1 | Q | | 2[1] | 4[3] | 2[1] | 4[3] | 3 | 2[1] | 2[3] 3[3])7] | 2[3] 3[3])7] |
| | N1 | EF2 | Q | ASY27[c] | 2[1] | 4 | 2[1] | 4 | 3 | 1[1] | 2 | 2 |
| N1 | P1 | | | ASY27[c] | 2[1] | 4 | 2[1] | 4 | 3 | 1[1] | 2 | 2 |
| | N1 | | R | | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 0 |
| N1 | P1 | | | | | | | | | | | |
| | N1[5] | IA2 | Q | | 2[1] | 0 | 2[1] | 0 | 0 | 2[1] | 0 | 0 |
| N1 | P1[8] | | | | | | | | | | | |
| | IA1 IA2 | | | | 2[1] | 4 | 2[1] | 4 | 3 | 2[1] | 4 5[7] | 4 5[7] |
| | PS1 | | | | 2[1] | 4 | 2[1] | 4 | 3 | 2[1] | 2 3[7] | 2 3[7] |
| | OS2[d] | | | | | | | | | | | |
| | N1[5] | IA2[a] | Q | | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| N1 | P1[8] | | | | | | | | | | | |
| | | PS1 | Q | | 0 | 2 | 0 | 2 | 2 | 0 | 1 | 1 |
| | | OS1 | Q1 | | 2[1] | 4 | 2[1] | 4 | 3 | 2[1] | 2 | 1 |
| | | | Q2 | | 1[1] | 0 | 1[1] | 0 | | 0 | 0 | 0 |
| | | OS2 | Q1 | | 1[1] | 6 | 1[1] | 6 | 6 | 1[1] | 6 | 5 |
| | | | Q2 | | 0 | 5 | 0 | 5 | 2 | 0 | 5 | 3 |
| | | PD1 | Q | | 0 | 20 | 0 | 20 | 0 | 0 | 22 | 20 |
| | | GI1 | Q | | 0 | 1 | 0 | 1 | 6 | 0 | 2 | 2 |
| | GI1 | GI1[f] | Q | | 0 | 4[13] | 0 | 4[13] | 19 | 0 | 6 | 6 |
| AND-AND AND-OR | GI1 | GI1 | Q | | 0 | 4[13] | 0 | 4[13] | 11 | 0 | 5 | 5 |

| maximum number of driven units | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| FF4 | | | N1 | EF1 | IA1 | EF2 | IA2 | PS1 | OS1 | OS2 | PA1 | PD1 | | GI1 |
| W | A | G | W | W | W | W | W | W | A2 | A | W | A | G | G |
| 1[1] | 2[10] | 2[10] | 5 | 1 | 1 | 2 | 0 | 6[9]2) | 4[9] | 2[10] | 1 | 1[10] | 1[10] | 2[10] |
| 1[1] | 1[10] | 2[10] | 5 | 1 | 1 | 2 | 0 | 2[10]2) | 1[10] | 2[10] | 1 | 1[10] | 1[10] | 2[10] |
| 1[1] | 3[10] | 3[10] | 12 | 1 | 1 | 2 | 0 | 7[9]2) | 5[9] | 4[10] | 2 | 3[10] | 3[10] | 4[10] |
| 1[1] | 3[10] | 3[10] | 12 | 1 | 1 | 2 | 0 | 7[9]2) | 5[9] | 4[10] | 2 | 3[10] | 3[10] | 4[10] |
| 0 | 1[3] | 0 | 0 | 0 | 0 | 1 | 1[5] | 1 | 4[4]3) | 1[3] | 0 | 1[3] | 0 | |
| 0 | 1 | 0 | 0 | 0 | 0 | 1 | 1[5] | 1 | 4[4] | 2 | 0 | 2 | 0 | |
| 0 | 1 | 0 | 0 | 0 | 0 | 1 | 1[5] | 1 | 1[4] | 1 | 0 | 1 | 0 | |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1[5] | 1 | 2[4] | 0 | 0 | 0 | 0 | |
| 0 | 2 | 0 | 0 | 0 | 0 | 1 | 1[5] | 1 | 5[4] | 3 | 0 | 3 | 0 | |
| 0 | 5 | 0 | 0 | 0 | 0 | 1 | 1[5] | 1 | 8 | 12 | 0 | 10 | 0 | |
| 0 | 3 | 0 | 0 | 0 | 0 | 1 | 1[5] | 1 | 6 | 4 | 0 | 3 | 0 | |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1[8] | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| 3[1] | 0 | 0 | 4 | | 4 | | 0 | 18[2] | | 0 | 0 | 0 | 0 | 0 |
| 1[6] | 0 | 0 | | | 0 | | 1 | 0 | | 0 | 0 | 0 | 0 | 0 |
| 2[1] | 2[3] 3[3]7) | 2 | 7 16[7] | 2 | 2 | 5 | 1 | 8[2] | 4[3] | 4[3] 7[3]7) | 1 | 2[3] | 2 | |
| 1[1] | 2 | 10 | 50 | 2 | 2 | 5 | 1 | 8[2] | 4 | 4 | 1 | 4 | 6 | |
| 1[1] | 2 | 10 | 27 | 2 | 2 | 5 | 1 | 8[2] | 4 | 4 | 1 | 4 | 6 | |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| 2[1] | 0 | 0 | 0 | 2 | 2 | 5 | 1 | 8[2] | 0 | 0 | 0 | 0 | 0 | |
| 2[1] | 4 5[7]) | 10 | 60 | 2 | 2 | 5 | 1 | 8[2] | 6 | 7 9[7]) | 10 | 7 9[7]) | 8 | |
| 2[1] | 2 3[7]) | 10 | 60 | 2 | 2 | 5 | 1 | 8[2] | 4 | 3 6[7]) | 6 | 3 6[7]) | 4 | |
| 0 | 0 | 2 | 6 9[7]) | 1 | 1 | 1 | 1 | 4[2] | 0 | 0 | 1 | 0 | 2 3[7]) | |
| 0 | 1 | 1 | 2 | 1 | 1 | 2 | 1 | 6[2] | 2 | 1 | 0 | 1 | 1 | 1 |
| 2[1] | 1 | 1 | 3 | 2 | 2 | 5 | 0 | 8[2] | 4 | 1 | 0 | 1 | 1 | 2 |
| 0 | 0 | 0 | 0 | 1 | 1 | 2 | 0 | 3[2] | 0 | 0 | 0 | 0 | 0 | 0 |
| 1[1] | 5 | 10 | 12 | 1 | 1 | 2 | 1 | 6[2] | 6 | 13 | 7 | 10 | 10 | 8 |
| 0 | 3 | 3 | 4 | 1 | 0 | 1 | 0 | 3[2] | 5 | 4 | 2 | 3 | 3 | 6 |
| 0 | 20 | 0 | 10 75[11]) | 0 | 25[12]) | 0 | 0 | 0 | 20 | 50 | 0 | 38 | 0 | 30 |
| 0 | 2 | 5 | 6 | | | | | 4[2] | 1 | 6 | 6 | 6 | 7 | 3 |
| 0 | 6 | 19 | 19 | | | | | 7[2]) | 4[13]) | 19 | 16 | 18 | 19 | 9 |
| 0 | 5 | 11 | 11 | | | | | 7[2]) | 4[13]) | 11 | 10 | 11 | 11 | 7 |

Notes:

P1 Unless specified otherwise a P1 may be interposed between two units without great influence upon the loadibility. AC inputs of FF1, FF2, FF3, FF4, OS1 and OS2 cannot be driven from it.

2PL1 The 2PL1 is normally used in conjunction with FF1 or FF2. In this case the input data are equivalent to those of the similar FF2 inputs. The output terminals are directly connected to the d.c. input terminals of the FF1 or FF2.

2PL2 Ditto for FF3 and FF4.

a) IA2 with only terminals N1 or N2 connected to $V_N$.
b) OS1 Q1 output only.
c) ASY27 common emitter stage with 1 kΩ collector resistor.
d) OS2 Q1 output only.
e) OS2 Q2 output only.
f) Used as NON-INVERTING AMPLIFIER.

 not recommended.

1. Each via a 4.7 kΩ ±5 % resistor in series with a separating diode OA200, anode to driven unit.
2. Each via a 12 kΩ ±5 % resistor, bypassed by a 330 pF capacitor.
3. Only if the chain of units indicated is driven by a FF1, FF2, FF3, FF4, PS1 or the Q1 terminal of an OS1 or OS2.
4. The maximum speed of operation is
$$\frac{30 \text{ kHz}}{\text{number of units driven by the N1 gate}}$$
5. Via a diode OA200, cathode to N1, anode to IA2, and bypassed by a 1500 pF capacitor.
6. Via a separating diode OA85, cathode to driven unit.
7. Only if the N-terminals of the driving unit are floating.
8. The P-terminal of the P1 gate is floating.
9. Total number for both Q-outputs together.
10. Total number per Q-output.
11. Only with a 390 Ω ±5 % resistance between the terminals Q and N of the driving unit PD1.
12. For each a resistance of 2.7 kΩ ±5 % between the terminals Q and N of the driving unit PD1.
13. Only with a 1.3 kΩ ±5 % resistance between the terminals Q and N of the driving unit.

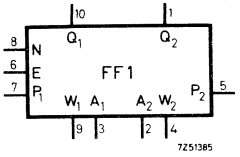
# FLIP-FLOP

Colour: red

The unit FF1 contains a transistor bi-stable multivibrator circuit. The transistors are medium-speed switching types.

The circuit constitutes a memory function when driven by means of a d.c. level or a positive-going voltage step (a.c. input signal), and it can also be used as a binary scale-of-two with a positive-going input signal.

| | |
|---|---|
| Pulse repetition frequency range: | 0–100 kHz |
| Ambient temperature range: | -20 to +60 °C |
| Weight: | approx. 20 g |

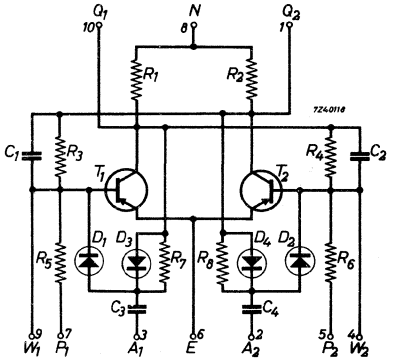



Drawing symbol

CIRCUIT DATA

Terminal

1 = $Q_2$ = output 2
2 = $A_2$ = a.c. input 2
3 = $A_1$ = a.c. input 1
4 = $W_2$ = d.c. input 2
5 = $P_2$ = supply +6V(2)
6 = E = common supply 0V
7 = $P_1$ = supply +6V(1)
8 = N = supply -6V
9 = $W_1$ = d.c. input 1
10 = $Q_1$ = output 1




Power Supply

Terminal 5: $V_{P2}$ = +6V ± 10%, $I_{P2}$ = 0.15mA [1] ) Nominal
6: $V_E$ = 0V common ) value
7: $V_{P1}$ = +6V ± 10%, $I_{P1}$ = 0.15mA [1] ) of the
8: $V_N$ = -6V ± 10%, $-I_N$ = 7mA [1] ) current

[1]) The sign is positive when the current flows towards the circuit.

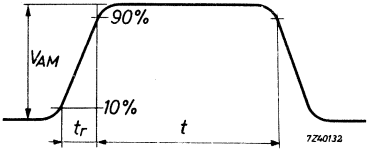
INPUT DATA

Input Signal Requirements [2])

AC Input Signal (A terminals)

A positive-going voltage step is applied to terminal $A_1$ or $A_2$, or to both terminals interconnected in the case of binary scale-of-two applications. This voltage step drives the transistor $T_1$ ($T_2$) into the non-conducting state.

| | | |
|---|---|---|
| Voltage | $V_{AM}$ | = min. $-0.66V_N$ |
| | | = max. $-V_N$ |
| Rise time | $t_r$ | = max. 0.4 µs |
| Length of driving pulse | t | = min. 0.5 µs |
| Input noise level | | = max. 1 V peak to peak |




DC Input Signals (W terminals)

A d.c. voltage level is applied to terminal $W_1$ or $W_2$. A positive voltage drives the transistor $T_1$ ($T_2$) into the non-conducting state and a negative voltage drives it into the conducting state.

Transistor conducting (output level "negative low")

| | | |
|---|---|---|
| Current | $-I_W$ | = min. 0.5 mA [1]) ($-V_W$ = max. 0.35 V) |
| limiting value | | = max. 10 mA [1]) |

[1]) The sign is positive when the current flows towards the circuit

[2]) These data apply to the most adverse working condition for a combination of units, namely to supply voltages $V_N$ = -5.4 V and $V_P$ = +6.6 V. Unless differently specified all the voltage and current figures quoted represent absolute maximum values.

Transistor non-conducting (output level "negative high")

Voltage $V_W$ = min. 0.2V
limiting value = max. 10V
Current $I_W$ = min. 1mA [1])
($I_W$ = appr. 1.1mA [1]) at $V_W$ = 6V)

Input Impedance

Equivalent to a capacitance of approximately 500pF ($A_1$, $A_2$ terminal or both terminals interconnected).

OUTPUT DATA

Output Signal Characteristics [2])

Transistor conducting (output level "negative low")

Voltage $-V_Q$ = max. 0.2V
Load current $-I_Q$ = max. 2.5mA [1])

Transistor non-conducting (output level "negative high")

Voltage $-V_Q$ = min. $-0.7V_N$ [1])
Load current $I_Q$ = max. 0.7mA

Load currents of equal sign, up to the values given as maxima can be drawn from the two output terminals simultaneously. In the case of simultaneous load currents of opposite sign, the maximum load currents given are not guaranteed.

Maximum Capacitive Load (2000pF for both Q-outputs together)

When the maximum capacitive and resistive loads are applied in parallel, the maximum pulse repetition frequency is not guaranteed.

Output Impedance

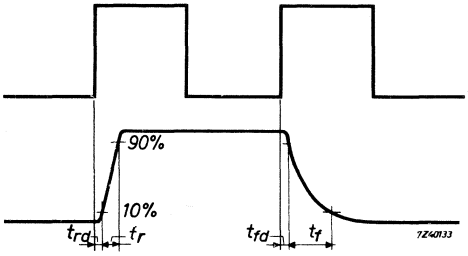
Equivalent to a resistance of approx.

$R_i$ = 50Ω for positive-going output voltage
$R_i$ = 1000Ω for negative-going output voltage

1) See note 1 on previous page
2) See note 2 on previous page

Switching and Delay Times (for orientation only)

A square wave input signal (A terminals) is assumed with an amplitude of min. $-0.7V_N$.




Unit Unloaded

| | | |
|---|---|---|
| Rise delay | $t_{rd}$ | = max. 0.8 µs |
| Rise time | $t_r$ | = max. 0.3 µs |
| Fall delay | $t_{fd}$ | = max. 0.6 µs |
| Fall time | $t_f$ | = max. 2 µs |

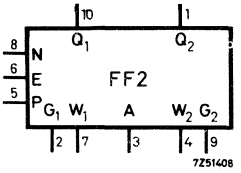
# FLIP-FLOP

Colour: red

The unit FF2 contains a transistor bi-stable multivibrator circuit. The transistors are medium-speed switching types.

The circuit constitutes a memory function when driven by means of a d.c. level or a positive-going voltage step (a.c. input signal). In the case of a.c. drive, the switching of the flip-flop can be controlled by a d.c. level supplied to the built-in gate circuits (e.g. in shift registers).

| | |
|---|---|
| Pulse repetition frequency range: | 0–100 kHz |
| Ambient temperature range: | −20 to +60 °C |
| Weight: | approx. 20 g |

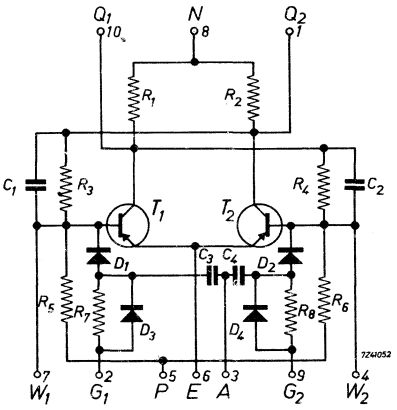



Drawing symbol

## CIRCUIT DATA

Terminal

1 = $Q_2$ = output 2
2 = $G_1$ = gate input 1
3 = A = a.c. input
4 = $W_2$ = d.c. input 2
5 = P = supply +6V
6 = E = common supply 0V
7 = $W_1$ = d.c. input 1
8 = N = supply −6V
9 = $G_2$ = gate input 2
10 = $Q_1$ = output 1




Power Supply

Terminal 5: $V_P$ = +6V ± 10%, $I_P$ = 0.3mA [1])
6: $V_E$ = 0V common
8: $V_N$ = −6V ± 10%, $-I_N$ = 7mA [1])

} Nominal value of the current

[1]) The sign is positive when the current flows towards the circuit.

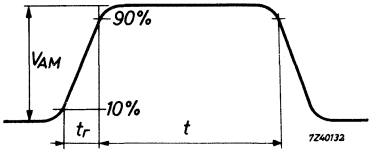
INPUT DATA

Input Signal Requirements [2])

AC Input Signal (A terminal)

A positive-going voltage step is applied to terminal A. This voltage step drives the transistor $T_1$ ($T_2$) into the non-conducting state if the corresponding gate has been opened by a proper d.c. gate input signal on terminal $G_1$ ($G_2$)

| | | | |
|---|---|---|---|
| Voltage | $V_{AM}$ | = min. | $-0.66 V_N$ |
| | | = max. | $- V_N$ |
| Rise time | $t_r$ | = max. | 0.4 µs |
| Length of driving pulse | t | = min. | 0.5 µs |
| Input noise level | | = max. | 1 V peak to peak |




DC Input Signal (W terminals)

A d.c. voltage level is applied to terminal $W_1$ or $W_2$. A positive voltage drives the transistor $T_1$ ($T_2$) into the non-conducting state and a negative voltage drives it into the conducting state.

Transistor conducting (output level "negative low")

| | | | |
|---|---|---|---|
| Current | $-I_W$ | = min. | 0.5 mA [1]) ($-V_W$ = max. 0.35 V) |
| limiting value | | = max. | 10 mA [1]) |

Transistor non-conducting (output level "negative high")

| | | | |
|---|---|---|---|
| Voltage | $V_W$ | = min. | 0.2 V |
| limiting value | | = max. | 10 V |
| Current | $I_W$ | = min. | 1 mA [1]) |
| | ($I_W$ | = appr. | 1.1 mA [1]) at $V_W$ = 6 V) |

[1]) The sign is positive when the current flows towards the circuit

[2]) These data apply to the most adverse working condition for a combination of units, namely to supply voltages $V_N$ = -5.4 V and $V_P$ = +6.6 V. Unless differently specified, all the voltage and current figures represent absolute maximum values.

Gate Input Signal (G terminals)

A d.c. voltage level is applied to terminal $G_1$ ($G_2$). Transistor $T_1$ ($T_2$) is driven into the non-conducting state by the a.c. input signal (A terminal) if the corresponding gate input $G_1$ ($G_2$) is at "negative low" level (i.e. gate open).

Note 1. The $G_1$ and $G_2$ input levels should not be "negative low" simultaneously.
2. The $G_1$ and $G_2$ input levels have to be present 8 µs before the arrival of the a.c. input signal

Gate Open (input level "negative low")

Voltage $-V_G$ = max. 0.2V
= min. 0V

Gate closed (input level "negative high")

Voltage $-V_G$ = min. $V_{AM}$ ($V_{AM}$ = amplitude of a.c. input signal)
= max. $-V_N$

Input Impedance

Equivalent to a capacitance of approx. 500 pF (A terminal)

OUTPUT DATA

Output Signal Characteristics [2])

Transistor conducting (output level "negative low")

Voltage $-V_Q$ = max. 0.2V
Load current $-I_Q$ = max. 2.5mA [1])

Transistor non-conducting (output level "negative high")

Voltage $-V_Q$ = min. $-0.7V_N$
Load current $I_Q$ = max. 0.7mA [1])

Load currents of equal sign, up to the values given as maxima, can be drawn from the two output terminals simultaneously. In the case of simultaneous load currents of opposite sign, the maximum load currents given are not guaranteed.

[1]) See note 1 on previous page

[2]) See note 2 on previous page

Maximum Capacitive Load ( 500 pF for each Q-output)

When the maximum capacitive and resistive loads are applied in parallel, the given maximum pulse repetition frequency is not guaranteed.

Output Impedance

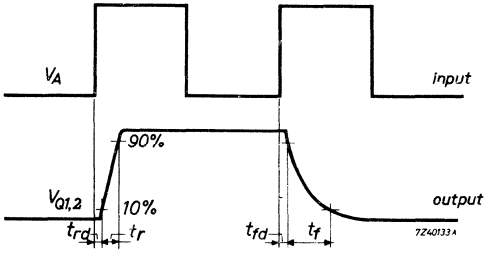
Equivalent to a resistance of approx.

$R_i$ = 50 Ω for positive-going output voltage

$R_i$ = 1000 Ω for negative-going output voltage

Switching and Delay Times (for orientation only)

A square wave input signal (A terminals) is assumed with an amplitude of min. $-0.7V_N$.




Unit Unloaded

| | | |
|---|---|---|
| Rise delay | $t_{rd}$ | = max. 0.8 µs |
| Rise time | $t_r$ | = max. 0.3 µs |
| Fall delay | $t_{fd}$ | = max. 0.6 µs |
| Fall time | $t_f$ | = max. 2 µs |

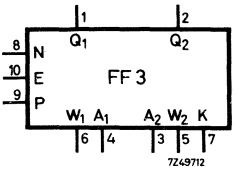
# FLIP-FLOP

Colour: red

The unit FF3 contains a transistor bi-stable multivibrator circuit. The transistors are medium-speed switching types.

The circuit constitutes a memory function when driven by means of a d.c. level or a positive-going trigger signal, and it can also be used as a binary scale-of-two when the trigger inputs are interconnected.

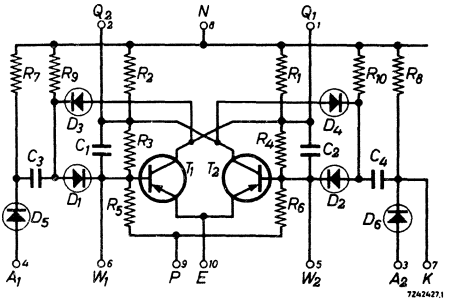
| | | |
|---|---|---|
| Frequency range | : | 0 - 100 kHz |
| Ambient temperature range: | | -20 to +60 °C |
| Weight | : | approx. 20 g |




Drawing symbol

## CIRCUIT DATA

Terminal




1 = $Q_1$ = output 1

2 = $Q_2$ = output 2

3 = $A_2$ = trigger input 2

4 = $A_1$ = trigger input 1

5 = $W_2$ = d.c. input 2

6 = $W_1$ = d.c. input 1

7 = K = terminal for external trigger input

8 = N = supply -6 V

9 = P = supply +6 V

10 = E = common supply 0 V

Power Supply

Terminal 8 : $V_N$ = -6 V ± 5 %, $-I_N$ = 8.8 mA } Nominal value

9 : $V_P$ = 6 V ± 5 %, $I_P$ = 0.6 mA } of the current

10 : $V_E$ = 0 V common

Notes

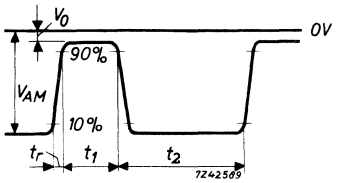
- The data given apply to the most adverse supply voltages for a combination of units, namely $V_N$=-5.7 V and $V_P$=6.3 V.
- The temperatures -20 °C and +60 °C, and the tolerances on the supply voltages are absolute limiting values.
- When a current is flowing towards the unit, the positive sign is used.

## INPUT DATA

### Input Signal Requirements

Trigger Input Signal (A terminals)

A positive-going voltage step is applied to terminal $A_1$ or $A_2$, or to both terminals interconnected in the case of binary scale-of-two applications. This voltage step drives the transistor $T_1$ ($T_2$) into the non-conducting state.
To terminal K external diodes can be connected (in the same sense as diode $D_6$) to provide the pulse-gate, corresponding with terminal $A_2$, with extra trigger inputs or condition inputs.




Voltage

| | | | | |
|---|---|---|---|---|
| $V_{AM}$ | = | min. | -0.7 | $V_N$ |
| | = | max. | - | $V_N$ |
| $-V_o$ | = | min. | 0 | V |
| | = | max. | 0.2 | V |

| | | $A_1$ or $A_2$ | $A_1$ and $A_2$ interconnected |
|---|---|---|---|
| Required direct current | $I_{AD}$ = | min. 0.88 mA | min. 1.75 mA |
| Required current during the transient averaged over: 0.4 µs | $I_{AT}$ = | min. 5 mA | min. 6 mA |
| 0.7 µs | = | min. 4 mA | min. 4.5 mA |

| | | | | |
|---|---|---|---|---|
| Rise time | $t_r$ | = | max. | 0.7 μs |
| Pulse duration | $t_1$ | = | min. | 1 μs |
| | $t_2$ | = | min. | 8 μs |
| Input noise level | $V_n$ | = | max. | 1 V peak to peak |

DC Input Signal (W terminals)

A d.c. voltage level is applied to terminal $W_1$ or $W_2$. A positive voltage drives the transistor $T_1$ ($T_2$) into the non-conducting state and a negative voltage drives it into the conducting state

| | | | | |
|---|---|---|---|---|
| Transistor conducting | | | | |
| Current | $-I_W$ | = | min. | 0.6 mA ($-V_W$ = max. 0.4 V) |
| limiting value | | = | max. | 15 mA |
| Transistor non-conducting | | | | |
| Voltage | $V_W$ | = | min. | 0.2 V |
| limiting value | | = | max. | 10 V |
| Current | $I_W$ | = | min. | 0.9 mA |

OUTPUT DATA

Voltages and currents

Transistor conducting

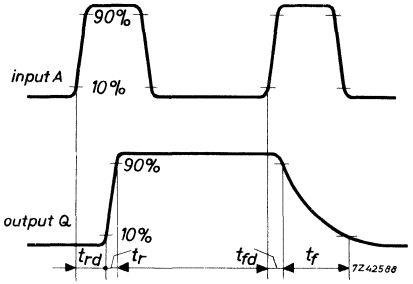
| | | | | |
|---|---|---|---|---|
| Voltage | $-V_Q$ | = | max. | 0.2 V |
| Available direct current | $-I_{QD}$ | = | max. | 6 mA |
| Available current during the transient | | | | |
| averaged over: 0.4 μs | $-I_{QT}$ | = | max. | 11 mA |
| 0.7 μs | | = | max. | 14 mA |

Transistor non-conducting

| | | | | |
|---|---|---|---|---|
| Voltage | $-V_Q$ | = | min. | -0.7 $V_N$ |
| Available direct current | $I_{QD}$ | = | max. | 0.7 mA |

## Switching and delay times

These data are for orientation only and refer to an input signal as specified under INPUT DATA.




| | Unit unloaded | Unit max. loaded |
|---|---|---|
| Rise delay | $t_{rd}$ = max. 1.0 µs | max. 1.1 µs |
| Rise time | $t_r$ = max. 0.3 µs | max. 0.7 µs |
| Fall delay | $t_{fd}$ = max. 0.8 µs | max. 0.8 µs |
| Fall time | $t_f$ = max. 1.7 µs | max. 1.7 µs |

# FLIP-FLOP

Colour: red

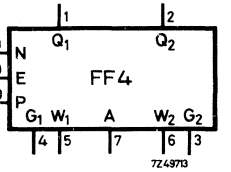
The unit FF4 contains a transistor bi-stable multivibrator circuit. The transistors are medium-speed switching types.

The circuit constitutes a memory function when driven by means of a d.c. level or a positive-going trigger signal. In the case of trigger drive, the switching of the flip-flop can be controlled by a d.c. level applied to the built-in gate circuits (e.g. in shift registers).

Frequency range : see INPUT DATA

Ambient temperature range : -20 to +60 °C

Weight : approx. 20 g




Drawing symbol

CIRCUIT DATA

Terminal

1 = $Q_1$ = output 1

2 = $Q_2$ = output 2

3 = $G_2$ = gate input 2

4 = $G_1$ = gate input 1

5 = $W_1$ = d.c. input 1

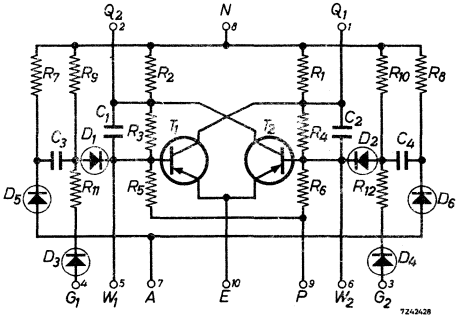
6 = $W_2$ = d.c. input 2

7 = A = trigger input

8 = N = supply -6 V

9 = P = supply +6 V

10 = E = common supply 0 V




Power Supply

Terminal 8 : $V_N$ = -6 V ± 5 %, $-I_N$ = 8.8 mA } Nominal value

9 : $V_P$ = +6 V ± 5 %, $I_P$ = 0.6 mA } of the current

10 : $V_E$ = 0 V common

Notes

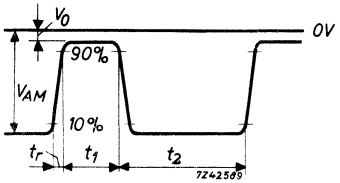
- The data given apply to the most adverse supply voltages for a combination of units, namely $V_N = -5.7$ V and $V_p = 6.3$ V.
- The temperatures -20 °C and +60 °C, and the tolerances on the supply voltages are absolute limiting values.
- When a current is flowing towards the unit, the positive sign is used.

## INPUT DATA

### Input Signal Requirements

Trigger Input Signal (A terminal)

A positive-going voltage step is applied to terminal A. This voltage step drives the transistor $T_1(T_2)$ into the non-conducting state if the corresponding gate has been opened by an appropriate gate input signal on terminal $G_1(G_2)$.




| | | | | | |
|---|---|---|---|---|---|
| Voltage | $V_{AM}$ | = | min. | -0.7 | $V_N$ |
| | | | max. | - | $V_N$ |
| | $-V_o$ | = | min. | 0 | V |
| | | | max. | 0.2 | V |
| Required direct current | $I_{AD}$ | = | min. | 1.75 | mA |
| Required current during the transient | | | | | |
| averaged over: 0.4 µs | $I_{AT}$ | = | min. | 6 | mA |
| 0.7 µs | | | min. | 4.5 | mA |
| Rise time | $t_r$ | = | max. | 0.7 | µs |
| Pulse duration | $t_1$ | = | min. | 3 | µs |
| | $t_2$ | = | min. | 11 | µs |
| Input noise level | $V_n$ | = | max. | 1 V peak to peak | |

DC Input signal (W terminals)

A d.c. voltage level is applied to terminal $W_1$ or $W_2$. A positive voltage drives the transistor $T_1(T_2)$ into the non-conducting state and a negative voltage drives it into the conducting state.

| | | |
|---|---|---|
| Transistor conducting | | |
| Current | $-I_W$ = min. 0.6 mA | ($-V_W$ = max. 0.4 V) |
| limiting value | = max. 15 mA | |
| Transistor non-conducting | | |
| Voltage | $V_W$ = min. 0.2 V | |
| limiting value | = max. 10 V | |
| Current | $I_W$ = min. 0.9 mA | |

Gate Input Signal (G terminals)

A d.c. voltage level is applied to terminal $G_1(G_2)$. Transistor $T_1(T_2)$ is driven into the non-conducting state by the trigger input signal (A terminal) if the corresponding gate is opened by an appropriate gate input signal.

| | | gate open | gate closed |
|---|---|---|---|
| Voltage | $-V_G$ | = min. 0 V | min. $V_{AM}$ |
| | | max. 0.2 V | max. - $V_N$ |
| Required gate current caused by negative transient of $V_{AM}$ | $I_{GD}$ | = min. 1.75 mA | min. 1.2 mA |

| | | to open gate | to close gate |
|---|---|---|---|
| Required average current during the positive transient of $V_G$ | $I_{GT}$ | = min. 1.6 mA | – |
| Gate setting time | | | |
| when the gate input level changes at random: | $t_{GS}$ | = min. 17 µs | min. 25 µs |
| when the gate input level changes within 2 µs after the positive going edge of the trigger signal: | $t_{GS}$ | = min. 11 µs | min. 11 µs |

Note: The latter applies to a shift register configuration so that the max. shift frequency is approximately 70 kHz.

During triggering the G levels should not be at zero voltage level simultaneously.

The gate setting time is the required waiting time between the last G level change and the potitive going edge of the trigger pulse.

OUTPUT DATA

Voltages and currents

Transistor conducting

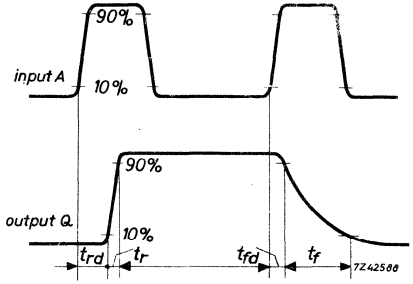
| | | | | |
|---|---|---|---|---|
| Voltage | $-V_Q$ | = max. | 0.2 | V |
| Available direct current | $-I_{QD}$ | = max. | 6 | mA |
| Available current during the transient | | | | |
| averaged over: 0.4 µs | $-I_{QT}$ | = max. | 11 | mA |
| 0.7 µs | | = max. | 14 | mA |

Transistor non-conducting

| | | | | |
|---|---|---|---|---|
| Voltage | $-V_Q$ | = min. | -0.7 | $V_N$ |
| Available direct current | $I_{QD}$ | = max. | 0.7 | mA |

Switching and delay times

These data are for orientation only and refer to an input signal as specified under INPUT DATA.




| | | Unit unloaded | | Unit max. loaded | |
|---|---|---|---|---|---|
| Rise delay | $t_{rd}$ | = max. 1.0 | µs | max. 1.1 | µs |
| Rise time | $t_r$ | = max. 0.3 | µs | max. 0.7 | µs |
| Fall delay | $t_{fd}$ | = max. 0.8 | µs | max. 0.8 | µs |
| Fall time | $t_f$ | = max. 1.7 | µs | max. 1.7 | µs |

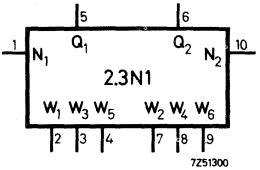
# DUAL NEGATIVE GATE

Colour: orange

The unit 2.3N1 contains two three-input germanium-diode gates, that perform an AND logical operation on negative input-voltage signals.

The two gate circuits are identical and can be used separately or combined into a multiple-input gate by interconnecting the output terminals $Q_1$ and $Q_2$. In this latter case only one negative supply terminal should be used.

| | |
|---|---|
| Pulse repetition frequency range: | 0-100 kHz |
| Ambient temperature range: | -20 to +60 °C |
| Weight: | approx. 20 g |

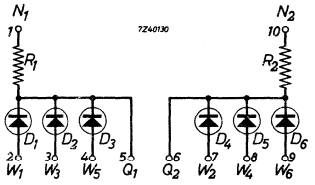



Drawing symbol

CIRCUIT DATA

Terminal

1 = $N_1$ = supply -6 V (1)
2 = $W_1$ = input 1
3 = $W_3$ = input 3
4 = $W_5$ = input 5
5 = $Q_1$ = output 1
6 = $Q_2$ = output 2
7 = $W_2$ = input 2
8 = $W_4$ = input 4
9 = $W_6$ = input 6
10 = $N_2$ = supply -6 V (2)



Power Supply

Terminal 1: $V_{N1} = -6V \pm 10\%$, $-I_{N1} = 0\text{–}0.5mA$ [1]) } Nominal value of the current
10: $V_{N2} = -6V \pm 10\%$, $-I_{N2} = 0\text{–}0.5mA$ [1]) }

INPUT DATA

Input Signal Requirements [2])

Voltage: Under all circumstances normally encountered when the unit is used in conjunction with other circuit blocks: $V_{Wn} = 0.1$ to $0.5V$ more positive than $V_Q$ dependent on the input current $I_{Wn}$.

Current: To be supplied to terminal $W_n$ having the least negative voltage level. For $V_{Wn}$ [1]) = 0 volt and $I_Q = 0mA$: $I_{Wn}$ = max. 0.48mA [1]) + max. 0.04mA [1]) for every W terminal at a negative voltage level.

OUTPUT DATA

Output Signal Characteristics [2])

Voltage: see INPUT DATA

Load current $I_Q$ = max. $\frac{-V_N + V_Q}{13}$ mA [1])

Output Impedance

When $V_Q$ is positive-going, the output impedance approximates the output impedance of the driving circuit. When $V_Q$ is negative-going, the output impedance is max. 13kΩ.

LIMITING VALUES

Current through conducting diode $I_{Wc}$ = max. 10mA

Voltage between terminals N and W = max. 30V

[1]) The sign is positive when the current flows towards the circuit.

[2]) These data apply to the most adverse working condition for a combination of units, namely to a supply voltage $V_N = -5.4V$. Unless differently specified, all the voltage and current figures quoted represent absolute maximum values.

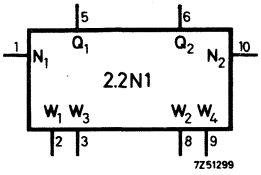
# DUAL NEGATIVE GATE

Colour: orange

The unit 2.2N 1 contains two two-input germanium-diode gates that perform an AND logical operation on negative input voltage signals.

The two gate circuits are identical and can be used separately or combined into a multiple-input gate by interconnecting the output terminals $Q_1$ and $Q_2$. In this latter case, only one negative supply terminal should be used.

| | |
|---|---|
| Pulse repetition frequency range: | 0–100 kHz |
| Ambient temperature range: | −20 to +60 °C |
| Weight: | approx. 20 g |

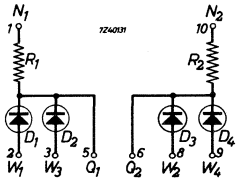



Drawing symbol

CIRCUIT DATA

Terminal

1 = $N_1$ = supply −6V (1)
2 = $W_1$ = input 1
3 = $W_3$ = input 3
4 = not connected
5 = $Q_1$ = output 1
6 = $Q_2$ = output 2
7 = not connected
8 = $W_2$ = input 2
9 = $W_4$ = input 4
10 = $N_2$ = supply −6V (2)




Power Supply

Terminal 1: $V_{N1} = -6V \pm 10\%$, $-I_{N1} = 0\text{–}0.5\,mA$ [1]) } Nominal value of the current
10: $V_{N2} = -6V \pm 10\%$, $-I_{N2} = 0\text{–}0{,}5\,mA$ [1]) }

[1]) The sign is positive when the current flows towards the circuit.

INPUT DATA

Input Signal Requirements [2])

Voltage: Under all circumstances normally encountered when the unit is used in conjunction with other circuit blocks: $V_{Wn}$ = 0.1 to 0.5 V more positive than $V_Q$ dependent on the input current $I_{Wn}$.

Current: To be supplied to terminal $W_n$ having the least negative voltage level. For $V_{Wn}$ = 0 volt and $I_Q$ = 0 mA: $I_{Wn}$ = max. 0.48 mA [1]) + max. 0.04 mA [1]) for every W terminal at a negative voltage level.

OUTPUT DATA

Output Signal Characteristics [2])

Voltage: See INPUT DATA

Load current $I_Q = \text{max.} \frac{-V_N + V_Q}{13}$ mA [1])

Output Impedance

When $V_Q$ is positive-going, the output impedance approximates the output impedance of the driving circuit. When $V_Q$ is negative-going, the output impedance is max. 13 kΩ.

LIMITING VALUES

Current through conducting diode $I_{Wc}$ = max. 10 mA

Voltage between terminals N and W = max. 30 V

[1]) The sign is positive when the current flows towards the circuit

[2]) These data apply to the most adverse working condition for a combination of units, namely to a supply voltage $V_N$ = -5.4 V. Unless differently specified, all the voltage and current figures quoted represent absolute maximum values.

# DUAL POSITIVE GATE

Colour: orange

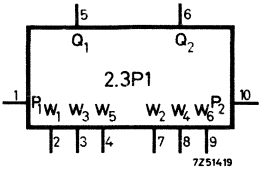
The unit 2.3P1 contains two three-input silicon-diode gates, that perform an OR logical operation on negative input-voltage signals.

The two gate circuits are identical and can be used separately or combined into a multiple-input gate by interconnecting the output terminals $Q_1$ and $Q_2$. In this latter case, only one positive supply terminal should be used.

Pulse repetition frequency range: 0–100 kHz

Ambient temperature range: −20 to +60 °C

Weight: approx. 20 g

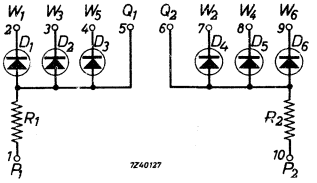



Drawing symbol

CIRCUIT DATA

Terminal

1 = $P_1$ = supply +6V (1)
2 = $W_1$ = input 1
3 = $W_3$ = input 3
4 = $W_5$ = input 5
5 = $Q_1$ = output 1
6 = $Q_2$ = output 2
7 = $W_2$ = input 2
8 = $W_4$ = input 4
9 = $W_6$ = input 6
10 = $P_2$ = supply + 6V (2)




Power Supply

Terminal 1: $V_{P1}$ = 6V ± 10%, $I_{P1}$ = 0.05–0.1 mA [1)]
10: $V_{P2}$ = 6V ± 10%, $I_{P2}$ = 0.05–0.1 mA [1)]

} Nominal value of the current

[1]) The sign is positive when the current flows towards the circuit.

INPUT DATA

Input Signal Requirements [2])

Voltage: Under all circumstances normally encountered when the unit is used in conjunction with other circuit blocks: $V_{Wn}$ = 0.4 to 1 V more negative than $V_Q$ dependent on the input current $I_{Wn}$.

Current : To be supplied to terminal $W_n$ having the most negative voltage level. $-I_{Wn}$ = approx. $I_Q$ + max. 0.07 mA at $-V_Q$ = 1 V.

OUTPUT DATA

Output Signal Characteristics [2])

Voltage: See INPUT DATA

Load current $I_Q$ = approx. $-I_{Wn}$ - max. 0.07 mA [1]) at $-V_Q$ = 1 V

Output Impedance

When $V_Q$ is negative-going, the output impedance approximates the output impedance of the driving circuit. When $V_Q$ is positive-going, the output impedance is max. 130 kΩ.

LIMITING VALUES

Current through conducting diode $I_{Wc}$ = max. 10 mA

Voltage between terminals P and W = max. 30 V

[1]) The sign is positive when the current flows towards the circuit

[2]) These data apply to the most adverse working conditions for a combination of units, namely to a supply voltage $V_P$ = +6.6 V. Unless differently specified, all the voltage and current figures quoted represent absolute maximum values.

# DUAL POSITIVE GATE

Colour: orange

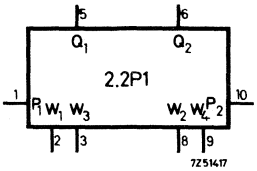
The unit 2.2P1 contains two two-input silicon-diode gates, that perform an OR logical operation on negative input-voltage signals.

The two gate circuits are identical and can be used separately or combined into a multiple-input gate by interconnecting the output terminals $Q_1$ and $Q_2$. In this latter case, only one positive supply terminal should be used.

Pulse repetition frequency range: 0–100 kHz

Ambient temperature range: −20 to +60 °C

Weight: approx. 20 g

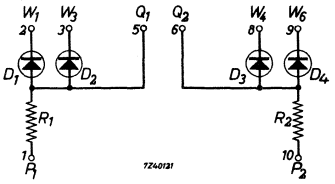



Drawing symbol

CIRCUIT DATA

Terminal

1 = $P_1$ = supply +6 V (1)
2 = $W_1$ = input 1
3 = $W_3$ = input 3
4 = not connected
5 = $Q_1$ = output 1
6 = $Q_2$ = output 2
7 = not connected
8 = $W_2$ = input 2
9 = $W_4$ = input 4
10 = $P_2$ = supply +6 V (2)




Power Supply

Terminal 1: $V_{P1} = 6\,V \pm 10\%$, $I_{P1} = 0.05\text{–}0.1\,mA$ [1]) } Nominal value of the current

Terminal 10: $V_{P2} = 6\,V \pm 10\%$, $I_{P2} = 0.05\text{–}0.1\,mA$ [1]) } Nominal value of the current

[1]) The sign is positive when the current flows towards the circuit

INPUT DATA

Input Signal Requirements [2])

Voltage: Under all circumstances normally encountered when the unit is used in conjunction with other circuit blocks: $V_{Wn}$ = 0.4 to 1V more negative than $V_Q$ dependent on the input current $I_{Wn}$.

Current: To be supplied to terminal $W_n$ having the most negative voltage level. $-I_{Wn}$ = approx. $I_Q$ + max. 0.07 mA at $-V_Q$ = 1V

OUTPUT DATA

Output Signal Characteristics [2])

Voltage: See INPUT DATA

Load current $I_Q$ = approx. $-I_{Wn}$ -max. 0.07 mA [1]) at $-V_Q$ = 1V

Output Impedance

When $V_Q$ is negative-going, the output impedance approximates the output impedance of the driving circuit. When $V_Q$ is positive-going, the output impedance is max. 130 kΩ.

LIMITING VALUES

Current through conducting diode: $I_{Wc}$ = max. 10 mA

Voltage between terminals P and W = max. 30V

[1]) The sign is positive when the current flows towards the circuit

[2]) These data apply to the most adverse working conditions for a combination of units, namely to a supply voltage $V_P$ = +6.6V. Unless differently specified, all the voltage and current figures quoted represent absolute maximum values.

# DUAL PULSE LOGIC

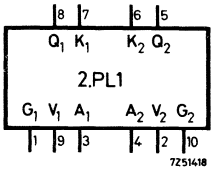
Colour: orange

The unit 2.PL1 contains two identical germanium diode pulse gates which are controlled by a d.c. voltage level.

The circuits are normally used in conjunction with flip-flop circuits. With the dual pulse logic a second pair of a.c. inputs are formed for a flip-flop FF1, or in combination with flip-flops FF2 a bi-directional shift register can be made. In these applications the twin pulse logic output terminals are to be connected directly to the flip-flop d.c. input terminals.

In each circuit a silicon diode is incorporated for reset purposes of the connected flip-flop.

| | |
|---|---|
| Pulse repetition frequency range: | 0–100 kHz |
| Ambient temperature range: | −20 to +60 °C |
| Weight: | approx. 20 g |

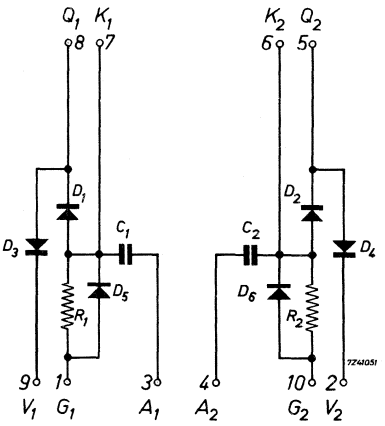



Drawing symbol

CIRCUIT DATA

Terminal

1 = $G_1$ = gate input 1
2 = $V_2$ = reset input 2
3 = $A_1$ = a.c. input 1
4 = $A_2$ = a.c. input 2
5 = $Q_2$ = output 2
6 = $K_2$ = normally not used
7 = $K_1$ = normally not used
8 = $Q_1$ = output 1
9 = $V_1$ = reset input 1
10 = $G_2$ = gate input 2




Power Supply

The unit is not connected to any supply voltage

INPUT DATA

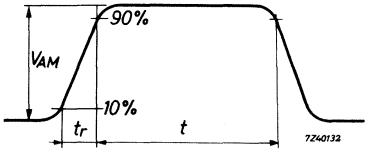
These data are dependent on the driven circuit, the values given apply to use of the dual pulse logic in conjunction with flip-flop circuits FF1 or FF2.

Input Signal Requirements [1])

AC Input Signal (A terminals)

A positive-going voltage step is applied to terminal $A_1$ or $A_2$ or to both terminals interconnected.

This voltage step passes the pulse gate if it has been opened by a proper d.c. gate input signal on terminal $G_1$ ($G_2$)




| | | | |
|---|---|---|---|
| Voltage | $V_{AM}$ | = min. | -0.66 $V_N$ |
| | | = max. | - $V_N$ |
| Rise time | $t_r$ | = max. | 0.4 µs |
| Length of driving pulse | t | = min. | 0.5 µs |
| Input noise level | | = max. | 1 V peak to peak |

Gate Input Signal (G terminals)

A d.c. voltage level is applied to terminal $G_1$ ($G_2$)

The a.c. input signal (terminal $A_1$ ($A_2$)) passes if the corresponding gate input $G_1$ ($G_2$) is at "negative low" level (i.e. gate open).

Note 1: The $G_1$ and $G_2$ input levels should not be "negative low" simultaneously

Note 2: The $G_1$ and $G_2$ input levels have to be present 8 µs before the arrival of the a.c. input signal

[1]) These data apply to the most adverse working condition for a combination of units, namely to supply voltages $V_N$ = -5.4 V and $V_P$ = +6.6 V. Unless differently specified, all the voltage and current figures represent absolute maximum values.

Gate Open (input level "negative low")

Voltage $-V_G$ = max. 0.2V

= min. 0V

Gate Closed (input level "negative high")

Voltage $-V_G$ = min. $V_{AM}$ ($V_{AM}$ = amplitude of a.c. input signal)

= max. $-V_N$

Reset Input Signal (V terminals)

A negative reset signal can be applied to terminal $V_1$ or $V_2$

Current $-I_V$ = min. 0.5mA [1]) ($-V_V$ = max. 1V)

limiting value = max. 10mA [1])

OUTPUT DATA

When used in conjunction with flip-flop circuits FF1 or FF2, the output terminals ($Q_1$ and $Q_2$) are directly connected to the flip-flop d.c. input terminals ($W_1$ and $W_2$)

Input Impedance

Equivalent to a capacitance of approx. 500pF. ($A_1$, $A_2$ terminal or both terminals interconnected).

[1]) The sign is positive when the current flows towards the circuit

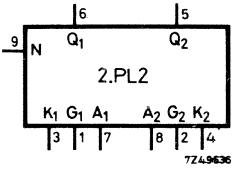
# DUAL PULSE LOGIC

Colour: orange

The unit 2.PL2 contains two identical pulse gates which are controlled by a d.c. voltage level.

The circuits are normally used in conjunction with flip-flop circuits. With the dual pulse logic a second pair of a.c. inputs are formed for a flip-flop FF3, or in combination with flip-flops FF4 a bi-directional shift register can be made. In these applications the 2.PL2 output terminals are to be connected directly to the flip-flop d.c. input terminals.

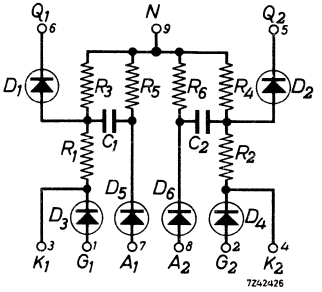
| | |
|---|---|
| Frequency range | : see INPUT DATA |
| Ambient temperature range | : -20 to +60 °C |
| Weight | : approx. 20 g |




Drawing symbol

CIRCUIT DATA

Terminal 1 = $G_1$ = gate input 1
2 = $G_2$ = gate input 2
3 = $K_1$ = terminal for external gate input
4 = $K_2$ = terminal for external gate input
5 = $Q_2$ = output 2
6 = $Q_1$ = output 1
7 = $A_1$ = trigger input 1
8 = $A_2$ = trigger input 2
9 = N = supply -6 V
10 = not connected




Power Supply

Terminal 9 : $V_N$ = -6 V ± 5 %, $-I_N$ = 0-2.5 mA Nominal value of the current

Notes

- The data given apply to the most adverse supply voltages for a combination of units, namely $V_N$=-5.7V and $V_P$=6.3V.
- The temperatures -20 °C and +60 °C, and the tolerances on the supply voltages are absolute limiting values.
- When a current is flowing towards the unit, the positive sign is used.

INPUT DATA

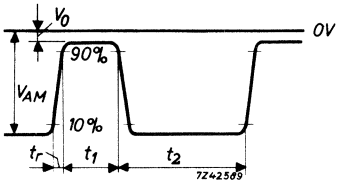
These data are dependent on the driven circuit, the values given apply to use of the dual pulse logic in conjunction with flip-flops FF3 or FF4.

Input Signal Requirements

Trigger Input Signal (A terminals)

A positive going voltage step is applied to terminal $A_1$ or $A_2$ or to both terminals interconnected.

This voltage step passes the pulse gate if it has been opened by an appropriate gate input signal on terminal $G_1(G_2)$.




| | | | | | |
|---|---|---|---|---|---|
| Voltage | $V_{AM}$ | = min. | -0.7 $V_N$ | | |
| | | = max. | - $V_N$ | | |
| | $-V_o$ | = min. | 0 V | | |
| | | = max. | 0.2 V | | |
| | | | $A_1$ or $A_2$ | $A_1$ and $A_2$ interconnected | |
| Required direct current | $I_{AD}$ | = min. | 0.88 mA | min. 1.75 mA | |
| Required current during the transient | | | | | |
| averaged over: 0.4 µs | $I_{AT}$ | = min. | 5 mA | min. 6 mA | |
| 0.7 µs | | = min. | 4 mA | min. 4.5 mA | |

| | | | |
|---|---|---|---|
| Rise time | $t_r$ | = max. 0.7 | µs |
| Pulse duration | $t_1$ | = min. 3 | µs |
| | $t_2$ | = min. 11 | µs |
| Input noise level | $V_n$ | = max. 1 | V peak to peak |

Gate Input Signal (G terminals)

A d.c. voltage level is applied to terminal $G_1$ ($G_2$).

The trigger input signal (terminal $A_1$($A_2$) passes if the corresponding gate is opened by an appropriate gate input signal.

To terminal $K_1$($K_2$) external diodes can be connected (in the same sense as diode $D_3$($D_4$)), to provide the corresponding pulse gate with extra condition inputs.

| | | gate open | gate closed |
|---|---|---|---|
| Voltage | $-V_G$ | = min. 0 V | min. $V_{AM}$ |
| | | = max. 0.2 V | max. - $V_N$ |
| Required gate current caused by negative transient of $V_{AM}$ | $I_{GT}$ | = min. 1.75 mA | min. 1.2 mA |
| | | to open gate | to close gate |
| Required average current during the positive transient of $V_G$ | $I_{GT}$ | = min. 1.6 mA | |
| Gate setting time | | | |
| when the gate input level changes at random | $t_{GS}$ | = min. 17 µs | min. 25 µs |
| when the gate input level changes within 2 µs after the positive going edge of the trigger signal | $t_{GS}$ | = min. 11 µs | min. 11 µs |

Note: The latter applies to a shift register configuration so that the max. shift frequency is approximately 70 kHz

During triggering the G levels should not be at zero voltage level simultaneously.

The gate setting time is the required waiting time between the last G level change and the positive going edge of the trigger pulse.

OUTPUT DATA

When used in conjunction with flip-flops FF3 and FF4, the output terminals ($Q_1$ and $Q_2$) are directly connected to the flip-flop d.c. input terminals ($W_1$ and $W_2$).

# EMITTER FOLLOWER/INVERTER AMPLIFIER

Colour: yellow

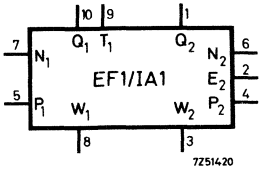
The unit EF1/IA1 contains a transistor emitter-follower circuit and a transistor inverter circuit. The transistors are medium-speed switching types.

The two circuits, i.e. the standard circuits EF1 and IA1, can be used either independently or in combination.

Pulse repetition frequency range: 0–100 kHz

Ambient temperature range: −20 to +60 °C

Weight: approx. 20 g

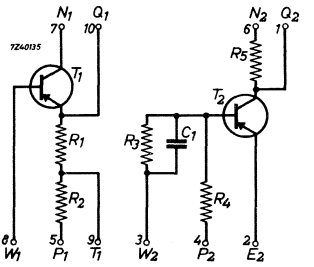



Drawing symbol

CIRCUIT DATA

Terminal

1 = $Q_2$ = output 2
2 = $E_2$ = common supply 0 V
3 = $W_2$ = input 2
4 = $P_2$ = supply +6 V
5 = $P_1$ = supply +6 V
6 = $N_2$ = supply −6 V
7 = $N_1$ = supply −6 V
8 = $W_1$ = input 1
9 = $T_1$ = tapped output 1
10 = $Q_1$ = output 1




EF1 terminals with index 1
IA1 terminals with index 2

Power Supply

| | | | |
|---|---|---|---|
| Terminal 2: | $V_{E2}$ | = 0 V common | |
| 4: | $V_{P2}$ | = +6 V ± 10%, $I_{P2}$ = 0.16 mA [1] | Nominal value of the current |
| 5: | $V_{P1}$ | = +6 V ± 10%, $I_{P1}$ = 3.3–6.6 mA [1] | |
| 6: | $V_{N2}$ | = −6 V ± 10%, $-I_{N2}$ = 0–6 mA [1] | |
| 7: | $V_{N1}$ | = −6 V ± 10%, $-I_{N1}$ = 3.3–25 mA [1] | |

For input and output data see 2.IA1 and 2.EF1 specifications.

[1]) The sign is positive when the current flows towards the circuit

# DUAL EMITTER FOLLOWER

Colour: yellow

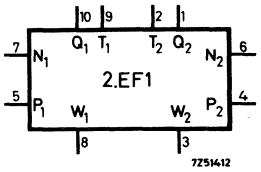
The unit 2.EF1 contains two identical transistor emitter-follower circuits that constitute a non-inverting buffer-amplifier function with a low output impedance. The transistors are medium-speed switching types.

The unit is equipped with a tap on the output resistor for cases in which a level shift towards the positive supply line is required.

Pulse repetition frequency range: 0-100 kHz

Ambient temperature range: -20 to +60 °C

Weight: approx. 20 g

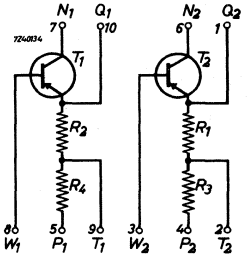



Drawing symbol

CIRCUIT DATA

Terminal

1 = $Q_2$ = output 2
2 = $T_2$ = tap output 2
3 = $W_2$ = input 2
4 = $P_2$ = supply +6V (2)
5 = $P_1$ = supply +6V (1)
6 = $N_2$ = supply -6V (2)
7 = $N_1$ = supply -6V (1)
8 = $W_1$ = input 1
9 = $T_1$ = tap output 1
10 = $Q_1$ = output 1




Power Supply

| | | | |
|---|---|---|---|
| Terminal 4: | $V_{P2}$ | = +6V ± 10%, $I_{P2}$ = 3.3-6.6 mA [1] | Nominal value of the current |
| 5: | $V_{P1}$ | = +6V ± 10%, $I_{P1}$ = 3.3-6.6 mA [1] | |
| 6: | $V_{N2}$ | = -6V ± 10%, $-I_{N2}$ = 3.3-25 mA [1] | |
| 7: | $V_{N1}$ | = -6V ± 10%, $-I_{N1}$ = 3.3-25 mA [1] | |

[1]) The sign is positive when the current flows towards the circuit

INPUT DATA

Input Signal Requirements [2])

A d.c. voltage level is applied to terminal $W_1$ ($W_2$)

Input level "negative low"

Voltage $V_W$ = max. 0.3V more negative than $V_Q$

limiting value = max. 10V

Current $-I_W$ = min. 0.12mA [1]) (unit unloaded)

$I_W$ = max. 0.12mA [1]) ($-I_Q$ at max. value)

Input level "negative high"

Voltage $V_W$ = max. 0.3V more negative than $V_Q$

limiting value $-V_W$ = max. $-V_N$

= min. $-0.7V_N$

Current $-I_W = \text{min.} \frac{I_Q + 6}{34}$ mA [1])

$-I_W = \text{min.} \frac{I_T + 5.1}{34}$ mA [1])

Input Impedance

Equivalent to a capacitance of approx. 20 pF

OUTPUT DATA

Output Signal Characteristics [2])

Output level "negative low"

Voltage $V_Q$ = max. 0.3V more positive than $V_W$

$V_T$ = min. 0.2V

Load current $-I_Q$ = max. 2.2mA [1])

$-I_T$ = max. 1.8mA [1]) at $V_T$ = 0.2V

Output level "negative high"

Voltage $V_Q$ = max. 0.3V more positive than $V_W$

[1]) The sign is positive when the current flows towards the circuit

[2]) These data are derived from the most adverse working condition for a combination of units, namely to supply voltages $V_N$ = -5.4V and $V_P$ = +6.6V. Unless differently specified, all the voltage and current figures quoted represent absolute maximum values.

Load current $I_Q$ and $I_T$

| $V_W$ | $I_{Q\,max}$ | $I_{T\,max}$ at $V_T = -0.5\,V$ | $I_{T\,max}$ at $V_T = -1\,V$ |
|---|---|---|---|
| $0.7V_N$ | 2 mA | 4.5 mA | 3 mA |
| $0.8V_N$ | 4 mA | 6 mA | 4.5 mA |
| $0.9V_N$ | 11 mA | 7.5 mA | 6 mA |
| $0.95V_N$ | 17 mA | 9 mA | 7.5 mA |

Output Impedance

Equivalent to a resistance of approx.

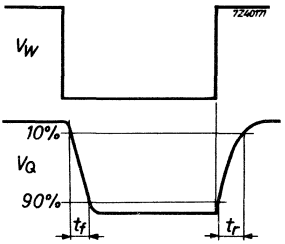
$R_i$ = 2000 Ω for a non-conducting transistor

$R_i$ = $0.03\,Z_o$ for a conducting transistor

($Z_o$ being the output impedance of the unit driving the W terminal)

Switching and Delay Times (for orientation only)

A square wave input signal (W terminal) is assumed with an amplitude of min. $-0.7V_N$.




Unit Unloaded

Fall time $t_f$ = max. 0.1 µs

Rise time $t_r$ = max. 0.1 µs

# DUAL INVERTER AMPLIFIER

Colour: yellow

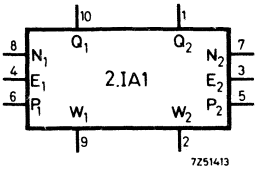
The unit 2.IA1 contains two identical transistor inverter circuits. The transistors are medium-speed switching types.

The circuits constitute an inverting (NOT) function when driven by a signal on the W terminal.

Pulse repetition frequency range: 0–100 kHz

Ambient temperature range: -20 to + 60 °C

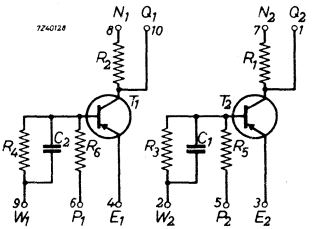
Weight: approx. 20 g




Drawing symbol

CIRCUIT DATA

Terminal
1 = $Q_2$ = output 2
2 = $W_2$ = input 2
3 = $E_2$ = common supply 0V (2)
4 = $E_1$ = common supply 0V (1)
5 = $P_2$ = supply +6V (2)
6 = $P_1$ = supply +6V (1)
7 = $N_2$ = supply -6V (2)
8 = $N_1$ = supply -6V (1)
9 = $W_1$ = input 1
10 = $Q_1$ = output 1




Power Supply

| | | | |
|---|---|---|---|
| Terminal 3: | $V_{E2}$ | = 0V common | |
| 4: | $V_{E1}$ | = 0V common | |
| 5: | $V_{P2}$ | = +6V ± 10%, $I_{P2}$ = 0.16mA [1]) | Nominal value of the current |
| 6: | $V_{P1}$ | = +6V ± 10%, $I_{P1}$ = 0.16mA [1]) | |
| 7: | $V_{N2}$ | = -6V ± 10%, $-I_{N2}$ = 0–6mA [1]) | |
| 8: | $V_{N1}$ | = -6V ± 10%, $-I_{N1}$ = 0–6mA [1]) | |

[1]) The sign is positive when the current flows towards the circuit

INPUT DATA

Input Signal Requirements [2])

Transistor conducting (output level "negative low")

| | | |
|---|---|---|
| Voltage | $-V_W$ = min. | $-0.7V_N$ |
| limiting value | = max. | $-V_N$ |
| Current | $-I_W$ = min. | 0.6mA [1]) |

Transistor non-conducting (output level "negative high")

| | | |
|---|---|---|
| Voltage | $-V_W$ = max. | 0.3V |
| limiting value | $V_W$ = max. | 10V |

Input Impedance

Equivalent to a capacitance of approx. 400 pF.

OUTPUT DATA

Output Signal Characteristics [2])

Transistor conducting (output level "negative low")

| | | |
|---|---|---|
| Voltage | $-V_Q$ = max. | 0.2V |
| Load current | $-I_Q$ = max. | 4.3mA [1]) terminal $N_1$ ($N_2$) connected to $V_N$ |
| | = max. | 10mA [1]) terminal $N_1$ ($N_2$) floating |

Transistor non-conducting (output level "negative high")

| | | |
|---|---|---|
| Voltage | $-V_Q$ = min. | $-0.7V_N$ |
| | $I_Q$ = max. | 1.5mA [1]) terminal $N_1$ ($N_2$) connected to $V_N$ |
| | = | 0mA [1]) terminal $N_1$ ($N_2$) floating |

[1]) The sign is positive when the current flows towards the circuit

[2]) These data apply to the most adverse working conditions for a combination of units, namely to supply voltages $V_N$ = -5.4V and $V_P$ = +6.6V. Unless differently specified, all the voltage and current figures quoted represent absolute maximum values.

Output Impedance

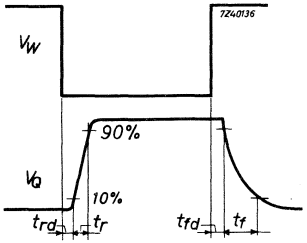
Equivalent to a resistance of approx.

$R_i$ = 50 Ω for positive-going output voltage

$R_i$ = 1000 Ω for negative-going output voltage

Switching and Delay Times (for orientation only)

A square wave input signal is assumed with an amplitude of min. $-0.7V_N$.




Unit Unloaded

| | | |
|---|---|---|
| Rise delay | $t_{rd}$ | = max. 0.1 µs |
| Rise time | $t_r$ | = max. 0.3 µs |
| Fall delay | $t_{fd}$ | = max. 0.6 µs |
| Fall time | $t_f$ | = max. 0.2 µs |

# DUAL EMITTER FOLLOWER

Colour: yellow

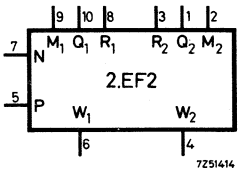
The unit 2.EF2 contains two identical EF2 transistor emitter follower circuits that constitute a buffer amplifier function. The unit has especially been designed to amplify the weak output signals originating from a diode gate circuit.

The unit drives a grounded emitter transistor directly at the base. By connecting the built-in anti-bottoming diode ($D_1$ or $D_2$) via the M terminal to the collector of the driven grounded emitter stage, hole-storage effects in this stage are avoided. In this way short transients are maintained.

The output signal is normally taken from the Q terminal. When a flip-flop is to be set or reset by an EF2, normally the R output is used, the memory property of the flip-flop then being maintained.

The transistors used are medium-speed switching types.

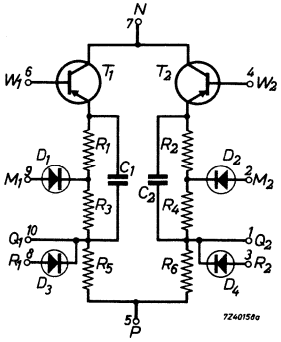
| | |
|---|---|
| Pulse repetition frequency range: | 0-100 kHz |
| Ambient temperature range: | -20 to +60 °C |
| Weight: | approx. 20 g |




Drawing symbol

CIRCUIT DATA

| Terminal | |
|---|---|
| 1 = $Q_2$ | = output 2 |
| 2 = $M_2$ | = clamp diode 2 |
| 3 = $R_2$ | = diode output 2 |
| 4 = $W_2$ | = input 2 |
| 5 = P | = supply +6 V |
| 6 = $W_1$ | = input 1 |
| 7 = N | = supply -6 V |
| 8 = $R_1$ | = diode output 1 |
| 9 = $M_1$ | = clamp diode 1 |
| 10 = $Q_1$ | = output 1 |



Power Supply

Terminal 5: $V_P$ = +6V ± 10%, $I_P$ = 3.5-4mA [1]) Nominal value
7: $V_N$ = -6V ± 10%, $-I_N$ = 4-12mA [1]) of the current

INPUT DATA

Input Signal Requirements [2])

Input level "negative low"

Current $-I_W$ = max. 0.07mA [1]) (unit unloaded)
$I_W$ = max. 0.12mA [1]) ($-I_Q$ at maximum value)

Input level "negative high"

Current $-I_W$ = min. 0.3 mA [1])

The unit can be driven from an N1 gate [3]) or from an N1-P1 gate [3]) sequence.

Limiting Values

Voltage $-V_W$ = max. $-V_N$
$V_W$ = max. 10V

Input Impedance

Equivalent to a capacitance of approx. 50 pF

OUTPUT DATA

Output Signal Characteristics [2])

These data apply to the EF2 driven from an N1 gate [3]) or from an N1-P1 gate [3]) sequence.

---

[1]) The sign is positive when the current flows towards the circuit

[2]) These data are derived from the most adverse working condition for a combination of units, namely to supply voltages $V_N$ = -5.4V and $V_P$ = +6.6V. Unless differently specified, all the voltage and current figures quoted represent absolute maximum values.

[3]) The standard N1 gate is incorporated in the gate units 2.3N1 and 2.2N1, the standard P1 gate is incorporated in the units 2.3P1 and 2.2P1.

EF2 driven from N1 gate [3])

Gate input level "negative low"

Load current $-I_Q$ = max. 0.07 mA [1]) at $V_Q$ = 0.2 V

Gate input level "negative high"

Load current $I_Q$ = max. 2.9 mA [1]) at $-V_Q$ = 0.5 V
$I_R$ = max. 1.9 mA [1]) at $-V_R$ = 0.5 V

EF2 driven from N1-P1 gate [3]) sequence

Gate input level "negative low"

Load current $-I_Q$ = max. 0.12 mA [1]) at $V_Q$ = 0.2 V

Gate input level "negative high"

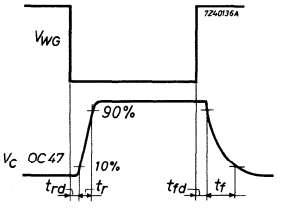
Load current $I_Q$ = max. 0.95 mA [1]) at $-V_Q$ = 0.4 V
$I_R$ = max. 0.5 mA [1]) at $-V_R$ = 0.35 V

Switching and Delay Times (for orientation only)

These data apply to the EF2 driven from an N1-P1 gate [3]) sequence, the EF2 is driving a grounded emitter OC 47 stage from its Q output terminal, the data are given for two values of the OC 47 collector current.

A square wave input signal with an amplitude of min. $-0.7 V_N$ is applied to the gate input terminal.

| Collector current OC 47 | | = 6 mA | = 20 mA |
|---|---|---|---|
| Rise delay | $t_{rd}$ | = max. 0.3 µs | max. 0.6 µs |
| Rise time | $t_r$ | = max. 0.3 µs | max. 1.5 µs |
| Fall delay | $t_{fd}$ | = max. 2 µs | max. 3.5 µs |
| Fall time | $t_f$ | = max. 0.5 µs | max. 1.2 µs |




[1]) See note 1 on previous page

[2]) See note 2 on previous page

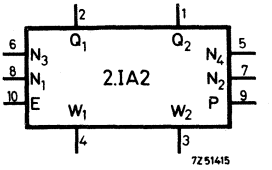
[3]) See note 3 on previous page

# DUAL INVERTER AMPLIFIER

Colour: yellow

The unit 2.IA2 contains two identical inverter amplifier circuits, that constitute an inverting function with an appreciable power amplification between input and output. The unit has especially been designed to amplify the weak output signals originating from a diode gate circuit, whilst it can also be used as a driver for power stages. The transistors used, are medium-speed switching types.

| | |
|---|---|
| Pulse repetition frequency range: | 0–100 kHz |
| Ambient temperature range: | −20 to +60 °C |
| Weight: | approx. 20 g |

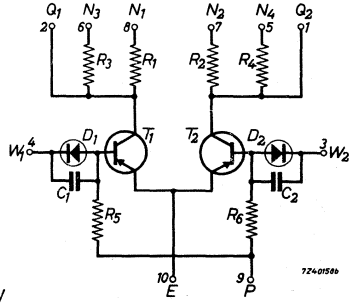



Drawing symbol

CIRCUIT DATA

Terminal

1 = $Q_2$ = output 2
2 = $Q_1$ = output 1
3 = $W_2$ = input 2
4 = $W_1$ = input 1
5 = $N_4$ = supply −6 V (2) [1])
6 = $N_3$ = supply −6 V (1) [1])
7 = $N_2$ = supply −6 V (2) [1])
8 = $N_1$ = supply −6 V (1) [1])
9 = P = supply +6 V
10 = E = common supply 0 V




[1]) Use dependent on application

Power Supply

| | | | |
|---|---|---|---|
| Terminal 5: | $V_{N4}$ | = -6V ± 10%, $-I_{N4}$ = 0-4mA [1] | Nominal value of the current |
| 6: | $V_{N3}$ | = -6V ± 10%, $-I_{N3}$ = 0-4mA [1] | |
| 7: | $V_{N2}$ | = -6V ± 10%, $-I_{N2}$ = 0-2mA [1] | |
| 8: | $V_{N1}$ | = -6V ± 10%, $-I_{N1}$ = 0-2mA [1] | |
| 9: | $V_P$ | = +6V ± 10%, $I_P$ = 0.2mA [1] | |
| 10: | $V_E$ | = 0V common | |

INPUT DATA

Input Signal Requirements [2]

Application 1 (use as gate amplifier): IA2 driven by a standard negative (N1) gate [3], or standard negative (N1) gate followed by a standard positive (P1) gate [3] circuit.

In the latter case the P supply terminal of the P1 gate is left floating.

Transistor conducting (output level "negative low")

Current $-I_W$ = min. 0.3 mA [2] ($-V_W$ = min. 1V)

Transistor non-conducting (output level "negative high")

Voltage $-V_W$ = max. 0.2 V

Application 2 (use as power amplifier): IA2 driven by a grounded emitter stage with a collector resistance of 1 kΩ connected to the -6 V supply terminal. This driving stage can be a standard IA1 circuit (incorporated in the units EF1/IA1 and 2.IA1) or another IA2 circuit with both corresponding −6 V supply terminals connected to the negative supply line. In both cases the collector (Q terminal) of the driving stage is connected directly to the W terminal of the IA2.

---

[1]) The sign is positive when the current flows towards the circuit.

[2]) These data apply to the most adverse working conditions for a combination of units, namely to supply voltages $V_N$ = -5.4 V and $V_P$ = +6.6 V. Unless differently specified, all the voltage and current figures quoted represent absolute maximum values.

[3]) The standard N1 gate is incorporated in the gate units 2.3N1 and 2.2N1, the standard P1 gate is incorporated in the units 2.3P1 and 2.2P1.

Transistor conducting (output level "negative low")

Current $-I_W$ = min. 3.7mA [1]) ($-V_W$ = max. 1.3V)

Transistor non-conducting (output level "negative high")

Voltage $-V_W$ = max. 0.2V

Limiting Values

Voltage $V_W$ = max. 10V

Current $-I_W$ = max. 10mA [1])

OUTPUT DATA

Output Signal Characteristics [2])

Application 1 (see above)

Transistor conducting (output level "negative low")

Voltage $-V_Q$ = max. 0.2V

Load current $-I_Q$ = max. 5.5mA [1]) [3])
= max. 3.6mA [1]) [4])
= max. 0.07mA [1]) [5])

Transistor non-conducting (output level "negative high")

Voltage $-V_Q$ = min. $-0.7V_N$

Load current $I_Q$ = max. 0mA [1]) [3])
= max. 0.5mA [1]) [4])
= max. 1.5mA [1]) [5])

[1]) See note [1]) on previous page

[2]) See note [2]) on previous page

[3]) With all N terminals floating

[4]) With terminals N1 or N2 connected to the -6V supply

[5]) With terminals N1 and N3 or N2 and N4 connected to the -6V supply

Application 2 (see above)

Transistor conducting (output level "negative low")

| | | | |
|---|---|---|---|
| Voltage | $-V_Q$ = max. 0.2 V | = max. 0.25 V | = max. 0.3 V |
| Load current | $-I_Q$ = max. 31 mA [1)3)] | = max. 41 mA [1)3)] | = max. 70 mA [1)3)] |
| | = max. 25 mA [1)5)] | = max. 35 mA [1)5)] | = max. 64 mA [1)5)] |

Transistor non-conducting (output level "negative high")

| | | |
|---|---|---|
| Voltage | $-V_Q$ | = min. $-0.7 V_N$ |
| Load current | $I_Q$ | = 0 mA [1)3)] |
| | | = max. 1.5 mA [1)5)] |

Output Impedance

Equivalent to a resistance of approx.

$R_i$ = 50 Ω for positive-going output voltage

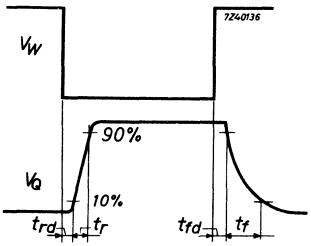
$R_i$ = 1000 Ω for negative-going output voltage [5)]

Switching and Delay Times (for orientation only)

A square wave signal with an amplitude of min. $-0.7 V_N$ is fed via a standard negative (N1) gate [2)] followed by a standard positive (P1) gate [2)], to the W1 (W2) input terminal of the IA2.

Unit Unloaded

| | | |
|---|---|---|
| Rise delay | $t_{rd}$ | = max. 0.5 µs |
| Rise time | $t_r$ | = max. 2.2 µs |
| Fall delay | $t_{fd}$ | = max. 1.2 µs |
| Fall time | $t_f$ | = max. 2.5 µs |




[2)] See note 3 on page A104

[1)3)5)] See corresponding notes on previous page

# PULSE SHAPER

Colour: green

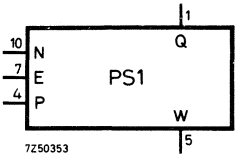
The unit PS1 contains a transistor squaring-amplifier followed by an inverter circuit. The transistors are medium-speed switching types.

A d.c. input signal of a magnitude exceeding the input tripping level of the unit, is re-shaped and inverted into the standard d.c. level at the output. The output voltage transients are very short and can be used for driving other circuit blocks, multivibrator circuits included.

Pulse repetition frequency range: 0-100 kHz

Ambient temperature range: -20 to +60 °C

Weight: approx. 20 g




Drawing symbol

CIRCUIT DATA

Terminal

1 = Q = output

2 = internally connected

3 = internally connected

4 = P = supply +6V

5 = W = input

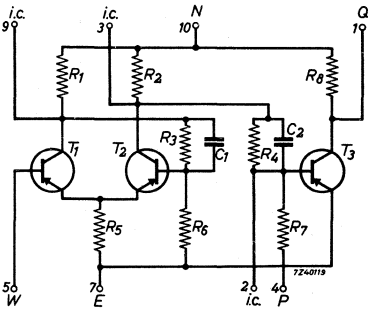
6 = internally not connected

7 = E = common supply 0V

8 = internally not connected

9 = internally connected

10 = N = supply -6V




Power Supply

| | | | |
|---|---|---|---|
| Terminal 4: | $V_P$ | = +6V ± 10%, $I_P$ = 0.48 mA [1] | Nominal value of the current |
| 7: | $V_E$ | = 0V common | |
| 10: | $V_N$ | = -6V ± 10%, $-I_N$ = 3.3-6.2 mA [1] | |

[1]) The sign is positive when the current flows towards the circuit.

INPUT DATA

Input Signal Requirements [2])

A d.c. voltage level is applied to terminal W.

Transistor $T_3$ conducting (output level "negative low")

| | | |
|---|---|---|
| Voltage | $-V_W$ = min. | $-0.4V_N$ |
| Current | $-I_W$ = min. | 0.1 mA [1]) |
| limiting value | = max. | 10 mA [1]) |

Transistor $T_3$ non-conducting (output level "negative high")

| | | |
|---|---|---|
| Voltage | $-V_W$ = max. | 1 V |
| limiting value | $V_W$ = max. | 10 V |
| Current | $I_W$ = min. | 0.07 mA [1]) |

Hysteresis (difference between on and off tripping level)

| | | |
|---|---|---|
| Voltage | $\Delta V_W$ = min. | 0.2 V |

Input Impedance

Equivalent to a capacitance of approx. 330 pF

OUTPUT DATA

Output Signal Characteristics [2])

Transistor $T_3$ conducting (output level "negative low")

| | | |
|---|---|---|
| Voltage | $-V_Q$ = max. | 0.2 V |
| Load current | $-I_Q$ = max. | 1.2 mA [1]) |

Transistor $T_3$ non-conducting (output level "negative high")

| | | |
|---|---|---|
| Voltage | $-V_Q$ = min. | $-0.7V_N$ |
| Load current | $I_Q$ = max. | 0.6 mA [1]) |

[1]) The sign is positive when the current flows towards the circuit.

[2]) These data apply to the most adverse working conditions for a combination of units, namely to supply voltages $V_N$ = -5.4 V and $V_P$ = +6.6 V. Unless differently specified, all the voltage and current figures quoted represent absolute maximum values.

Output Impedance

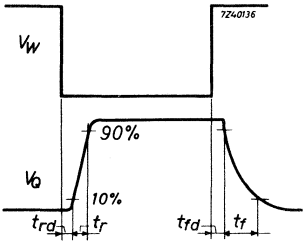
Equivalent to a resistance of approx.

$R_i$ = 100 Ω for positive-going output voltage

$R_i$ = 2200 Ω for negative-going output voltage

Switching and Delay Times (for orientation only)

A square wave input signal is assumed with an amplitude of min. -0.7 $V_N$.




Unit Unloaded

| | | |
|---|---|---|
| Rise delay | $t_{rd}$ | = max. 0.1 µs |
| Rise time | $t_r$ | = max. 0.2 µs |
| Fall delay | $t_{fd}$ | = a function of driving current |
| Fall time | $t_f$ | = max. 0.2 µs |

# PULSE SHAPER

Colour : green

This unit contains a Schmitt trigger followed by an inverter amplifier. An input signal of a magnitude exceeding the thresholds (tripping levels) of the unit, is re-shaped and inverted into the standard d.c. level at the output. The output voltage transients are short and suitable for driving other circuit blocks at their trigger inputs (A).

The terminals A, W, $X_1$ and $X_2$ are provided in order to be able to use the PS 2 for the following purposes:

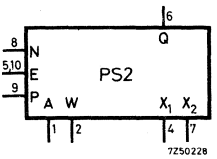
- as a pulse shaper, driven by an external source
- as a relaxation oscillator
- as a crystal controlled oscillator
- as a pulse shaper, driven by circuit blocks of the 100 kHz or 1-Series.

In the last application the number of inputs can be increased by connecting diodes type AAY 21/OA 85/OA 95 to the externally interconnected terminals A and W. The maximum number of diodes is 10.

Pulse repetition frequency range : 0 to 100 kHz

Ambient temperature range : −20 to +60 °C

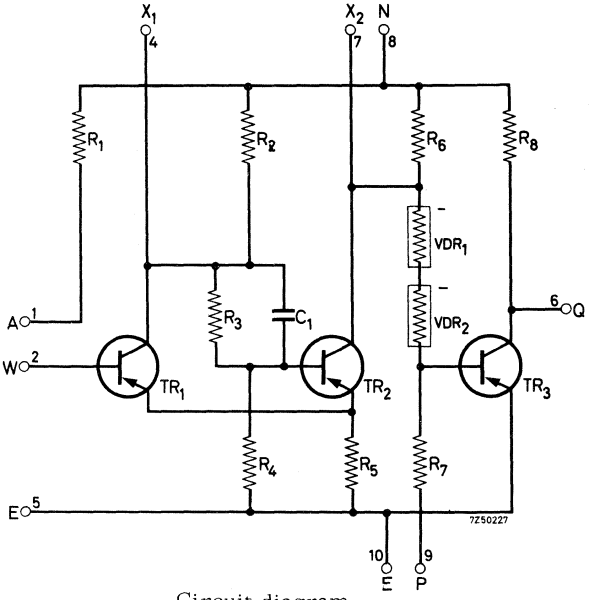
Weight : approx. 20 g




drawing symbol

CIRCUIT DATA

Terminal 1 = A = to be interconnected with terminal 2 for internal driving purposes
2 = W = input
3 = not connected
4 = $X_1$ = internally connected
5 = E = common supply 0 V (interconnected with terminal 10)
6 = Q = output
7 = $X_2$ = internally connected
8 = N = supply −6 V
9 = P = supply +6 V
10 = E = common supply 0 V




Circuit diagram

Power supply

Terminal 8 = $V_N$ = −6 V ±5 %, $-I_N$ = 3.2 - 7.5 mA } nominal value
9 = $V_P$ = +6 V ±5 %, $I_P$ = 0.19 mA } of the current
10 = $V_E$ = 0 V common

Notes

- The data given apply to the most adverse supply voltages for a combination of units, namely $V_N$ = −5.7 V and $V_P$ = +6.3 V.
- The temperatures −20 °C and +60 °C, and the tolerances on the supply voltages are absolute limiting values.
- When a current is flowing towards the unit, the positive sign is used.

INPUT DATA

Unit driven by a non-standard circuit (external souree)

Internal resistance ($R_i$) of the driving circuit
$R_i$ = max. 12 kΩ ($T_{amb}$ = min. 0 °C)
$R_i$ = max. 8 kΩ ($T_{amb}$ = min. −20 °C)

Input voltage to be applied to terminal W:

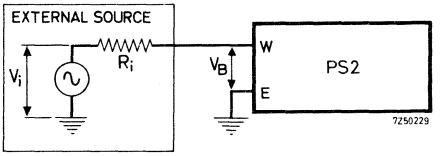
ON threshold (transistor $TR_3$ conducting)

| | operating | limiting value |
|---|---|---|
| Voltage | $-V_W$ = min. −0.4 $V_N$ | = −7.5 V |
| Current | $-I_W$ = max. 0.1 mA | = 15 mA |

OFF threshold (transistor $TR_3$ non-conducting)

| | operating | limiting value |
|---|---|---|
| Voltage | $-V_W$ = max. −0.17 $V_N$ | = −10 V |
| Current | $I_W$ = max. 0.05 mA (at $-V_W$ = 0.2 V) | |
| | = max. 0.1 mA (at $V_W$ = 10 V) | |

Hysteresis (difference between ON and OFF tripping levels)

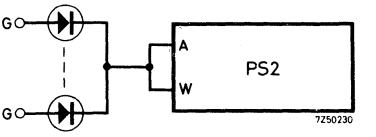



The hysteresis is affected by the internal resistance ($R_i$) of the driving circuit (external source). The relation is given by the following formula:

| $T_{amb}$ = min. 0 °C | $T_{amb}$ = min. −20 °C |
|---|---|
| $\Delta V_i$ = min. (0.07 $V_N$ − 0.033 $R_i$) | $\Delta V_i$ = min. 0.07 $V_N$ − 0.05 $R_i$) |
| $\Delta V_B = \frac{\Delta V_i}{1 + 0.057\ R_i}$ | $\Delta V_B = \frac{\Delta V_i}{1 + 0.071\ R_i}$ |

($R_i$ in kΩ and V in volt)

Unit driven by circuit blocks of the 1-Series




For this operation terminal A has to be connected to terminal W and the input voltage $V_G$ has to be applied via a diode, type AAY 21/OA 85/OA 95. The maximum number of parallel diodes is 10.

Transistor $TR_3$ conducting (output level "negative low")

| | | | |
|---|---|---|---|
| Voltage | $-V_G$ | = max. $-V_N$<br>= min. $-0.7\ V_N$ | |

Transistor $TR_3$ non-conducting (output level "negative high")

| | | | |
|---|---|---|---|
| Voltage | $-V_G$ | = min. 0<br>= max. 0.2 | V<br>V |
| Required direct current | $I_{GD}$ | = max. 0.7 | mA |
| Required transient current<br>averaged over 0.4 $\mu$s<br>averaged over 0.7 $\mu$s | $I_{GT}$ | = max. 1.1<br>= max. 0.75 | mA<br>mA |

OUTPUT DATA

Transistor $TR_3$ conducting (output level "negative low")

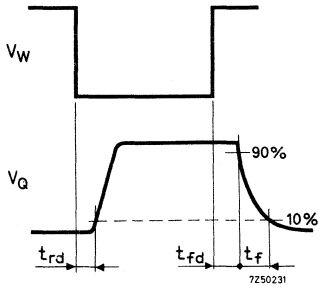
| | | | |
|---|---|---|---|
| Voltage | $-V_Q$ | = max. 0.2<br>= min. 0 | V<br>V |
| Available direct current | $-I_{QD}$ | = max. 20 | mA |
| Available transient current<br>averaged over 0.4 $\mu$s<br>averaged over 0.7 $\mu$s | $-I_{QT}$ | = max. 8<br>= max. 13.7 | mA<br>mA |

Transistor $TR_3$ non-conducting (output level "negative high")

| | | | |
|---|---|---|---|
| Voltage | $V_Q$ | = max. $V_N$ | |
| Current | $I_{QD}$ | = max. 0.65 mA<br>(at $V_Q = 0.7\ V_N$) | |

Switching and delay times (when unit is used in combination with 1-Series circuit blocks)

A square wave input signal is assumed with an amplitude of min. $-0.7\ V_N$




Unit fully loaded

| | |
|---|---|
| Rise delay | $t_{rd}$ = max. 0.7 $\mu$s |
| Fall delay | $t_{fd}$ = max. 1.2 $\mu$s |
| Fall time | $t_f$ = max. 0.7 $\mu$s |

Note

- If for a particular application a capacitor is required between terminal W (2) and earth, use should be made of terminal 5 in order to avoid noise on the common earth point which could disturb the proper operation of the unit.

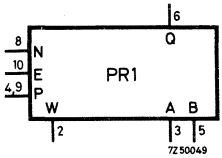
# POSITIVE RESET UNIT

Colour: blue

This unit is intended for resetting purposes of flip-flops FF 1, FF 2, FF 3 and FF 4. When a "negative low" level is applied to the input terminal (W), the unit produces a positive reset signal at its output terminal (Q). The time, that the reset level will be present, is determined by the driving circuit.
In general a reset time of maximum 2 $\mu$s per flip-flop is required when a chain of flip-flops is to be reset.
Up to 15 flip-flops can be reset without external interconnections. By interconnecting the terminals A and P the maximum number of flip-flops that can be reset is 30; by interconnecting the terminals B and P maximum 40 flip-flops can be reset simultaneously.

To reset a flip-flop the output terminal (Q) of the PR1 has to be connected to an input terminal (W) of a flip-flop via a diode OA 85 or OA 95 (anode to Q).

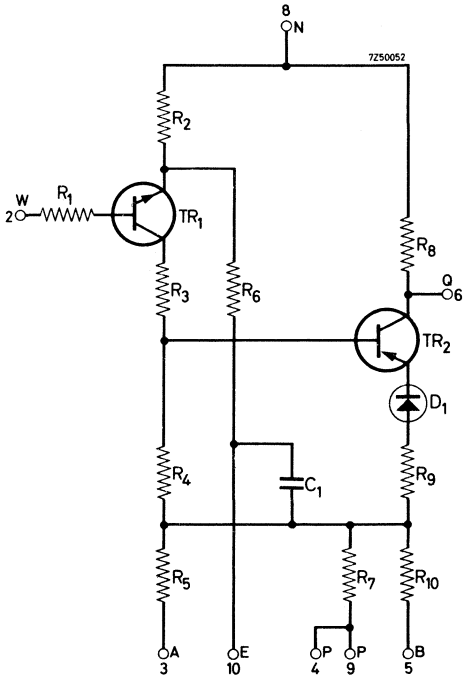
| | |
|---|---|
| Ambient-temperature range | −20 to +60 °C |
| Weight | approx. 20 g |




Drawing symbol

CIRCUIT DATA

Terminal 1 = not connected
2 = W = input
3 = A = to be interconnected with terminal 4 for resetting maximum 30 flip-flops
4 = P = supply + 6 V (internally connected to terminal 9)
5 = B = to be interconnected with terminal 4 for resetting maximum 40 flip-flops
6 = Q = output
7 = not connected
8 = N = supply −6 V
9 = P = supply +6 V
10 = E = common supply 0 V




Circuit diagram

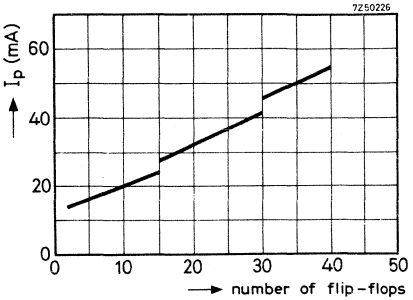
Power supply

Voltages

Terminal 8 : $V_N$ = −6 V ± 5%
9 : $V_P$ = +6 V ± 5%
10 : $V_E$ = 0 V common

Currents (at nominal voltage)

| | $I_N$ | $I_P$ |
|---|---|---|
| W-input at "1" level | −3.5 mA | 1.1 mA |
| W-input at "0" level | −7.5 mA | see diagram on next page. |




Notes

- The data given apply to the most adverse supply voltages for a combination of units, namely $V_N = -5.7$ V and $V_P = +6.3$ V.
- The temperatures $-20\ ^{o}C$ and $+60\ ^{o}C$, and the tolerances on the supply voltages are absolute limiting values.
- When a current is flowing towards the unit, the positive sign is used.

INPUT DATA

Input signal (W-terminal)

A "negative low" level applied to the input terminal (W) produces a positive reset signal at the output terminal (Q).

Transistor TR2 conducting (reset condition)

| | | | |
|---|---|---|---|
| Voltage | $-V_W$ | = min. 0 | V |
| | | = max. 0.2 | V |
| limiting value | $V_W$ | = max. 6.5 | V |
| Required direct current | $I_{WD}$ | = min. 0.1 | mA |
| Required transient current averaged over 0.7 $\mu$s | $I_{WT}$ | = min. 0.08 | mA |

Transistor TR2 non-conducting

| | | | |
|---|---|---|---|
| Voltage | $-V_W$ | = min. 0.7 | $V_N$ |
| | | = max. | $V_N$ |

OUTPUT DATA

Transistor $TR_2$ conducting (reset condition)

| | | | |
|---|---|---|---|
| Voltage | $V_Q$ | = min. 1.0 | V |
| Available direct current | $I_{QD}$ | = min. 15 | mA |
| A and P interconnected | | = min. 30 | mA |
| B and P interconnected | | = min. 40 | mA |

Transistor $TR_2$ non-conducting

| | | | |
|---|---|---|---|
| Voltage | $-V_Q$ | = min. 0.5 | V |
| | | = max. | $V_N$ |

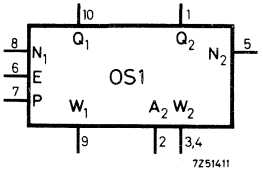
# ONE-SHOT MULTIVIBRATOR

Colour: green

The unit OS1 contains a transistor monostable multivibrator circuit. The transistors are medium-speed switching types.

When a positive-going voltage step is applied to terminal $A_2$ the circuit generates a pulse on the Q-terminals. The length of the output pulse is determined by the value of the external capacitance C between the terminals 4 and 10.

| | |
|---|---|
| Pulse repetition frequency range: | 0–100 kHz |
| Ambient temperature range: | −20 to +60 °C |
| Weight: | approx. 20 g |

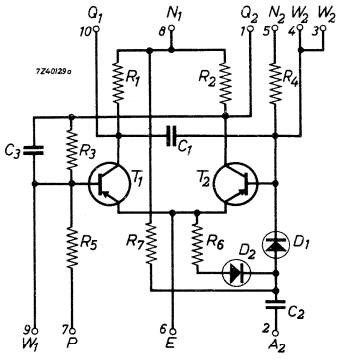



Drawing symbol

CIRCUIT DATA

Terminal

1 = $Q_2$ = output 2
2 = $A_2$ = a.c. input 2
3 = $W_2$ } = d.c. input 2
4 = $W_2$ }
5 = $N_2$ = supply −6 V
6 = E = common supply 0
7 = P = supply +6 V
8 = $N_1$ = supply −6 V
9 = $W_1$ = d.c. input 1
10 = $Q_1$ = output 1




Power Supply

| | | |
|---|---|---|
| Terminal 6: | $V_E$ | = 0 V |
| 7: | $V_P$ | = +6 V ± 10%, $I_P$ = 0.15 mA [1] ) Nominal value |
| 8: | $V_N$ | = −6 V ± 10%, $-I_N$ = 6–7 mA [1] ) of the current |

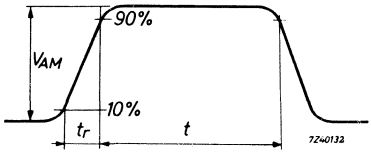
[1]) The sign is positive when the current flows towards the circuit.

## INPUT DATA

### Input Signal Requirements [2])

#### AC Input signal ($A_2$ terminal)

A positive-going voltage step is applied to terminal $A_2$. This voltage step drives the transistor $T_2$ into the non-conducting state.




| | | | |
|---|---|---|---|
| Voltage | $V_{AM}$ | = min. | $-0.66 V_N$ |
| | | = max. | $V_N$ |
| Rise time | $t_r$ | = max. | 0.4 µs |
| Length of driving pulse | t | = min. | 0.5 µs |
| Input noise level | | = max. | 1 V peak to peak |

#### DC Input signal (W terminals)

The W terminals are normally not used.

### Input Impedance

Equivalent to a capacitance of approx. 500 pF ($A_2$ terminal)

## OUTPUT DATA

### Output Signal Characteristics [2])

Transistor conducting (output level "negative low")

| | | | |
|---|---|---|---|
| Voltage | $-V_Q$ | = max. | 0.2 V |
| Load current | $-I_{Q1}$ | = max. | 2.2 mA [1]) |
| | $-I_{Q2}$ | = max. | 0.5 mA [1]) |

Transistor non-conducting (output level "negative "high" )

| | | | |
|---|---|---|---|
| Voltage | $-V_Q$ | = min. | $-0.7 V_N$ |
| Load current | $I_{Q1}$ | = max. | 1.5 mA [1]) |
| | $I_{Q2}$ | = max. | 0.7 mA [1]) |

[1]) The sign is positive when the current flows towards the circuit

[2]) These data apply to the most adverse working conditions for a combination of units, namely to supply voltages $V_N = -5.4$ V and $V_P = +6.6$ V. Unless differently specified, all the voltage and current figures quoted represent absolute maximum values.

Load currents of equal sign, up to the values given as maxima, can be drawn from the two output terminals simultaneously. In the case of simultaneous load currents of opposite sign, the maximum load currents given are not guaranteed.

Maximum Capacitive Load (2000 pF)

When the maximum capacitive and resistive loads are applied in parallel, the given maximum pulse repetition frequency is not guaranteed.

Output Impedance

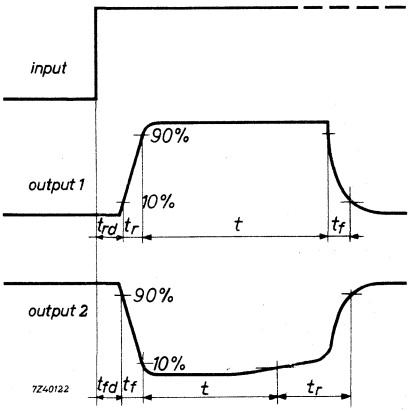
Equivalent to a resistance of approx.

$R_i$ = 50 Ω for positive-going output voltage

$R_i$ = 1000 Ω for negative-going output voltage

Switching and Delay Times (for orientation only)

A square wave input signal ($A_2$ terminal) is assumed with an amplitude of min. $-0.7V_N$.




Unit Unloaded

Output 1 ($Q_1$ terminal)

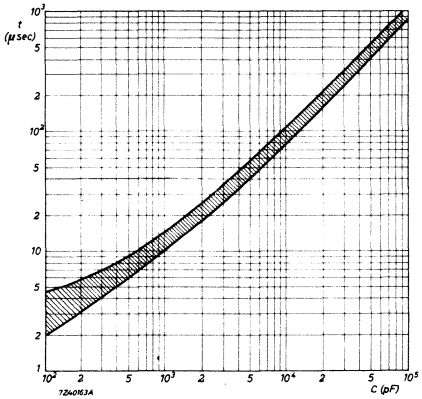
| | | |
|---|---|---|
| Rise delay | $t_{rd}$ | = max. 0.8 µs |
| Rise time | $t_r$ | = max. 0.3 µs |
| Fall time | $t_f$ | = dependent on the external capacitance between the terminals 4 and 10 |

Output 2 ($Q_2$ terminal)

| | | | |
|---|---|---|---|
| Fall delay | $t_{fd}$ | = max. 0.2 µs | |
| Fall time | $t_f$ | = max. 1.8 µs | |
| Rise time | $t_r$ | = max. 1 µs | (without external capacitance) |

Length of the output pulse

When the unit is unloaded, and without external capacitance t = 1.5–4.0 µs




In this diagram, the pulse length t has been plotted as a function of the external capacitance C between the terminals 4 and 10, at an ambient temperature of 25 °C and at supply voltages $V_N$ = -6 V and $V_P$ = +6 V.

Note 1 In case an electrolytic capacitor is used for C, care should be taken that its + terminal is connected to terminal 4. The use of electrolytic capacitors should be avoided when close-tolerance pulse lengths are required.
According as the C value is higher, the sensitivity to disturbing signals (mainly on the supply line -6 V) increases. In this case a large external blocking capacitor may be required between the -6 V supply and 0 V common, to be mounted close to the unit.

Note 2 The length of the output pulse is affected by capacitively loading the $Q_2$ terminal. In general, it will be within 0 to 25 % of the values given above.

Stability of Pulse Length

An increase in supply voltage $V_N$ of 5 % reduces the pulse length by less than 1 %. Any variation of the supply voltage $V_P$ has practically no influence. An increase in ambient temperature of 1 °C reduces the pulse length by less than 0.5 %.

# ONE-SHOT MULTIVIBRATOR

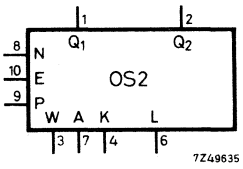
Colour : green

The unit OS2 contains a monostable multivibrator circuit equipped with medium-speed switching type transistors.

When a positive-going voltage step is applied to terminal A, the circuit generates a pulse at the Q-terminals.
The duration of the output pulse is determined by the value of:

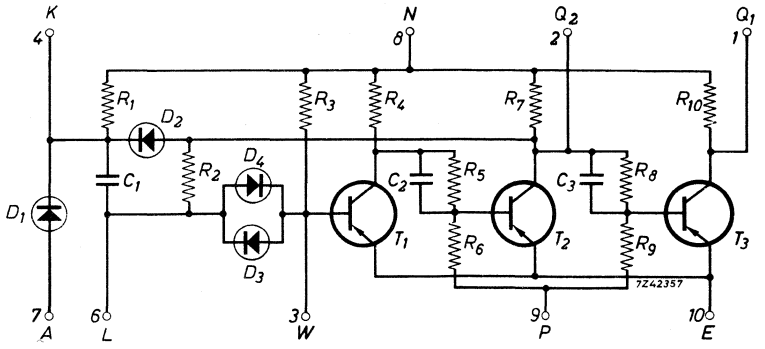
(a) the external capacitance parallel to $C_1$ between the terminals K and L (for pulses longer than the intrinsic value);
(b) the external resistance between the terminals $Q_1$ and W (for pulses shorter than the intrinsic value).

| | |
|---|---|
| Frequency range | 0 - 100 kHz |
| Permissible ambient temperature | -20 to +60 °C |
| Weight | approx. 20 g |




Drawing symbol

CIRCUIT DATA



Terminals

| | | | |
|---|---|---|---|
| 1 = $Q_1$ | = output 1 | 6 = L | = for external capacitor |
| 2 = $Q_2$ | = output 2 | 7 = A | = trigger input |
| 3 = W | = d.c. input | 8 = N | = supply (-6 V) |
| 4 = K | = for external capacitor | 9 = P | = supply (+6 V) |
| 5 = not connected | | 10 = E | = common of supply (0 V) |

Power supply

8 : $V_N$ = -6 V ± 5 %, $-I_N$ = 8.8 mA

9 : $V_P$ = +6 V ± 5 %, $I_P$ = 0.4 mA nominal value

10 : $V_E$ = 0 V common

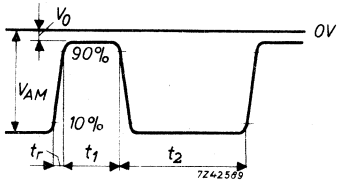
Notes

- The data given apply to the most adverse supply voltages for a combination of units, namely $V_N$ = -5.7 V and $V_P$ = 6.3 V.
- The temperatures -20 °C and +60 °C, and the tolerances on the supply voltages are absolute limiting values.
- When a current is flowing towards the unit, the positive sign is used.

## INPUT REQUIREMENTS

Trigger input signal (A terminal)

A positive-going voltage pulse is applied to terminal A. The leading edge of this voltage pulse drives by means of the transistor $T_1$ the transistor $T_2$ into the conducting, and the transistor $T_3$ into the non-conducting state.




Voltage levels

$V_{AM}$ = min. -0.7 $V_N$

= max. $-V_N$

$-V_o$ = min. 0 V

= max. 0.2 V

| | | | | |
|---|---|---|---|---|
| Required current during the transient | | | | |
| averaged over: 0.4 µs | $I_{AT}$ | = min. | 2.4 | mA |
| 0.7 µs | | = min. | 1.4 | mA |
| Required direct current 1) | $I_{AD}$ | = min. | 1.3 | mA |
| Rise time | | | | |
| without external capacitor | $t_r$ | = max. | 0.4 | µs |
| with a capacitor of min. 200 pF between terminals K and L | $t_r$ | = max. | 0.7 | µs |
| Duration of driving pulse | $t_1$ | = min. | 1 | µs |
| Recovery time | $t_2$ | = min. | 6 | µs 2) |
| when the duration of the output pulse ($t_o$) exceeds 7.5 µs | $t_2$ | = min. | 0.8 | $t_o$ 2) |
| Input noise level | $V_n$ | = max. | 1 | V peak to peak |

OUTPUT DATA

Voltages and currents

| Transistor conducting | | Output $Q_1$ | Output $Q_2$ |
|---|---|---|---|
| Voltage | $-V_Q$ | = max. 0.2 V | max. 0.2 V |
| Available direct current | $-I_{QD}$ | = max. 18 mA | max. 6 mA |
| Available current during the transient | | | |
| averaged over: 0.4 µs | $-I_{QT}$ | = max. 19 mA | max. 15 mA |
| 0.7 µs | | = max. 25 mA | max. 21 mA |

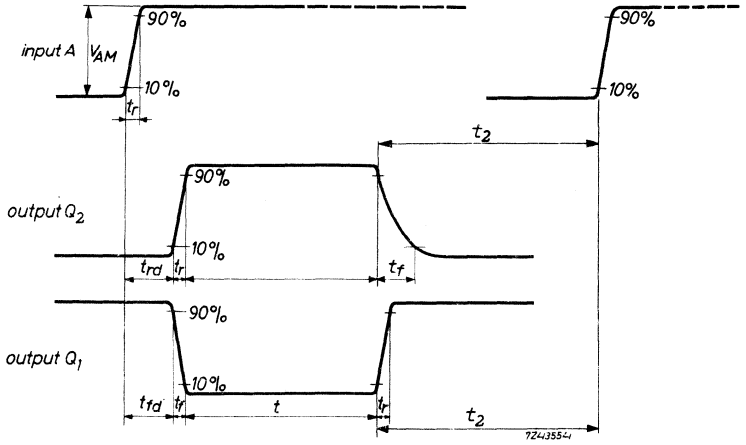
| Transistor non-conducting | | Output $Q_1$ | Output $Q_2$ |
|---|---|---|---|
| Voltage | $-V_Q$ | = min. $-0.7\ V_N$ | min. $-0.7\ V_N$ |
| Available direct current | $I_{QD}$ | = max. 0.7 mA | max. 0.25 mA |

1) This is the current flowing to the input of the OS2 during the input pulse after decay of the output pulse, if the duration of the input pulse is longer.

2) The recovery time $t_2$ is starting at the trailing edge ot $V_A$ when $t_1 > t_o$ and at the trailing edge of $V_{Q2}$ when $t_o > t_1$

## Switching and delay times

These data refer to an input signal as specified under "Input Data".




| Unit unloaded | | Output $Q_1$ | Output $Q_2$ |
|---|---|---|---|
| Rise delay | $t_{rd}$ = | - | $t_{rA}$ + max. 0.4 µs |
| Rise time | $t_r$ = | max. 0.2 µs | max. 0.2 µs |
| Fall delay | $t_{fd}$ = | $t_{rA}$ + max. 0.5 µs | - |
| Fall time | $t_f$ = | max. 0.4 µs | max. 3 µs |

## Duration of the output pulse

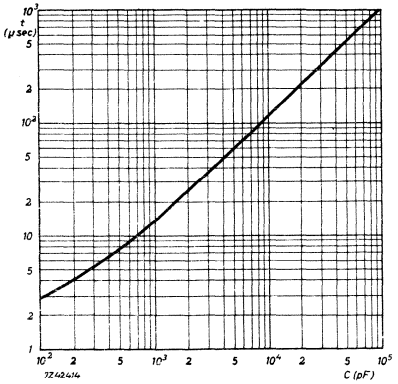
Unit unloaded

| | |
|---|---|
| Intrinsic value | $t_o$ = max. 4 µs |
| With resistor of 12 kΩ [1] between terminals $Q_1$ and W | $t_o$ = max. 2 µs |

With a capacitor between terminals K and L, at an ambient temperature of 25 °C and supply voltages $V_N$ = -6 V and $V_P$ = +6 V, see figure given below.

For larger capacitances log t is proportionate to log C.

[1]) minimum permissible value




Stability of pulse duration

A variation of the supply voltage $V_N$ of 5 % varies the pulse duration by less than 1 % in the same direction.

The influence of a variation of the supply voltage Vp of 5 % is negligible.

An increase in ambient temperature by 1 °C gives a reduction of the pulse duration of less than 0.5 % and vice versa.

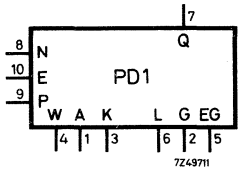
Note. In case an electrolytic capacitor is used for $C_{ext}$ care should be taken that its + terminal is connected to terminal 6.

# PULSE DRIVER

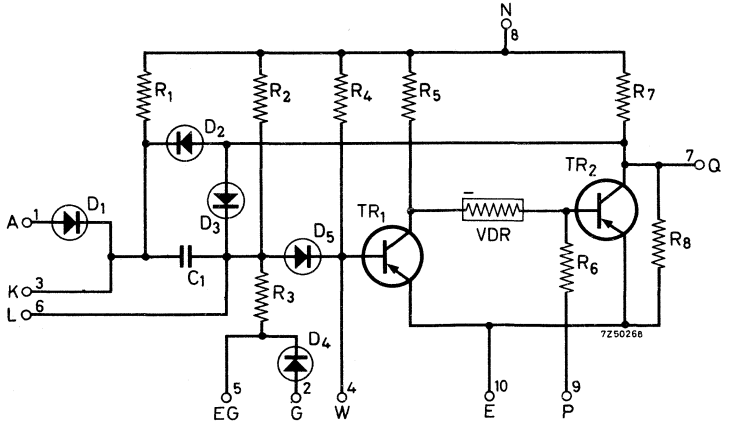
Colour: green

The unit PD1 contains a monostable multivibrator with a built-in trigger gate. It is mainly intended as a clock source, delivering trigger pulses for a great number of flip-flops FF1, FF2, FF3, and FF4 or as a counter driver.
The trigger gate can be controlled by a d.c. voltage level applied to terminal G.
The number of condition inputs can be extended with the aid of external diodes OA85/OA95 at the extension input E.G.
When a positive-going voltage step is applied to terminal A, the unit generates a pulse at the output (Q)-terminal, provided the gate is open.
The duration of the output pulse can be increased by means of an external capacitor between the terminals K and L (for pulses longer than the intrinsic value, e.g. necessary when driving a FF4 or 2PL2).
For mounting in the chassis 4322 026 38240 a printed-wiring board PDA 1, catalogue number 4322 026 34710, is available. On this standard printed-wiring board up to four PD 1's can be mounted (see section "ACCESSORIES FOR CIRCUIT BLOCKS 100 kHz SERIES").

| | |
|---|---|
| Frequency range | : see INPUT DATA |
| Permissible ambient temperature | : -20 to +60 °C |
| Weight | : approx. 20 g |




Drawing symbol



## CIRCUIT DATA

Terminal 1 = A = trigger input
2 = G = gate input
3 = K = for external capacitor
4 = W = d.c. input
5 = EG = extension gate input
6 = L = for external capacitor
7 = Q = output
8 = N = supply -6 V
9 = P = supply +6 V
10 = E = common supply 0 V

### Power supply

Terminal 8: $V_N$ = -6 V ± 5 %, $-I_N$ = 26 mA ($T_1$ conducting)
= 51 mA ($T_2$ conducting)
9: $V_P$ = +6 V ± 5 %, $I_P$ = 0.4 mA
10: $V_E$ = 0 V common

Notes

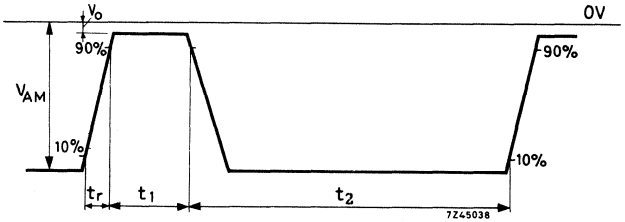
- The data given apply to the most adverse supply voltages for a combination of units, namely $V_N$ = -5.7 V and $V_P$ = 6.3 V.
- The temperatures -20 °C and +60 °C, and the tolerances on the supply voltages are absolute limiting values.
- When a current is flowing towards the unit, the positive sign is used.

## INPUT DATA

### Input Signal Requirements

#### Trigger Input Signal (A terminal)

A positive-going voltage step is applied to input terminal A. This voltage step generates a pulse at the output Q if the gate has been opened by an appropriate gate input signal on terminal G.




Voltage

$V_{AM}$ = min. -0.7 $V_N$
= max. - $V_N$
$-V_o$ = min. 0 V
= max. 0.2 V

| | |
|---|---|
| Required direct current | $I_{AD}$ = min. 1.7 mA |
| Required average current during the transient | $I_{AT}$ = min. 1.5 mA (practically independent of rise time) |
| Rise time | $t_r$ = max. 0.7 µs |
| Pulse duration | $t_1$ = min. 1 µs |
| Recovery time | $t_2$ = min. 6 µs (without external capacitor) |
| | $t_2$ = min. 11 µs (with $C_{EXT}$ = 1000 pF between terminals K and L) |
| Note | Type of diodes and maximum number to be connected in parallel at terminal K: 6 x OA85/OA95. |

Input Impedance:

Equivalent to a capacitance of 500 pF.

Gate Input Signals (G-terminals)

A d.c. voltage level is applied to terminal G. A "negative low" voltage opens the gate.

| | | Gate open | Gate closed |
|---|---|---|---|
| Voltage | $-V_G$ | = min. 0 V | min. - 0.7 $V_N$ |
| | | max. 0.2 V | max. - $V_N$ |
| Required gate current caused by negative transient of $V_A$ | $I_{GD}$ | = min. 1.75 mA | min. 0.5 mA |
| Required average current during the positive transient of $V_G$ | | $I_{GT}$ = min. 1.2 mA | |

Gate Setting Times:

| When the gate changes at random: | | to open gate | to close gate |
|---|---|---|---|
| Without external capacitor | $t_{gs}$ | = min. 8.5 µs | min. 25 µs |
| With an external capacitor of 1000 pF between K and L | | = min. 24 µs | 75 µs |

| | | to open gate | to close gate |
|---|---|---|---|
| When the gate level changes within 1 µs after the positive going edge of the trigger signal: | | | |
| Without external capacitor | $t_{gs}$ | = min. 6 µs | 0 |
| With external capacitor of 1000 pF between K and L | | = min. 11 µs | 0 |

Notes

- The gate setting time is the time the gate (G)-signal shall be present in advance to open the gate for the trigger (A) -signal.
- The absolute maximum value of the external capacitor is 1000 pF.
- Type of diodes and maximum number to be connected in parallel at terminal EG: 6 x OA85/OA95.

W-terminal (base connection transistor T1):

Transistor $T_1$ non-conducting:

Voltage limiting value

$V_W$ = min. 0.2 V
$V_W$ = max. 2.5 V

These voltages may be applied for max. 5 µs and a max.freq. of 100 kHz

Transistor $T_1$ conducting:

Current (limiting value)

$-I_W$ = max. 2 mA
(at $-V_W$ = max. 0.5 V)

Up to max.6 output-Q terminals of pulse logic units 2.PL2 may be connected to the W-input terminal of the PD 1 each via a resistor of 560 Ω ± 5%.

OUTPUT DATA

Voltages and Currents

Transistor conducting:

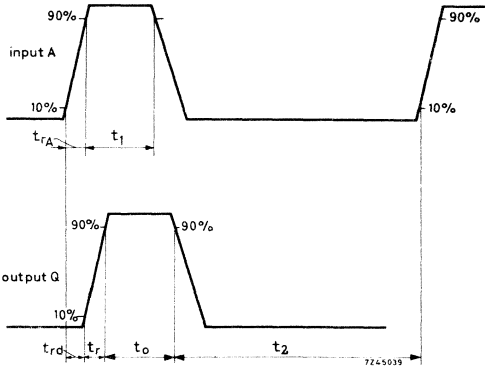
| | | |
|---|---|---|
| Voltage | $-V_Q$ | = max. 0.2 V |
| Available direct current | $-I_{QD}$ | = max. 65 mA |
| Available current during the transient: averaged over 0.7 µs | $-I_{QT}$ | = max. 90 mA |

Transistor non-conducting :

Voltage $-V_Q$ = min. - 0.7 $V_N$
= max. - 0.84 $V_N$

Switching and Delay Times:

These data are for orientation only and refer to an input signal as specified under INPUT DATA.




$t_{rd} = t_{rA} + 0.2$ µs
(fully loaded)

| Unit max. loaded with: | $t_r + t_o$: | ext. capacitor between terminals K and L: |
|---|---|---|
| 20 x FF1 or FF2 | max. 1.5 µs | none |
| 5 x FF3 | min. 1.2 µs | none |
| 20 x FF3 | max. 2 µs | none |
| 20 x FF4 (at 70 kHz) | max. 4 µs | $C_{ext}$ = 1000 pF ± 5% (absolute max. value of $C_{ext}$). |

The recovery time $t_2$ is starting at the trailing edge of $V_A$ when $t_1 > t_o$ and at the trailing edge of $V_Q$ when $t_o > t_1$ ($t_1$ = duration of input pulse $V_A$).

The typical output pulse duration of an unloaded pulse driver PD 1, triggered via a PL 2 unit (at 70 kHz): $t_r + t_o = 3.2$ µs.

# POWER AMPLIFIER

The PA1 consists of an n-p-n/p-n-p transistor amplifier circuit, designed to be used as a power amplifier in the range of circuit blocks. The amplifier is non-inverting, and can be driven directly by the circuit blocks FF1, FF2, FF3, FF4, GI1, IA1, IA2 and OS2

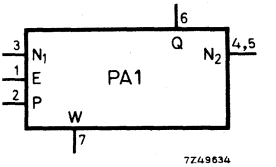
The output loadability is 600 mA at 60 V (abs. max. values). The built-in diode across the output terminals protects the output transistor against voltage transients which occur when the unit is driving an inductive load.

The circuit is mounted on an epoxy-paper printed-wiring board, the output transistor is provided with an aluminium heat sink.

Frequency range : 0-100 Hz

Ambient temperature range: -20 to +60 °C

Weight : approx. 60 g




CIRCUIT DATA

Terminal: 1 = E = common supply 0 V

2 = P = supply +6 V

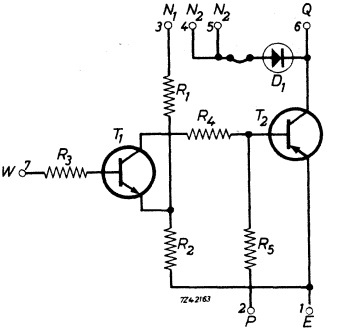
3 = N1 = supply -6 V

4 = N2 ) = supply abs. max. 60 V

5 = N2 )

6 = Q = output

7 = W = input




Power Supply

Terminal: 1: $V_E$ = 0 V common

2: $V_P$ = 6 V ± 10 %, $I_P$ = max. 20 mA 1) 2)

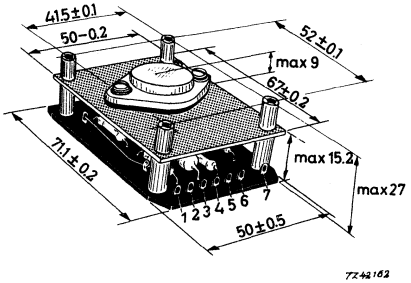
3: $V_{N1}$ = -6 V ± 10 %, $-I_{N1}$ = max. 70 mA ($T_2$ non-conducting)
= max. 110 mA ($T_2$ conducting)

4) 5) $V_{N2}$ = max. 60 V, $-I_{N2}$ = max. 600 mA 1) 2)

1) The sign is positive when the current flows towards the unit.

2) When $-V_{N2}$ is applied to the unit, care must be taken that Vp is present as well, otherwise transistor T2 may be damaged.

## MECHANICAL CONSTRUCTION




The dimensions (approx. 71 mm x 50 mm x 27 mm) and terminal location can be seen from the figure given above. Since the aluminium heat sink is insulated from the circuit, no special measures need be taken as regards mounting of the unit.

In the mounting chassis 4322 026 38240 the PA 1 is to be mounted directly on a printed-wiring board. On such a standard printed-wiring board PAA 1 up to four PA 1's can be mounted, the next position in the chassis being left empty.
To ensure proper cooling of the unit, the PA 1 has to be mounted in such a way that a free flow of air through it is guaranteed.

## INPUT DATA

Input Signal Requirements 2)

A d.c. voltage level is applied to terminal W.

Output-transistor conducting

| | | | |
|---|---|---|---|
| Voltage | $-V_w$ | = | max. 0.2 V<br>min. 0 V |
| Current | $I_w$ | = | min. 2.5 mA 1) |

Output-transistor non-conducting

| | | | |
|---|---|---|---|
| Voltage | $-V_w$ | = | min. 4.25 V |
| Limiting value | | = | max. 13.2 V |
| Current | $-I_w$ | = | min. 0.1 mA 1) |

## OUTPUT DATA

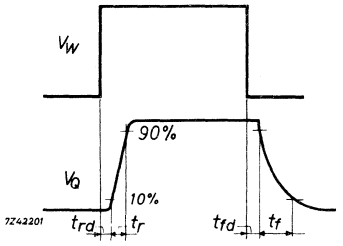
Output Signal Characteristics 2)

Output transistor conducting

| | | | |
|---|---|---|---|
| Voltage | $-V_Q$ | = | max. 0.75 V |
| Load current | $-I_Q$ | = | max. 600 mA 1) |

Output transistor non-conducting

| | | | |
|---|---|---|---|
| Voltage | $-V_Q$ | = | max. 60 V (dependent on the value of $V_{N2}$ which is abs. max. 60 V.) |
| Leakage current | $-I_Q$ | = | max. 14.5 mA 1) |




1) The sign is positive when the current flows towards the unit.

2) These data apply to the most adverse working conditions for a combination of units, namely to supply voltages $V_N$ = -5.4 V and $V_p$ = +6.6 V. Unless differently specified, all the voltage and current figures quoted represent absolute maximum values.

Switching and Delay Times (for orientation only)

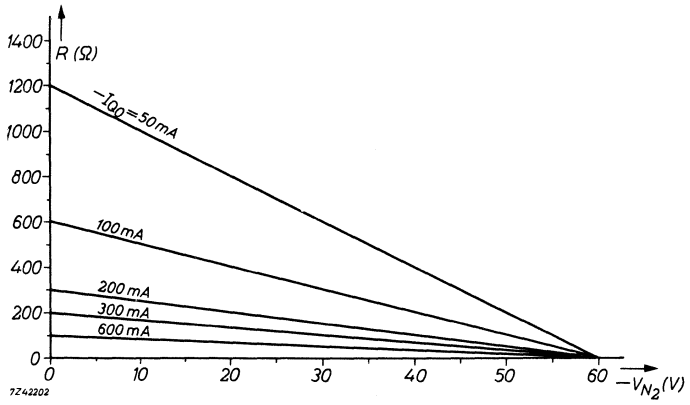
A square wave input signal is applied with an amplitude of 4.25 V, a rise time of max. 2.2 µs and a fall time of max. 2.5 µs

Unit loaded with a resistor of 100 Ω

| | | | |
|---|---|---|---|
| Rise delay | $t_{rd}$ | = max. | 15 µs |
| Rise time | $t_r$ | = max. | 120 µs |
| fall delay | $t_{fd}$ | = max. | 70 µs |
| fall time | $t_f$ | = max. | 60 µs |

Unit loaded with an inductive load

The unit is provided with a built-in diode to protect the output transistor against voltage transients which occur when an inductive load is switched. This protection is realised at the expense of a very long fall delay time of the current in this load. At supply voltages below 60 V, however, a wire jumper in series with this diode can be interchanged with a resistor to decrease this delay time.
The maximum permissible value of this resistor is given in the figure below, with the current flowing through the load at the moment of switching-off as parameter.



# DECADE COUNTER

The unit DC1 consists of four flip-flops type FF1 mounted on a printed wiring board, the flip-flops are connected as a counter.

The counter is provided with pulse feed-back to achieve that six of the sixteen possible positions are skipped. The flip-flops can be reset by means of a common positive signal.

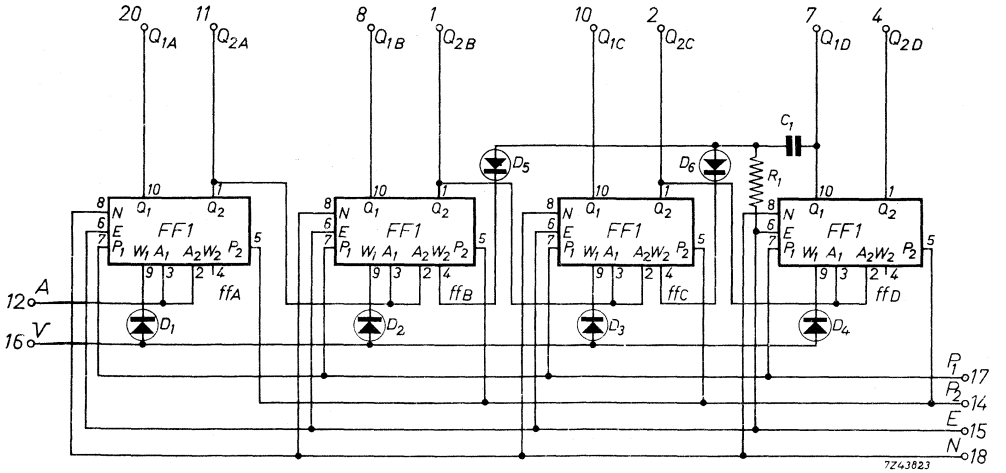
The reset diodes $D_1$, $D_2$, $D_3$, $D_4$ and the feed-back network $D_5$, $D_6$, $R_1$ and $C_1$ are mounted on the printed wiring board.

The printed wiring board 4322 026 33620 is provided with plated-through holes, double sided printed wiring and double sided gold-plated contacts.

The mating connector type 2422 020 51491 is normally not supplied with the counter.

| | |
|---|---|
| Pulse repetition frequency range | : 0 - 100 kHz |
| Ambient temperature range | : -20 to + 60 °C |
| Weight | : approx. 100 g |

CIRCUIT DATA



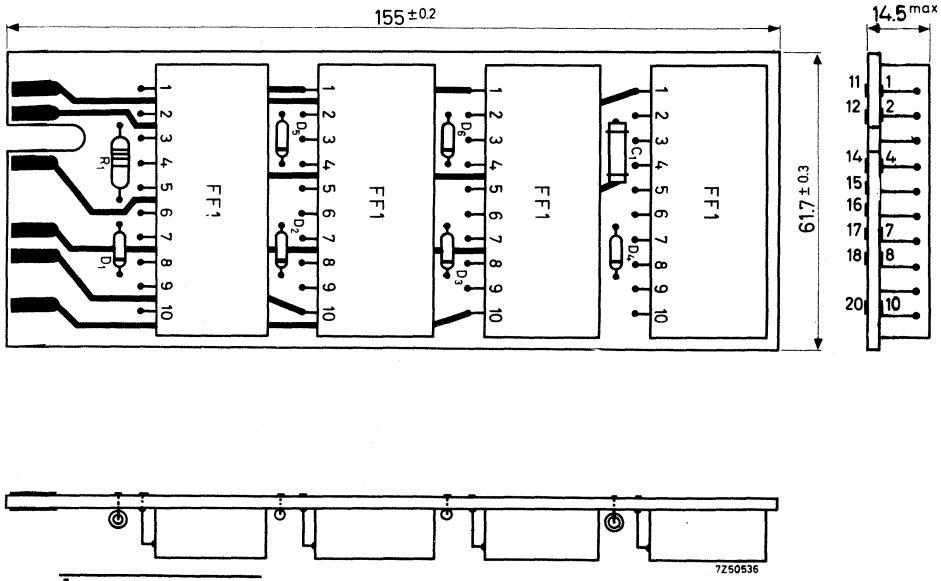
Terminal:

| | |
|---|---|
| 1 = $Q_{2B}$ = output 2 flip-flop B | 12 = A = a.c. input |
| 2 = $Q_{2C}$ = output 2 flip-flop C | 14 = $P_2$ = supply +6V (2) |
| 4 = $Q_{2D}$ = output 2 flip-flop D | 15 = E = common supply 0V |
| 7 = $Q_{1D}$ = output 1 flip-flop D | 16 = V = reset input |
| 8 = $Q_{1B}$ = output 1 flip-flop B | 17 = $P_1$ = supply +6V (1) |
| 10 = $Q_{1C}$ = output 1 flip-flop C | 18 = N = supply -6V |
| 11 = $Q_{2A}$ = output 2 flip-flop A | 20 = $Q_{1A}$ = output 1 flip-flop A |

Power Supply

| | | |
|---|---|---|
| Terminal 14: | $V_{P2}$ = +6V ± 10%, $I_{P2}$ = 0.6mA [1] | Nominal value of the current |
| 15: | $V_E$ = 0V common | |
| 17: | $V_{P1}$ = +6V ± 10%, $I_{P1}$ = 0.6mA [1] | |
| 18: | $V_N$ = -6V ± 10%, $-I_N$ = 28mA [1] | |

DIMENSIONS AND TERMINAL LOCATION







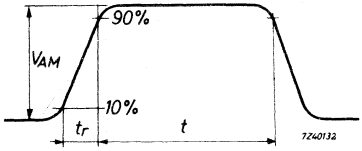
[1]) The sign is positive when the current flows towards the circuit

INPUT DATA

Input Signal Requirements [2])

AC Input Signal (A terminal)

A positive-going voltage step is applied to terminal A. This voltage step advances the counter one position.




| | | | |
|---|---|---|---|
| Voltage | $V_{AM}$ | = min. | $-0.66\ V_N$ |
| | | = max. | $-\ V_N$ |
| Rise time | $t_r$ | = max. | 0.4 µs |
| Length of driving pulse | $t$ | = min. | 0.5 µs |
| Input noise level | | = max. | 1 V peak to peak |

Reset Input Signal (V terminal)

For resetting the counter a positive d.c. voltage is applied to terminal V. This signal causes all $Q_1$ terminals to reach "negative high" and all $Q_2$ terminals to reach "negative low" level.

Input level during reset

| | | | |
|---|---|---|---|
| Voltage | $V_V$ | = min. | 1 V |
| limiting value | | = max. | 10 V |
| Current | $I_V$ | = min. | 4 mA [1]) |
| | | ($I_V$ = approx. 4.4 mA [1]) at $V_V$ = 6 V) | |

[1]) The sign is positive when the current flows towards the circuit

[2]) These data apply to the most adverse working condition for a combination of units, namely to supply voltages $V_N$ = -5.4 V and $V_P$ = +6.6 V. Unless differently specified, all the voltage and current figures represent absolute maximum values.

Input level during counting

During counting terminal V should be left floating or be returned to a voltage level:

Voltage $-V_V$ = min. 0.4 V

limiting value = max. 30 V

Input Impedance

Equivalent to a capacitance of approx. 500 pF (A terminal)

OUTPUT DATA

These data apply to each individual flip-flop stage.

Output Signal Characteristics [2])

Transistor conducting (output level "negative low")

Voltage $-V_Q$ = max. 0.2 V

Load current $-I_Q$ = max. 2.5 mA [1])

Transistor non-conducting (output level "negative high")

Voltage $-V_Q$ = min. $-0.7 V_N$

Load current $I_Q$ = max. 0.7 mA [1])

Load currents of equal sign, up to the values given as maxima, can be drawn from two corresponding output terminals simultaneously. In the case of simultaneous load currents of opposite sign, the maximum load currents given are not guaranteed.

Maximum Capacitive Load

1. If loaded during positive as well as negative-going pulses (e.g. FF1, FF2, OS1):

500 pF for terminals $Q_{1D}$ and $Q_{2D}$ together

1500 pF for terminals $Q_{1A}$ and $Q_{2A}$ together,

$Q_{1B}$ and $Q_{2B}$ together,

$Q_{1C}$ and $Q_{2C}$ together

[1]) See note 1 on previous page

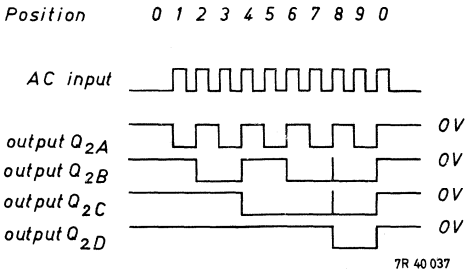
[2]) See note 2 on previous page

2. If loaded only during positive-going pulses
(e.g. FF3, FF4, OS2):

500 pF for terminal $Q_{1D}$
1500 pF for each terminal $Q_{2A}$, $Q_{2B}$, $Q_{2C}$
2000 pF for each terminal $Q_{1A}$, $Q_{1B}$, $Q_{1C}$, $Q_{2D}$

When the maximum capacitive and resistive loads are applied in parallel, the given maximum pulse repetition frequency is not guaranteed.

Output levels during counting




The output levels at the $Q_2$ terminals can be taken from the above figure. Note that when a $Q_2$ output is at "negative low" level the corresponding $Q_1$ terminal is at "negative high" level and vice-versa.

# DUAL DECADE COUNTER

The unit 2.DCA 2 contains two identical decade counter units, mounted on a printed wiring board. Each counter consists of four flip-flops FF3, connected to operate in the 1-2-4-8 code. To achieve this operation, it is provided with a gate-diode with the result that six of the sixteen possible positions are skipped. The flip-flops can be reset by means of a common positive signal.

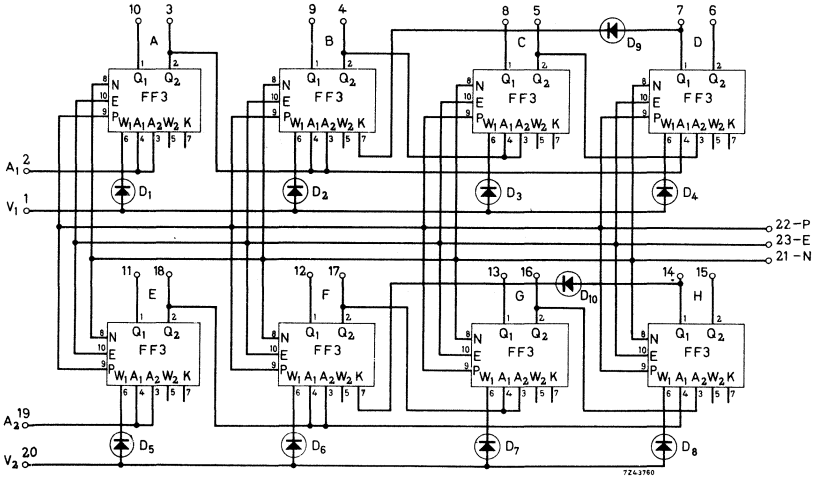
The reset diodes $D_1$ up to $D_8$ inclusive and the gate-diodes $D_9$ and $D_{10}$ are mounted on the printed wiring board as well.

The printed wiring board is provided with plated-through holes and single-sided gold-plated contacts.

With the mating connector , 2422 020 52592, not supplied with the dual decade counter, the printed wiring board of standard dimensions (121.8mm x x 180.3mm x 1.6mm) can be used directly in the standard mounting chassis, catalog number 4322 026 38240.

The fixation of the circuit blocks FF3 to the p.w. board is secured by means of locking tags, catalog number 4322 026 33690.

| | |
|---|---|
| Pulse repetition frequency range: | 0 - 100 kHz |
| Ambient temperature range: | -20 to +60 °C |
| Weight: | approx. 210 g |




Terminal

| | |
|---|---|
| 1 = $V_1$ = reset input counter 1 | 13 = $Q_{1G}$ = output 1 flip-flop G |
| 2 = $A_1$ = a.c. input counter 1 | 14 = $Q_{1H}$ = output 1 flip-flop H |
| 3 = $Q_{2A}$ = output 2 flip-flop A | 15 = $Q_{2H}$ = output 2 flip-flop H |
| 4 = $Q_{2B}$ = output 2 flip-flop B | 16 = $Q_{2G}$ = output 2 flip-flop G |
| 5 = $Q_{2C}$ = output 2 flip-flop C | 17 = $Q_{2F}$ = output 2 flip-flop F |
| 6 = $Q_{2D}$ = output 2 flip-flop D | 18 = $Q_{2E}$ = output 2 flip-flop E |
| 7 = $Q_{1D}$ = output 1 flip-flop D | 19 = $A_2$ = a.c. input counter 2 |
| 8 = $Q_{1C}$ = output 1 flip-flop C | 20 = $V_2$ = reset input counter 2 |
| 9 = $Q_{1B}$ = output 1 flip-flop B | 21 = N = common negative supply |
| 10 = $Q_{1A}$ = output 1 flip-flop A | 22 = P = common positive supply -6V |
| 11 = $Q_{1E}$ = output 1 flip-flop E | 23 = E = common supply 0V +6V |
| 12 = $Q_{1F}$ = output 1 flip-flop F | |

Power Supply

Terminal 21: $V_N = -6V \pm 5\%$, $-I_N = 70mA$

22: $V_P = +6V \pm 5\%$, $I_P = 4.8mA$

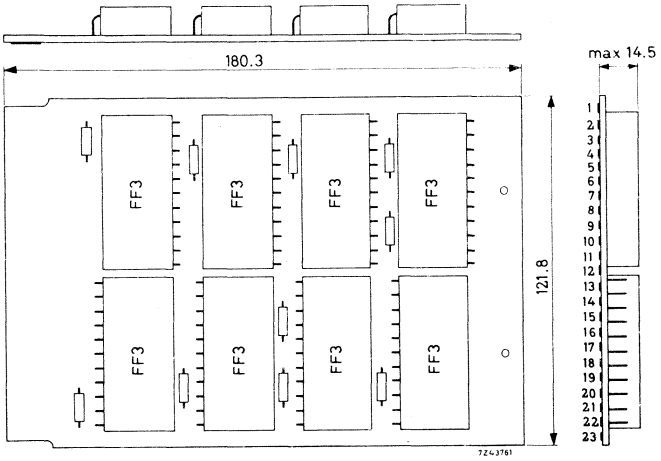
23: $V_E = 0V$

} Nominal value of the current

Notes:

- When a current is flowing towards the unit, the positive sign is used
- The data given apply to the most adverse supply voltages for a combination of units, namely
  $V_N = -5.7V$ and $V_P = +6.3V$
- The temperatures -20 °C and +60 °C, and the tolerances on the supply voltages are absolute limiting values.

Dimensions and Terminal Location

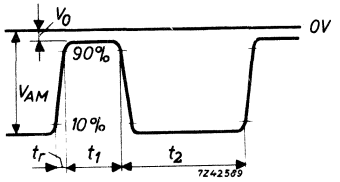



INPUT DATA

Input Signal Requirements

Trigger Input Signal ($A_1$ and/or $A_2$ terminals)

A positive-going voltage step is applied to terminal A. This voltage step advances the counter one position.



| | | |
|---|---|---|
| Voltage | $V_{AM}$ | = min. $-0.7V_N$ |
| | | = max. $-V_N$ |
| | $-V_0$ | = min. 0V |
| | | = max. 0.2V |
| Required direct current | $I_{A1D}(I_{A2D})$ | = min. 1.75mA |
| Required current during the transient averaged over 0.4µs | $I_{A1T}$ ($I_{A2T}$) | = min. 6mA |
| 0.7µs | | = min. 4.5mA |
| Rise time | $t_r$ | = max. 0.7µs |
| Pulse duration | $t_1$ | = min. 1µs |
| | $t_2$ | = min. 8µs |
| Input noise level | $V_n$ | = max. 1V peak to peak |

Reset Input Signal ( $V_1$ and/or $V_2$ terminals)

For resetting the counter a positive d.c.voltage is applied to terminal V. This signal causes all $Q_1$-terminals to reach a "negative-high" and all $Q_2$-terminals to reach a "negative-low" level.

Input level during reset

| | | |
|---|---|---|
| Voltage | $V_{v1}$ ($V_{v2}$) | = min. 1V |
| | | = max. 10V |
| Current | $I_{v1}$ ($I_{v2}$) | = min. 3.6 mA |

During counting it is recommended that terminal $V_1$ and/or $V_2$ are connected to a voltage level.

| | | |
|---|---|---|
| Voltage | $-V_{v1}$ ($-V_{v2}$) | = min. 0.4V |
| | | = max. 15V |
| Current | $-I_{v1}$ ($-I_{v2}$) | = min. 0.12mA (at $-V_{v1}$ ($-V_{v2}$) = 0.4V) |

OUTPUT DATA

These data apply to the various flip-flop stages.

## Output Signal Characteristics

### Transistor non-conducting

Voltage: $-V_Q$ = min. $-0.7V_N$

Available direct current $I_{QD}$ = max. 0.7 mA

### Transistor conducting

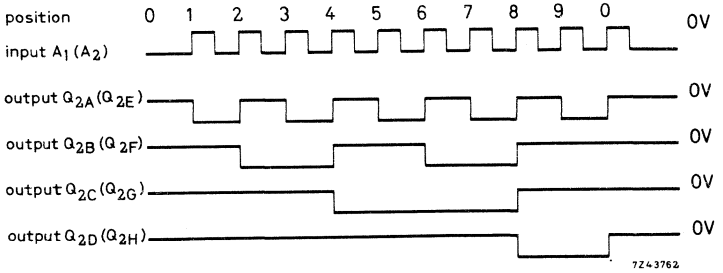
Voltage $-V_Q$ = max. 0.2 V
= min. 0 V

| | | output $Q_1$ | | output $Q_2$ | | | |
|---|---|---|---|---|---|---|---|
| | | Flip-Flop A-B-C E-F-G- | Flip-Flop D-H | Flip-Flop A-E | Flip-Flop B-F | Flip-Flop C-G | Flip-Flop D-H |
| max. available current during transient $-I_{QT}$ | averaged over 0.4 µs | 11 mA | 11 mA | 4 mA | 5 mA | 6 mA | 11 mA |
| | averaged over 0.7 µs | 14 mA | 14 mA | 9 mA | 9.5 mA | 10 mA | 14 mA |
| maximum available direct current $-I_{QD}$ | | 6 mA | 5.1 mA | 3.4 mA | 4.25 mA | 5.1 mA | 6 mA |

### Maximum Speed:

For all loads within the limits mentioned above, also applied simultaneously, the maximum counting speed of 100 kHz is guaranteed.

### Output levels during counting




The output levels at the $Q_2$-terminals are shown in the figure above.
Note that when a $Q_2$ output is at "negative-low" level the corresponding $Q_1$ output is at "negative-high" level and vice versa.
After 10 positive-going voltage steps at the input terminal $A_1$ ($A_2$), the output terminal $Q_{2D}$ ($Q_{2H}$) delivers one positive-going voltage step, whilst the decade counter has resumed its initial position, namely all $Q_2$-terminals being at 0V level.

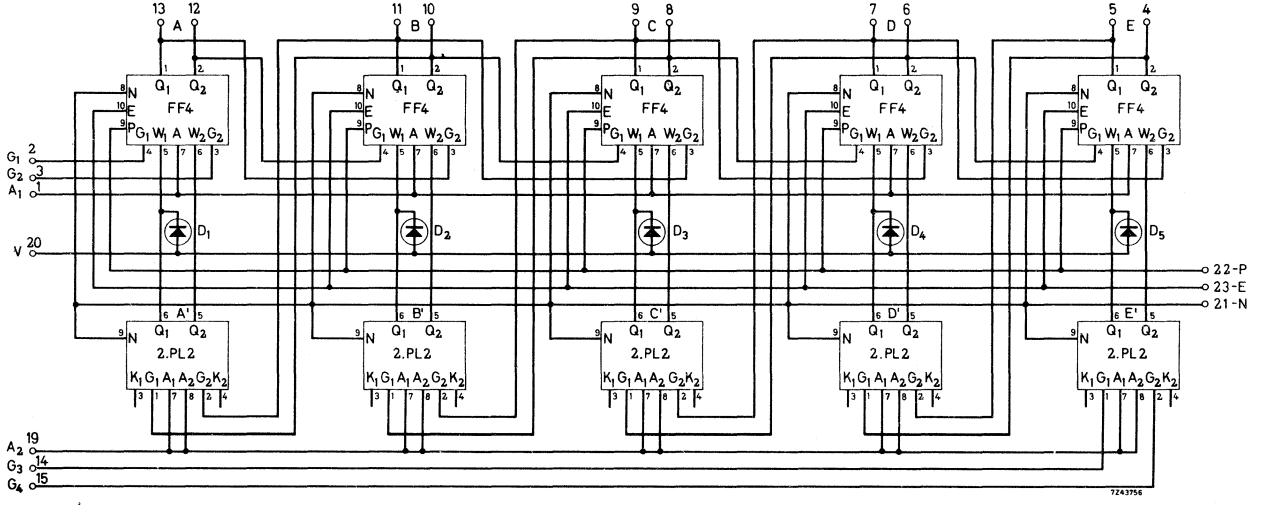
# REVERSIBLE COUNTER

The unit BCA 1 consists of five flip-flops FF4 and five dual pulse logic's 2.PL2, mounted on a printed-wiring board, interconnected to operate as a bi-directional shift register. A bi-directional decade counter can be realised by interconnecting the gate (G)-terminals of the first flip-flop with the output (Q)-terminals of the fifth flip-flop and the gate (G)-terminals of the fifth dual pulse logic with the output (Q)-terminals of the first flip-flop. These interconnections have to be made externally in such a way that the Q1- respectively Q2-terminal has to be connected with the corresponding $G_1$- respectively $G_2$-terminal.

The flip-flops can be reset by means of a common positive signal. The five reset diodes $D_1$ up to $D_5$ inclusive are mounted on the printed-wiring board as well. The printed-wiring board is provided with plated through holes and single sided gold plated contacts.
With the mating connector catalog number 2422 020 52592, not supplied with the reversible counter, this printed-wiring board of standard dimensions (121.8 mm x 180.3 mm x 1.6 mm) can be used directly in the standard mounting chassis catalog number 4322 026 38240. The fixation of the circuit blocks FF4 and 2.PL2 is secured by means of locking tags catalog number 4322 026 33690.

| | |
|---|---|
| Pulse repetition frequency range: | 0 - 70 kHz |
| Ambient temperature range: | −20 to +60 °C |
| Weight: | approx. 250 g |

## CIRCUIT DATA




Terminal

| | | | | | |
|---|---|---|---|---|---|
| 1 = $A_1$ | = a.c. input forward direction | 9 = $Q_{1C}$ | = output 1 flip-flop C | 16 = not connected | |
| 2 = $G_1$ | = gate input ($G_1$) flip-flop A | 10 = $Q_{2B}$ | = output 2 flip-flop B | 17 = not connected | |
| 3 = $G_2$ | = gate input ($G_2$) flip-flop A | 11 = $Q_{1B}$ | = output 1 flip-flop B | 18 = not connected | |
| 4 = $Q_{2E}$ | = output 2 flip-flop E | 12 = $Q_{2A}$ | = output 2 flip-flop A | 19 = $A_2$ | = a.c. input reverse direction |
| 5 = $Q_{1E}$ | = output 1 flip-flop E | 13 = $Q_{1A}$ | = output 1 flip-flop A | 20 = V | = reset input |
| 6 = $Q_{2D}$ | = output 2 flip-flop D | 14 = $G_3$ | = gate input ($G_1$) dual pulse logic E' | 21 = N | = common negative supply -6 V |
| 7 = $Q_{1D}$ | = output 1 flip-flop D | | | 22 = P | = common positive supply +6 V |
| 8 = $Q_{2C}$ | = output 2 flip-flop C | 15 = $G_4$ | = gate input ($G_2$) dual pulse logic E' | 23 = E | = common supply 0 V |

Power Supply

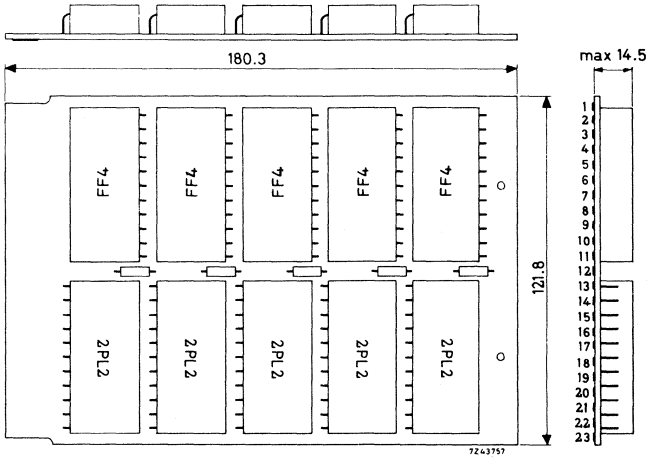
Terminal 21: $V_N = -6V \pm 5\%$, $-I_N = 55mA$
22: $V_P = +6V \pm 5\%$, $I_P = 3mA$
} Nominal value of the current

23: $V_E = 0V$

Notes

- When a current is flowing towards the unit, the positive sign is used
- The data given apply to the most adverse supply voltages for a combination of units, namely
  $V_N = -5.7V$ and $V_P = +6.3V$
- The temperatures $-20\,^{\circ}C$ and $+60\,^{\circ}C$ and the tolerances on the supply voltages are absolute limiting values

Dimensions and terminal location



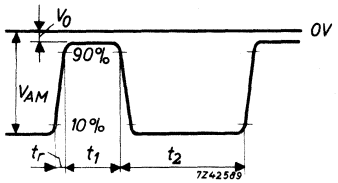

INPUT DATA

Input Signal Requirements

Trigger Input Signal ($A_1$ or $A_2$ terminal)

A positive-going voltage step is applied to terminal A. When this voltage step is applied to terminal $A_1$ the counter advances one position, when it is applied to terminal $A_2$ the counter reverses one position.

Voltage $V_{AM}$ = min. $-0.7V_N$
= max. $-V_N$
$-V_0$ = min. 0V
= max. 0.2V




Required direct current $I_{A1D}$ ($I_{A2D}$) = min. 8.8mA

Required current during the transient:
averaged over 0.4 µs $I_{A1T}$ ($I_{A2T}$) = min. 30mA
0.7 µs = min. 22.5mA

Rise time $t_r$ = max. 0.7 µs

Pulse duration $t_1$ = min. 3 µs

$t_2$ = min. 11 µs

Input noise level $V_n$ = max. 1V p-p

Gate Input Signal ($G_1$ and $G_2$ or $G_3$ and $G_4$ terminals)

A d.c. voltage level is applied to these G-terminals

| | | gate open | gate closed |
|---|---|---|---|
| Voltage | $-V_G$ = min. | 0V | $V_{AM}$ |
| | = max. | 0.2V | $-V_N$ |
| Required gate current caused by negative transient of $V_{AM}$ | $I_{GD}$ = min. | 1.75mA | min. 1.2 mA |
| Required average current during the positive transient of $V_G$ | $I_{GT}$ = min. | 1.6mA | |
| Gate setting time | | | |
| when the gate input level changes at random | $t_{GS}$ = min. | 17 µs | min. 25 µs |
| when the gate input level changes within 2 µs after the positive going edge of the trigger signal | $t_{GS}$ = min. | 11 µs | min. 11 µs |

Notes
- The latter applies to the shift register configuration so that the max. shift frequency is approximately 70 kHz
- During triggering the G levels should not be at zero voltage level simultaneously
- The gate setting time is the required waiting time between the last G level change and the positive-going edge of the trigger pulse

Reset Input Signal (V-terminal)

For resetting the counter a positive d.c. voltage is applied to terminal V. This signal causes all $Q_1$-terminals to reach a "negative high" and all $Q_2$-terminals to reach a "negative low" level.

Input Level during Reset

| | | |
|---|---|---|
| Voltage | $V_v$ = min. | 1 V |
| | = max. | 10 V |
| Current | $I_v$ = min. | 4.5 mA |

During shifting it is recommended that terminal V is connected to a voltage level:

| | | |
|---|---|---|
| Voltage | $-V_v$ = min. | 0.4 V |
| | = max. | 15 V |
| Current | $-I_v$ = min. | 0.15 mA (at $-V_v$ = 0.4 V) |

OUTPUT DATA

These data apply to the various flip-flop stages:

Output Signal Characteristics

Transistor non-conducting

| | | |
|---|---|---|
| Voltage | $-V_Q$ = min. | $-0.7 V_N$ |
| Available direct current | $I_{QD}$ = max. | 0.7 mA |

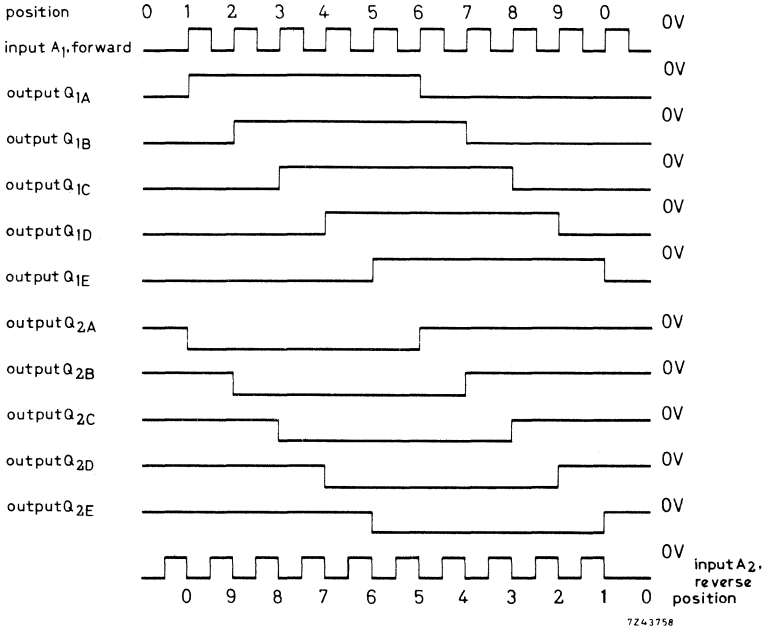
Transistor conducting

| | | |
|---|---|---|
| Voltage | $-V_Q$ = max. | 0.2 V |
| | = min. | 0 V |

| | | flip-flops B-C-D | flip-flops A-E |
|---|---|---|---|
| available current during the transient $-I_{QT}$ | averaged over 0.4 µs | max. 8 mA | max. 9.4 mA |
| | averaged over 0.7 µs | max. 11 mA | max. 12.4 mA |
| available direct current $-I_{QD}$ | | max. 3.75 mA | max. 4.25 mA |

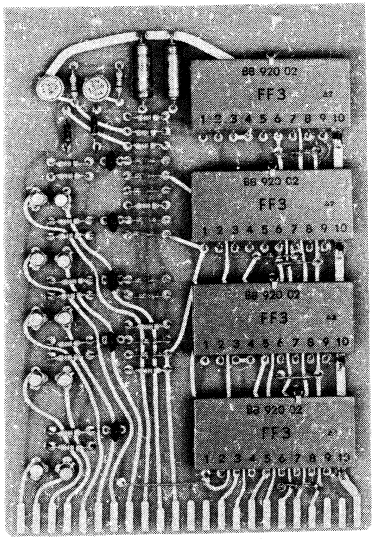
These current data apply to the unit, operating as a bi-directional shift register. When the unit is interconnected to form a bi-directional decade counter the lowest current values of $-I_{QT}$ and $-I_{QD}$ are valid for all flip-flops.

Output levels during counting, when the unit is externally interconnected to form a bi-directional decade counter. To this end terminals 2 and 5, 3 and 4, 12 and 15, 13 and 14 have to be connected.
The output levels at the Q-terminals can be taken from the figure below.




Note that after 10 positive-going voltage steps at the input terminal $A_1$ ($A_2$), the output terminal $Q_{2E}$ ($Q_{2A}$) delivers one positive-going voltage step, whilst the decade counter has retaken its initial position, namely all $Q_2$-terminals being at 0V level.

# DECADE COUNTER AND NUMERICAL INDICATOR TUBE DRIVER ASSEMBLY



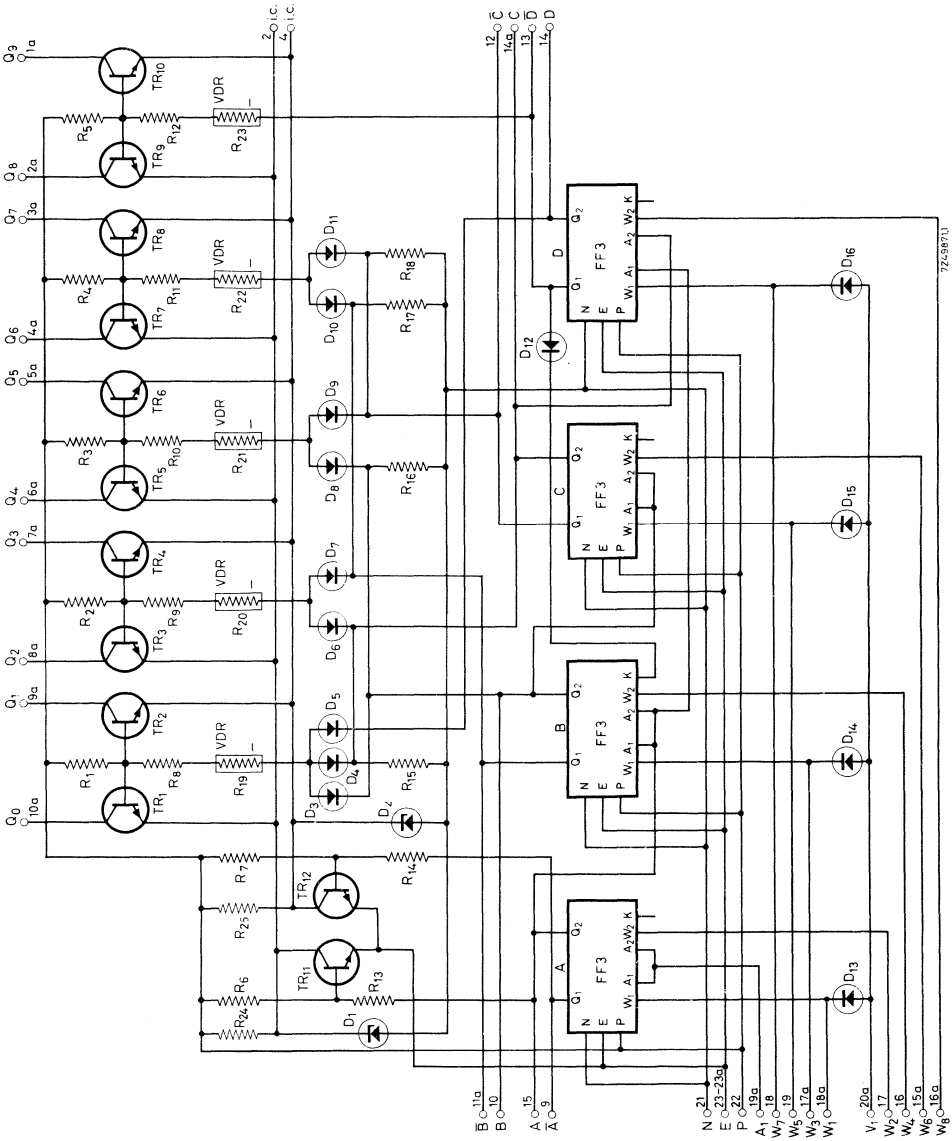

RZ 22603-6

This assembly contains one decade counter together with the decoding and driving circuits for the numerical indicator tubes ZM 1000, ZM 1020, ZM 1040 or ZM 1080, mounted on a printed-wiring board.
The counter consists of four flip-flops FF 3 (catalog number 2722 001 00021), connected to operate in the 1-2-4-8 code. The flip-flops can be reset by means of a common positive signal; the reset diodes $D_1$ up to and including $D_4$ are mounted on the printed-wiring board as well.

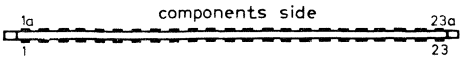
The printed-wiring board, provided with plated-through holes and double-sided goldplated contacts, is made of glass-epoxy material.
With the mating connector, catalog number 2422 020 52591, (not supplied with the DCA3), this printed-wiring board of standard dimensions (121.8 mm x 180.3 mm x 1.6 mm), can be used directly in the standard mounting chassis (catalog number 4322 026 38240).
The circuit blocks FF 3 are secured to the printed-wiring board by means of locking tags (catalog number 4322 026 33690).

| | | |
|---|---|---|
| Pulse repetition frequency range | : | 0 - 100 kHz |
| Ambient-temperature range | : | -20 to +60 °C |
| Weight | : | approx. 150 g |

CIRCUIT DATA



Terminals




1 = not connected
2 = internal connection
3 = not connected
4 = internal connection
5 = not connected
6 = not connected
7 = not connected
8 = not connected
9 = $\overline{A}$ = $Q_{1A}$ = output 1 flip-flop A
10 = B = $Q_{2B}$ = output 2 flip-flop B
11 = not connected
12 = $\overline{C}$ = $Q_{1C}$ = output 1 flip-flop C
13 = $\overline{D}$ = $Q_{1D}$ = output 1 flip-flop D
14 = D = $Q_{2D}$ = output 2 flip-flop D
15 = A = $Q_{2A}$ = output 2 flip-flop A
16 = $W_4$ = $W_2$ of flip-flop B
17 = $W_2$ = $W_2$ of flip-flop A
18 = $W_7$ = $W_1$ of flip-flop D
19 = $W_5$ = $W_1$ of flip-flop C
20 = not connected
21 = N = common negative supply −6 V
22 = P = common positive supply +6 V
23 = E = common supply 0 V

1a = $Q_9$ = digit number 9
2a = $Q_8$ = digit number 8
3a = $Q_7$ = digit number 7
4a = $Q_6$ = digit number 6
5a = $Q_5$ = digit number 5
6a = $Q_4$ = digit number 4
7a = $Q_3$ = digit number 3
8a = $Q_2$ = digit number 2
9a = $Q_1$ = digit number 1
10a = $Q_o$ = digit number 0
11a = $\overline{B}$ = $Q_{1B}$ = output 1 flip-flop B
12a = not connected
13a = not connected
14a = C = $Q_{2C}$ = output 2 flip-flop C
15a = $W_6$ = $W_2$ of flip-flop C
16a = $W_8$ = $W_2$ of flip-flop D
17a = $W_3$ = $W_1$ of flip-flop B
18a = $W_1$ = $W_1$ of flip-flop A
19a = $A_1$ = a.c. input counter
20a = $V_1$ = reset input counter
21a = not connected
22a = not connected
23a = E = common supply 0 V

Power supply

Terminal 21 : $V_N = -6\ V \pm 5\ \%$, $-I_N = 42\ mA$
22 : $V_P = +6\ V \pm 5\ \%$, $I_P = 8.8\ mA$
} nominal value of the current
23 = 23A : $V_E = 0\ V$

Notes

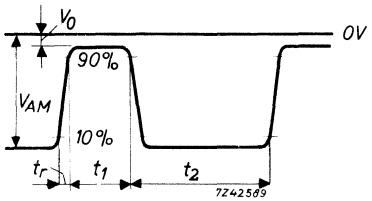
- The data given apply to the most adverse supply voltages for a combination of units, namely $V_N = -5.7\ V$ and $V_P = +5.7\ V$.
- The temperatures $-20\ ^oC$ and $+60\ ^oC$ and the tolerances on the supply voltages are absolute limiting values.
- When a current is flowing towards the unit, the positive sign is used.

INPUT DATA

Input signal requirements

Trigger input signal (terminal $A_1$)

A positive-going voltage step is applied to terminal $A_1$. This voltage step advances the counter one position.




| | | | |
|---|---|---|---|
| Voltage | $V_{AM}$ | = min. | $-0.7\ V_N$ |
| | | = max. | $-\ V_N$ |
| | $-V_0$ | = min. | 0 V |
| | | = max. | 0.2 V |
| Required direct current | $I_{A_1D}$ | = min. | 1.75 mA |
| Required current during the transient averaged over 0.4 µs | $I_{A_1T}$ | = min. | 6 mA |
| over 0.7 µs | | = min. | 4.5 mA |
| Rise time | $t_r$ | = max. | 0.7 µs |
| Pulse duration | $t_1$ | = min. | 1 µs |
| | $t_2$ | = min. | 8 µs |

Reset input signal (terminal $V_1$)

For resetting the counter a positive d.c. voltage is applied to terminal $V_1$. This signal causes all terminals $Q_1$ to reach a "negative high" and all terminals $Q_2$ to reach a "negative low" level.

Input level during reset

| | | | |
|---|---|---|---|
| Voltage | $V_{V_1}$ | = min. | 1 V |
| | | = max. | 10 V |
| Current | $I_{V_1}$ | = min. | 3.6 mA |

During counting it is recommended that terminal $V_1$ is connected to a voltage level.

| | | | |
|---|---|---|---|
| Voltage | $-V_{V_1}$ | = min. | 0.4 V |
| | | = max. | 10 V |
| Current | $-I_{V_1}$ | = min. | 0.12 mA (at $-V_{V_1}$ = 0.4 V) |

D.C. input (terminals W)

A d.c. voltage level is applied to terminals $W_1$ up to and including $W_8$. A positive voltage drives the corresponding transistor into the non-conducting state and a negative voltage drives the transistor into the conducting state.

Transistor conducting

| | | | |
|---|---|---|---|
| Current | $-I_W$ | = min. | 0.6 mA ($-V_W$ = max. 0.4 V) |
| | | = max. | 15 mA |

Transistor non-conducting

| | | | |
|---|---|---|---|
| Voltage | $V_W$ | = min. | 0.2 V |
| | | = max. | 10 V |
| Current | $I_W$ | = min. | 0.9 mA |

OUTPUT DATA

Decade counter section

The outputs of the counter (A, $\overline{A}$, B, $\overline{B}$, etc.) may furthermore be loaded with two gate invertors GI or two negative AND-gates. Output D of the last flip-flop is then still capable to drive a next decade.
A, B, C and D are the outputs of the flip-flops which are at 0 V level, when the decade is set on digit number 0.

Output transistor conducting

Voltage $-V_Q$ = min. 0 V, max. 0.2 V

| | | A | $\overline{A}$ | B | $\overline{B}$ | C | $\overline{C}$ | D | $\overline{D}$ |
|---|---|---|---|---|---|---|---|---|---|
| Available direct current (in mA) | $-I_{QD}$ = | 3.4 | 6 | 2.15 | 3.9 | 3 | 3.9 | 6 | 5.1 |
| Available transient current averaged over 0.7 $\mu$s (in mA) | $-I_{QT}$ = | 9 | 14 | 8.4 | 12.9 | 8.9 | 12.9 | 14 | 14 |

Output transistor non-conducting

Voltage $-V_Q$ = min. 0.7 $V_N$, max. $V_N$

| | | A | $\overline{A}$ | B | $\overline{B}$ | C | $\overline{C}$ | D | $\overline{D}$ |
|---|---|---|---|---|---|---|---|---|---|
| Available direct current (in mA) | $I_{QD}$ = | 0.1 | 0.13 | 0.1 | 0.1 | 0.1 | 0.1 | 0.13 | 0.1 |

Numerical indicator tube driver

The outputs $Q_0$ (terminal 10a) up to and including $Q_9$ (terminal 1a) have to be connected to the pins $k_0$ up to and including $k_9$ of the numerical indicator tube ZM 1000, ZM 1020, ZM 1040 or ZM 1080.
The anode of these tubes has to be connected via a resistor $R_a$ to the high voltage power supply $V_b$.

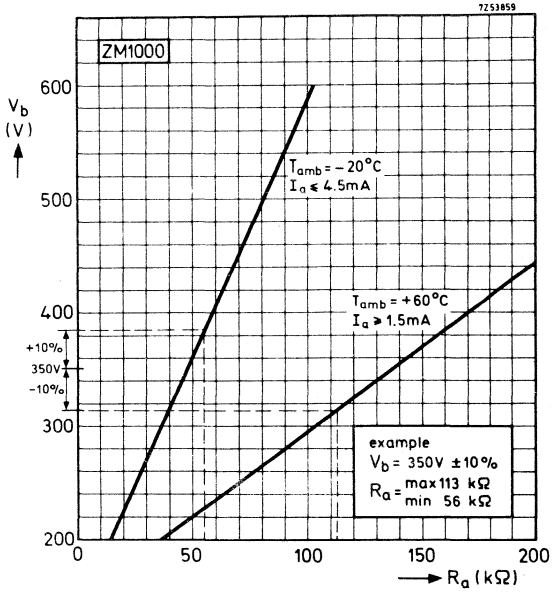
Output transistor conducting

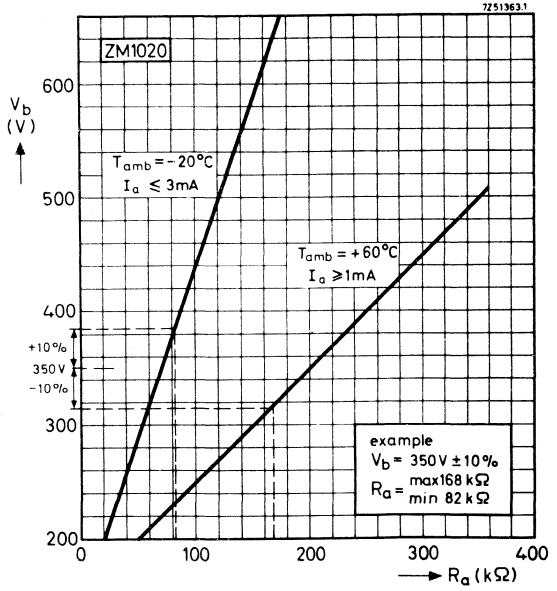
Voltage $V_Q$ = max. 3.2 V

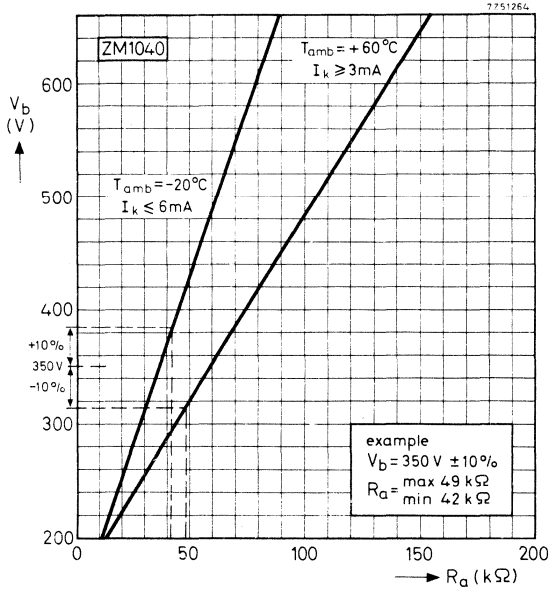
Current $I_Q$ = max. 6 mA

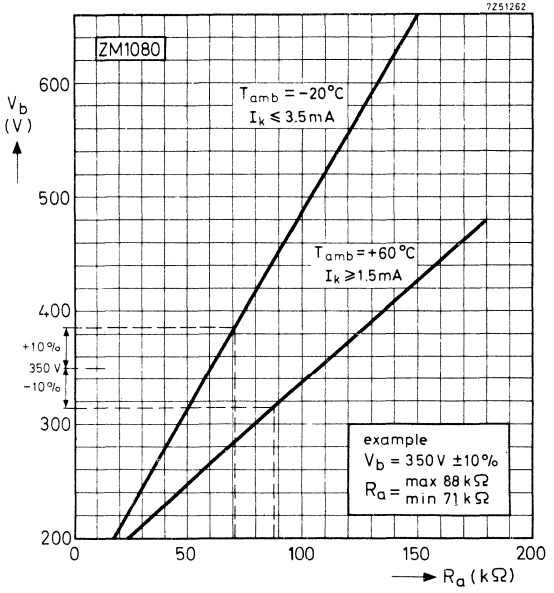
The available output current ($I_Q$) of the ten numerical outputs $Q_0$ up to and including $Q_9$ is sufficient to deliver the required current for the numerical indicator tube ZM 1000, ZM 1020, ZM 1040 or ZM 1080.

The relation between the permitted value and tolerances of the high voltage supply $V_b$ and the corresponding anode series resistor $R_a$ for the various indicator tubes over the whole temperature range is given in the following graphs.


7Z53859
ZM1000
$V_b$ (V)
600
500
400
300
200
+10%
350V
-10%
$T_{amb} = -20°C$
$I_a \leq 4.5mA$
$T_{amb} = +60°C$
$I_a \geq 1.5mA$
example
$V_b$ = 350V ±10%
$R_a$ = max 113 kΩ
min 56 kΩ
0
50
100
150
200
$R_a$ (kΩ)

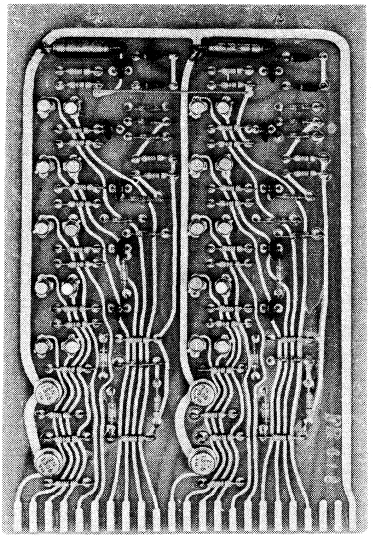

7Z51363.1
ZM1020
$V_b$ (V)
600
500
400
300
200
+10%
350V
-10%
$T_{amb} = -20°C$
$I_a \leq 3mA$
$T_{amb} = +60°C$
$I_a \geq 1mA$
example
$V_b$ = 350V ±10%
$R_a$ = max 168 kΩ
min 82 kΩ
0
100
200
300
400
$R_a$ (kΩ)




Wiring capacitance at each Q-output: max. 500 pF

# DUAL NUMERICAL INDICATOR TUBE DRIVER ASSEMBLY



RZ 22603-8

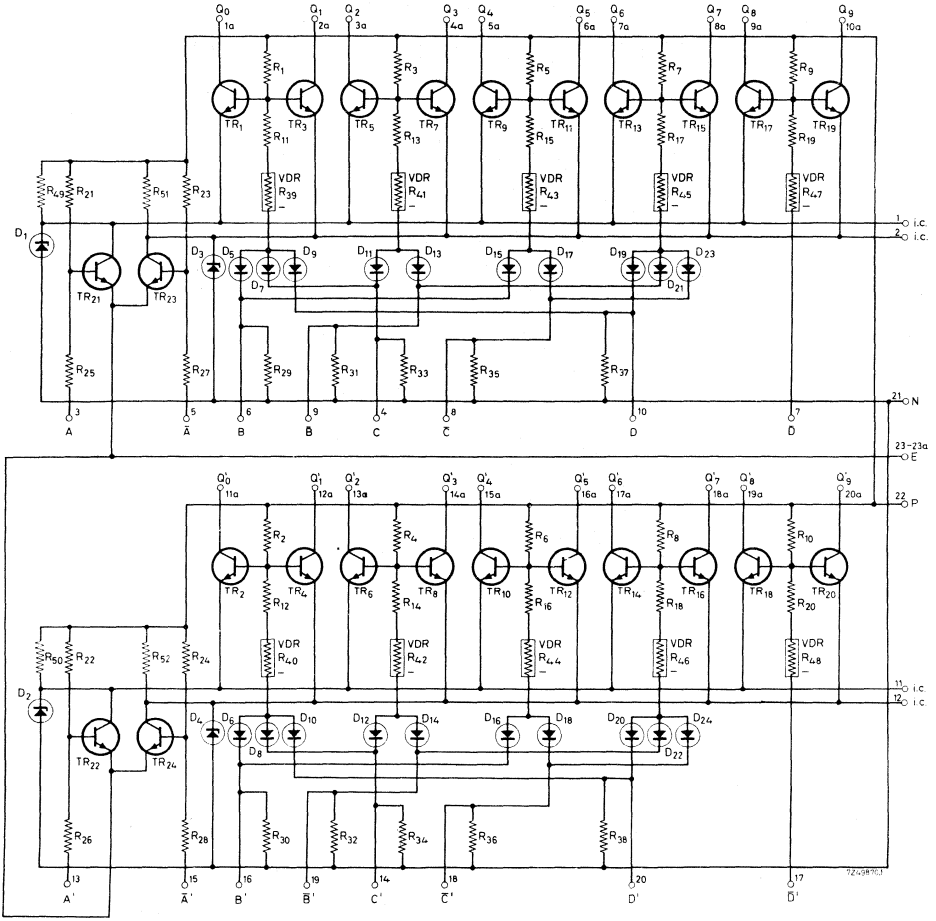
This assembly contains two BCD-to-decimal decoding and driving circuits for the numerical indicator tubes ZM 1000, ZM 1020, ZM 1040 or ZM 1080, mounted on a printed-wiring board.
The 2.ID 1 has been designed to operate in conjunction with decade counters in the 1-2-4-2 (jump at 8) or 1-2-4-8 code, e.g. the dual decade counter assembly 2.DCA 2 (catalog number 2722 009 00011).

The inputs A, $\overline{A}$, B, $\overline{B}$, C, $\overline{C}$, D, $\overline{D}$ and A', $\overline{A'}$, B', $\overline{B'}$, C', $\overline{C'}$, D', $\overline{D'}$ have to be connected to the corresponding outputs of the four flip-flops of the decade counter.
The inputs A, B, C, D and A', B', C', D' have to be at the "0" level for the digit number 0 to be indicated.

The printed-wiring board, provided with plated-through holes and double-sided goldplated contacts, is made of glass-epoxy material. With the mating connector (catalog number 2422 020 52591), not supplied with the 2.ID 1, this printed-wiring board of standard dimensions (121.8 mm x 180.3 mm x 1.6 mm) can be used directly in the standard mounting chassis (catalog number 4322 026 38240).

| | |
|---|---|
| Ambient-temperature range: | −20 to +60 °C |
| Weight | approx. 100 g |

CIRCUIT DATA




Terminals

1 = internal connection
2 = internal connection
3 = A = to be connected to output Q of first flip-flop
4 = C = to be connected to output Q of third flip-flop
5 = $\overline{A}$ = to be connected to output $\overline{Q}$ of first flip-flop
6 = B = to be connected to output Q of second flip-flop
7 = $\overline{D}$ = to be connected to output $\overline{Q}$ of fourth flip-flop
8 = $\overline{C}$ = to be connected to output $\overline{Q}$ of third flip flop
9 = $\overline{B}$ = to be connected to output $\overline{Q}$ of second flip-flop
10 = D = to be connected to output Q of fourth flip-flop

} decade counter 1

11 = internal connection
12 = internal connection
13 = A' = to be connected to output Q of first flip-flop
14 = C' = to be connected to output Q of third flip-flop
15 = $\overline{A'}$ = to be connected to output $\overline{Q}$ of first flip-flop
16 = B' = to be connected to output Q of second flip-flop
17 = $\overline{D'}$ = to be connected to output $\overline{Q}$ of fourth flip-flop
18 = $\overline{C'}$ = to be connected to output $\overline{Q}$ of third flip-flop
19 = $\overline{B'}$ = to be connected to output $\overline{Q}$ of second flip-flop
20 = D' = to be connected to output Q of fourth flip-flop
} decade counter 2
21 = N = common negative supply −6 V
22 = P = common positive supply +6 V
23 = 23a = E = common supply 0 V

1a up to and including 10a = numerical outputs $Q_0$ up to and including $Q_9$ to drive numerical indicator tube 1

11a up to and including 20a = numerical outputs $Q'_0$ up to and including $Q'_9$ to drive numerical indicator tube 2

Power supply

Terminal 21 : $V_N = -6\ V \pm 5\%$, $-I_N = 8.5\ mA$
22 : $V_P = +6\ V \pm 5\%$, $I_P = 7\ mA$
23 : $V_E = 0\ V$ common
} nominal value of the current required for one ID 1

Notes

- The data given apply to the most adverse supply voltages for a combination of units, namely: $V_N = -5.7\ V$ and $V_P = +6.3\ V$
- The temperatures −20 °C and +60 °C and the tolerances on the supply voltages are absolute limiting values.
- When a current is flowing towards the unit, the positive sign is used.

INPUT DATA

Input signal requirements (terminals A, $\overline{A}$, A', $\overline{A'}$, etc.)

Input at "0" level

Voltage $-V_I$ = min. 0 V
= max. 0.2 V

| | | A, A', $\overline{A}$, $\overline{A'}$ | B, B', $\overline{B}$, $\overline{B'}$, C, C', $\overline{C}$, $\overline{C'}$, D, D' | $\overline{D}$, $\overline{D'}$ |
|---|---|---|---|---|
| Required direct current | $I_I$ | 0 mA | 2.1 mA | 0 mA |
| Required transient current | $I_{QT}$ | 0 mA | 1.1 mA | 0 mA |

Input at negative high level

Voltage $-V_I$ = min. 0.7 $V_N$
= max. $V_N$

| | A, A', $\overline{A}$, $\overline{A'}$ | B, B', $\overline{B}$, $\overline{B'}$, C, C', $\overline{C}$, $\overline{C'}$, D, D' $\overline{D}$, $\overline{D'}$ |
|---|---|---|
| Required direct current $-I_I$ | 0.57 mA | 0.6 mA |

Input impedance: equivalent to a capacitance of approx. 150 pF

Operational data

- When an ID 1 is driven from a decade counter with flip-flops operating in the 1-2-4-8 code, these flip-flops may be additionally loaded with two negative AND-gates, or with two GI's if the decade counter is equipped with FF 3 flip-flops, or with one GI if the decade counter is equipped with FF 1 flip-flops. Output D of the last flip-flop is capable of driving a following decade counter.
- A, B, C, D and A', B', C', D' must be connected to the outputs of the flip-flops which are at "0" level, when the decade counter is set on digit number 0.

OUTPUT DATA

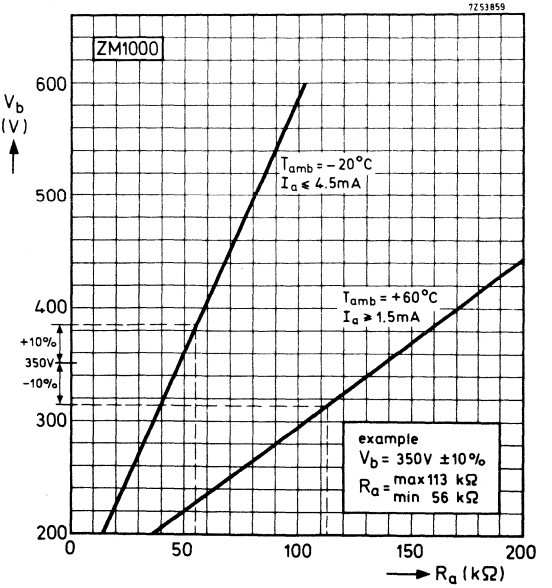
The outputs $Q_0$ up to and including $Q_9$ and $Q'_0$ up to and including $Q'_9$ have to be connected to the pins $k_0$ up to and including $k_9$ of the numerical indicator tube ZM 1000, ZM 1020, ZM 1040 or ZM 1080.
The anode of these tubes has to be connected via a resistor $R_a$ to the high voltage power supply $V_b$.

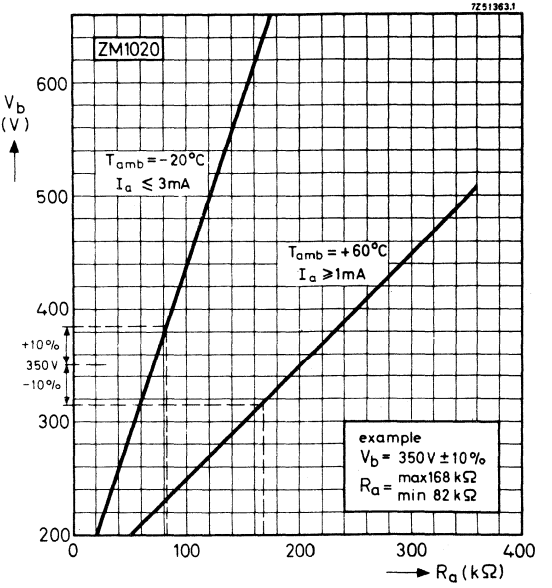
Output transistor conducting

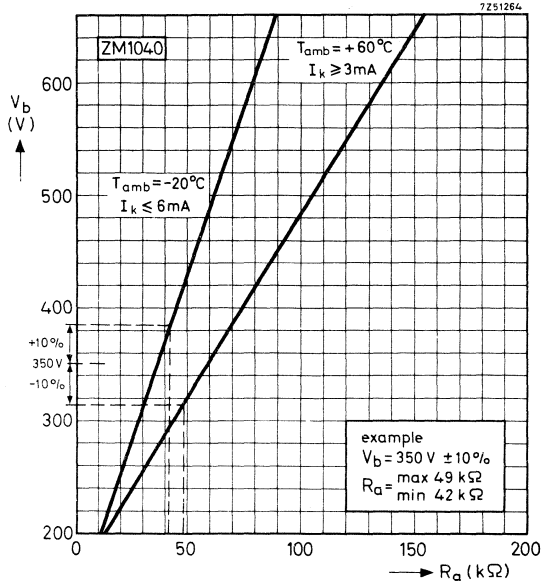
Voltage $V_Q$ = max. 3.2 V

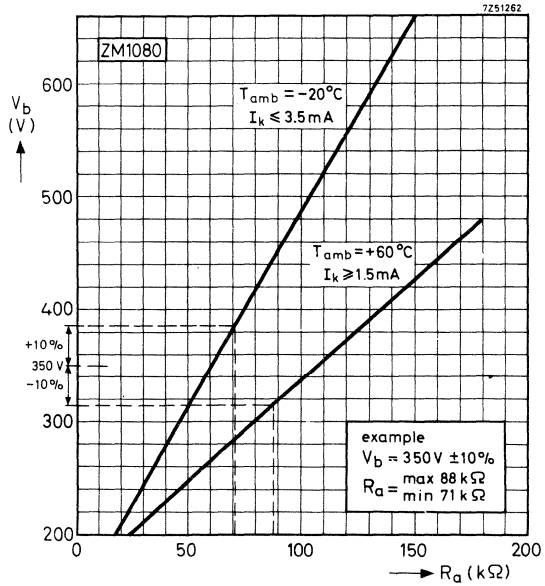
Current $I_Q$ = max. 6 mA

The available output current ($I_Q$) of the ten numerical outputs $Q_0$ (terminal 1a and 11a) up to and including $Q_9$ (terminal 10a and 20a) is sufficient to deliver the required current for the numerical indicator tube ZM 1000, ZM 1020, ZM 1040 or ZM 1080.
The relation between the permitted value and tolerances of the high voltage supply $V_b$ and the corresponding anode series resistor $R_a$ for the various indicator tubes over the whole temperature range is given in the following graphs.


7Z53859
ZM1000
$V_b$ (V)
600
500
400
300
200
+10%
350V
-10%
$T_{amb}$ = -20°C
$I_a \leq$ 4.5mA
$T_{amb}$ = +60°C
$I_a \geq$ 1.5mA
example
$V_b$ = 350V ±10%
$R_a$ = max 113 kΩ
min 56 kΩ
0
50
100
150
200
$R_a$ (kΩ)


7Z51363.1
ZM1020
$V_b$ (V)
600
500
400
300
200
+10%
350V
-10%
$T_{amb}$ = -20°C
$I_a \leq$ 3mA
$T_{amb}$ = +60°C
$I_a \geq$ 1mA
example
$V_b$ = 350V ±10%
$R_a$ = max 168 kΩ
min 82 kΩ
0
100
200
300
400
$R_a$ (kΩ)

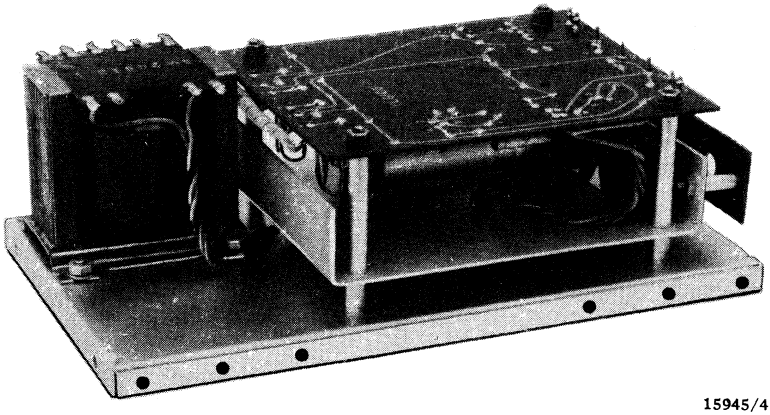



Wiring capacitance at each Q-output: max. 500 pF

# ACCESSORIES FOR CIRCUIT BLOCKS
# 100 kHz SERIES

# POWER SUPPLY UNIT



15945/4

| | |
|---|---|
| Input voltage | 220 $V_{ac}$ and 235 $V_{ac}$ |
| Output voltage | +6 $V_{dc}$ and −6 $V_{dc}$ |

APPLICATION

This power supply unit has been designed for use with the circuit blocks of the 100 kHz- and the 1-series. However, it is also suitable as a supply for other transistorised circuits.

CONSTRUCTION

The unit is dimensioned for mounting in the standardized 19" chassis. The power supply unit fits in chassis 4322 026 38240; the base plate of the unit then replaces a side plate of the chassis. The supply unit occupies the same space as four printed-wiring boards.

| | |
|---|---|
| Dimensions | 215 x 125 x 70 mm |
| Weight | 1.5 kg |

TECHNICAL PERFORMANCE

| | | |
|---|---|---|
| Input voltage | 220 $V_{ac}$ +10 %, −15 % | |
| | 235 $V_{ac}$ +10 %, −15 % | |
| Frequency | 50 to 60 | Hz |
| Fusing | 1 A fuse in the 220 V winding only | |

−6 V output [1])

| | | |
|---|---|---|
| Output voltage | 6 V, adjustable ±3 % (R5, see diagram) | |
| Output current | 600 | mA |
| Stability ratio at 220 V | 450:1 | |
| Ripple voltage | 50 | $mV_{rms}$ |
| Output resistance | 0.3 | Ω |
| Output impedance at 10 kHz | 0.2 | Ω |
| Temperature coefficient | −3 | mV/deg C |

+6 V output [1])

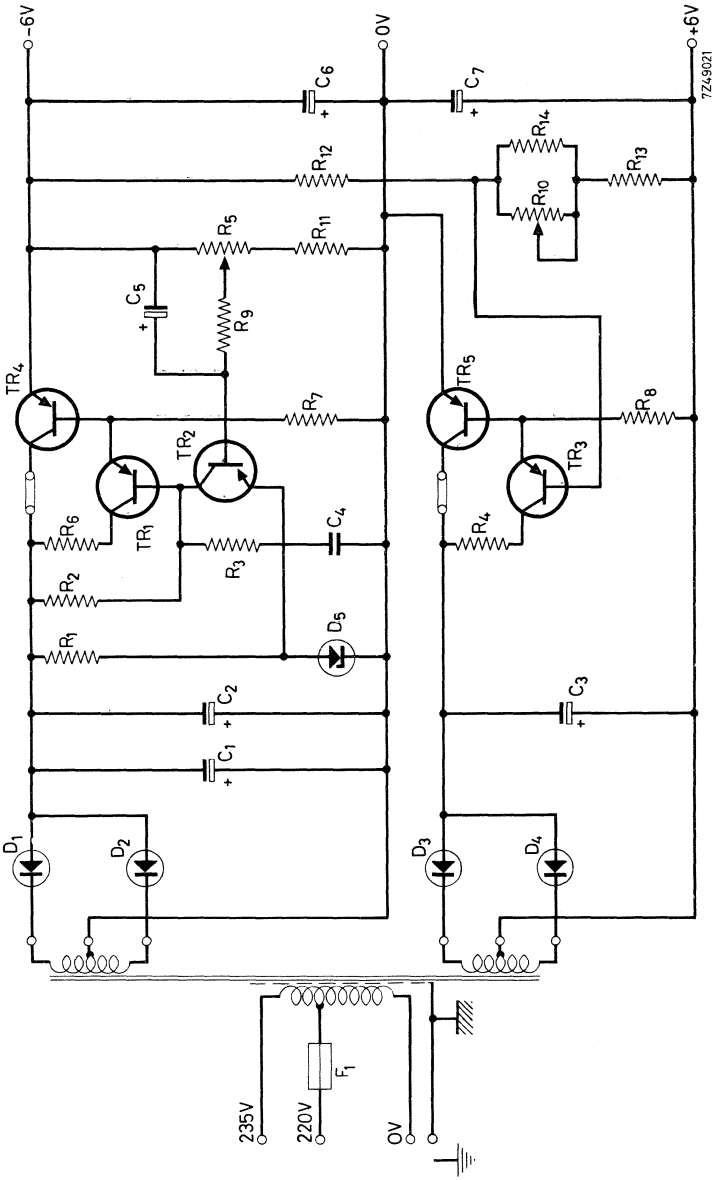
| | | |
|---|---|---|
| Output voltage | 6 V, adjustable ±3 % (R10, see diagram) | |
| Output current | 150 | mA |
| Stability ratio at 220 V | 360:1 | |
| Ripple voltage | 50 | $mV_{rms}$ |
| Output resistance | 1.5 | Ω |
| Output impedance at 10 kHz | 0.5 | Ω |
| Temperature coefficient | +6 | mV/deg C |

| | | |
|---|---|---|
| Operating-temperature range | −20 to +60 | °C |
| Storage-temperature range | −20 to +75 | °C |

In systems requiring more than one power supply unit, the earth tags (marked "0 V") may be interconnected, the positive tags (marked "+6 V") and the negative tags (marked "−6 V") must remain strictly separated.

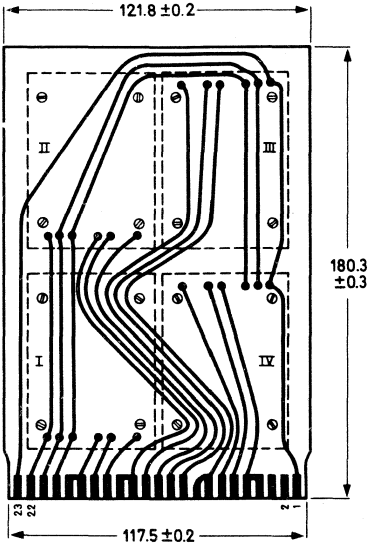
When a system is put into operation for the first time, the output voltages of the power supply units have to be adjusted to 6 V under nominal system load.

1) All values are given for full load.


-6V
0V
+6V
7Z49021
C6
C7
R14
R12
R10
R13
R5
R11
C5
R9
TR4
R7
TR5
R8
TR2
TR3
TR1
R6
C4
R4
R2
R3
D5
R1
C2
C3
C1
D1
D2
D3
D4
F1
235V
220V
0V

# PRINTED-WIRING BOARD FOR FOUR UNITS PA 1

This printed-wiring board fits the mounting chassis 4322 026 38240. It can be used directly with the aid of the mating connector 2422 020 52592. On this board up to four PA 1's can be mounted, the next position in the chassis being left empty.




Terminal location:

1 = E = common supply 0 V (interconnected to terminal 1)

2 = not connected

3 = not connected

4 = $N_2$, 5 = $N_2$ } supply max. 60 V

6 = Q = output PA 1

7 = W = input PA 1

} unit nr. IV

8 = $N_2$, 9 = $N_2$ } supply max. 60 V

10 = Q = output PA 1

11 = W = input PA 1

} unit nr. III

12 = W = input PA 1

13 = Q = output PA 1

14 = $N_2$, 15 = $N_2$ } supply max. 60 V

} unit nr. II

16 = W = input PA 1

17 = Q = output PA 1

18 = $N_2$, 19 = $N_2$ } supply max. 60 V

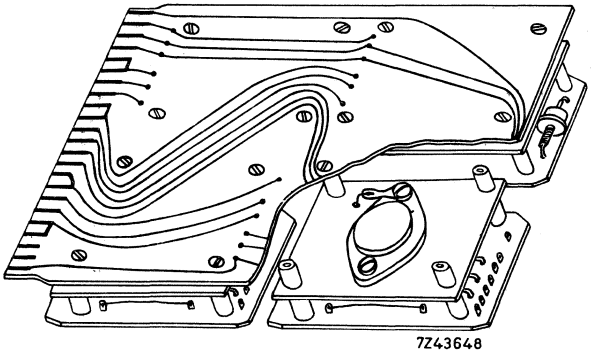
} unit nr. I

20 = $N_1$ = common supply −6 V

21 = P = common supply +6 V

22 = E = common supply 0 V

23 = E = common supply 0 V




| | |
|---|---|
| Material | glass epoxy with plated-through holes |
| Hole diameter | 1.2 mm |
| Contacts | 1 x 23, gold plated, pitch 0.2 inch |

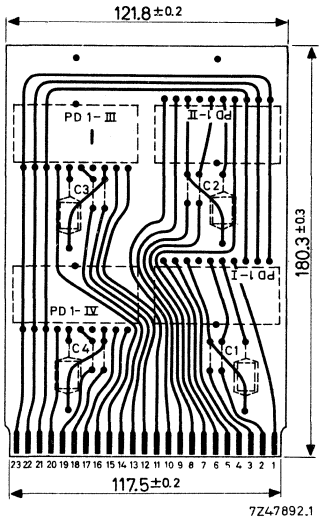
# PRINTED-WIRING BOARD FOR FOUR UNITS PD 1

This printed-wiring board with standard dimensions 121.8 mm x 180.3 mm x 1.6 mm (4.8" x 7.1" x 0.0625") is intended to accomplish the mounting of maximum four pulse driver units PD 1 (catalog number 2722 001 13011).

One printed-wiring board PDA 1 with four units PD 1 mounted on it, can be used in conjunction with three reversible counters BCA 1 (catalog number 2722 009 00021).
Two units PD 1 perform shift-pulse amplifying functions between two reversible counters BCA 1, one for the forward and one for the reverse direction.

The printed-wiring board is provided with two wire jumpers for each PD 1. In case the number of trigger- and gate-inputs has to be extended, these wire jumpers can be replaced by diodes, type OA 95. The required connections with the EG- and K-terminals of the PD 1 have already been made in the print pattern.
Furthermore the printed-wiring board is provided with two plated-through holes for each unit PD 1. In case the output-pulse duration of the PD 1 has to be increased, these holes can be used for mounting the required capacitor. The terminals of this capacitor are then directly connected to the K- and L-terminals of the concerning PD 1.

Holes are provided to secure the PD 1 rigidly to the board by means of the locking tag 4322 026 33690.
With the mating connector 2422 020 52592 the printed-wiring board can be used directly in the mounting chassis 4322 026 38240.




Terminal location:

1 = $Q_1$ = output PD 1-I
2 = $EG_1$ = extension gate input PD 1-I
3 = $K_1$ = extension trigger input PD 1-I
4 = $G_1$ = gate input PD 1-I
5 = $A_1$ = trigger input PD 1-I
6 = $Q_2$ = output PD 1-II
7 = $EG_2$ = extension gate input PD 1-II
8 = $K_2$ = extension trigger input PD 1-II
9 = $G_2$ = gate input PD 1-II
10 = $A_2$ = trigger input PD 1-II
11 = $A_3$ = trigger input PD 1-III
12 = $G_3$ = gate input PD 1-III
13 = $K_3$ = extension trigger input PD 1-III
14 = $EG_3$ = extension gate input PD 1-III
15 = $Q_3$ = output PD 1-III
16 = $A_4$ = trigger input PD 1-IV
17 = $G_4$ = gate input PD 1-IV
18 = $K_4$ = extension trigger input PD 1-IV
19 = $EG_4$ = extension gate input PD 1-IV
20 = $Q_4$ = output PD 1-IV
21 = N = common supply −6 V
22 = P = common supply +6 V
23 = E = common supply 0 V

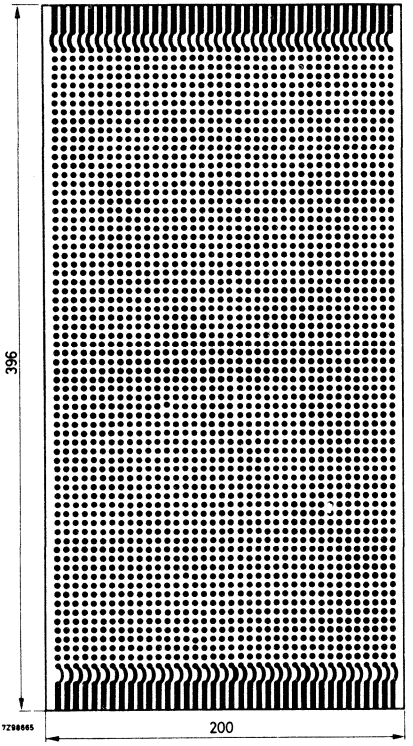
| | |
|---|---|
| Material | glass epoxy with plated-through holes |
| Hole diameter | 1.2 mm |
| Contacts | 1 x 23, gold plated, pitch 0.2 inch |

INPUT AND OUTPUT DATA

See specification of pulse driver unit PD 1 (catalog number 2722 001 13011)

# EXPERIMENTERS' PRINTED—WIRING BOARDS

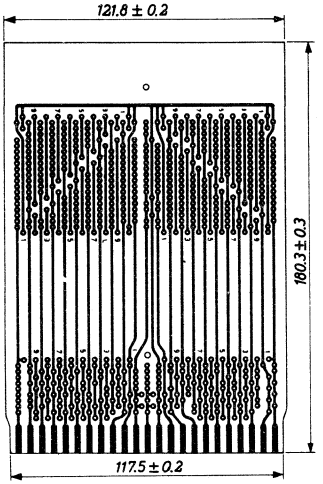
These experimenters' printed-wiring boards are very suitable for circuit blocks of the 100 kHz- and 1-Series.




| | | |
|---|---|---|
| Material | copper-clad phenolic resin bonded paper | |
| Grid pitch | 5.08 mm (0.2 inch) | |
| Contacts | gold plated, pitch 0.2 inch | |
| | single sided<br>2 x 38 | double sided<br>4 x 38 |
| Holes | with holes | – |
| Catalogue number | 4322 026 34900 | 4322 026 34910 |

# PRINTED-WIRING BOARD

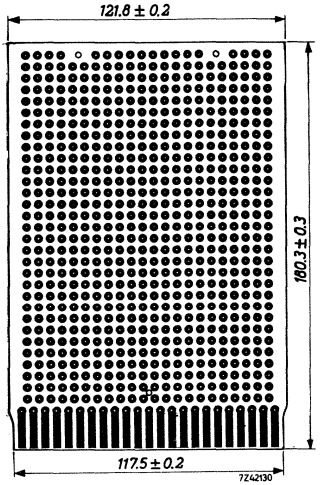
This printed-wiring board is intended for mounting circuit blocks of the 100 kHz- and 1-Series.
It fits the mounting chassis 4322 026 38240.




| | |
|---|---|
| Material | copper-clad phenolic resin bonded paper with punched holes |
| Hole diameter | 1.3 mm |
| Contacts | 1 x 23, gold plated, pitch 0.2 inch |

# EXPERIMENTERS' PRINTED–WIRING BOARD

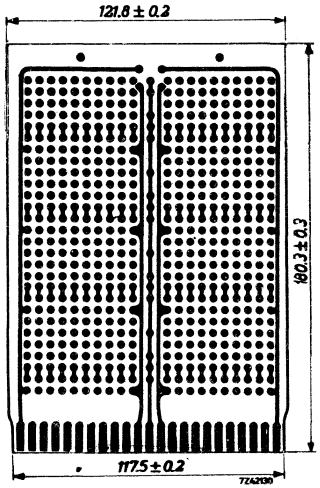
This experimenters' printed-wiring board is very suitable for circuit blocks of the 100 kHz- and 1-Series.
It fits the mounting chassis 4322 026 38240.




| | |
|---|---|
| Material | copper-clad phenolic resin bonded paper with punched holes |
| Grid pitch | 5.08 mm (0.2 inch) |
| Hole diameter | 1.3 mm |
| Contacts | 1 x 23, gold plated, pitch 0.2 inch |

# PRINTED—WIRING BOARD

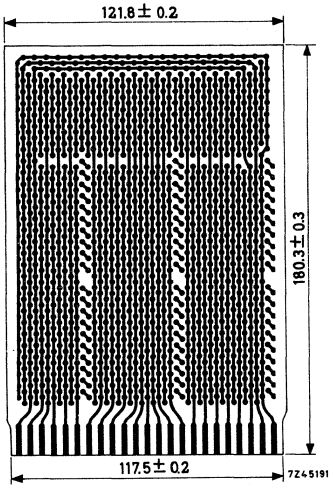
This printed-wiring board for 100 kHz- and 1-Series circuit blocks can accommodate 8 horizontally mounted blocks. Combination of circuit blocks with discrete components is easily possible on this board.
It fits the mounting chassis 4322 026 38240.




| | |
|---|---|
| Material | copper-clad phenolic resin bonded paper with plated-through holes |
| Hole diameter | 1.2 mm |
| Contacts | 1 x 23, gold plated, pitch 0.2 inch |

# PRINTED-WIRING BOARD

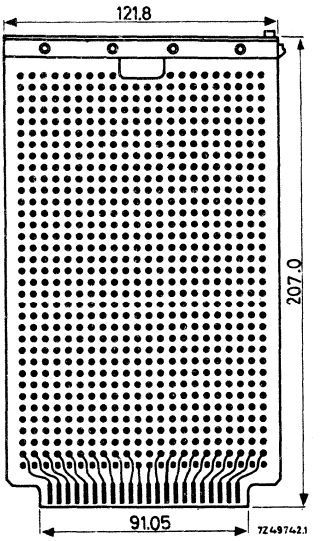
This printed-wiring board is intended for mounting circuit blocks of the 100 kHz- and 1-Series. It fits the mounting chassis 4322 026 38240.




| | |
|---|---|
| Material | copper-clad phenolic resin bonded paper with plated-through holes |
| Hole diameter | 1.2 mm |
| Contacts | 1 x 23, gold plated, pitch 0.2 inch |

# EXPERIMENTERS' PRINTED–WIRING BOARD

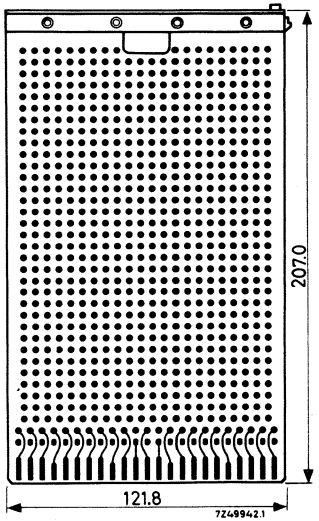
This experimenters' printed-wiring board (with extractor) is very suitable for circuit blocks of the 100 kHz- and 1-Series.
It fits the mounting chassis 4322 026 38230.




| | |
|---|---|
| Material | phenolic resin bonded paper with holes; on both sides are copper lands around each hole |
| Grid pitch | 5.08 mm (0.2 inch) |
| Hole diameter | 1.3 mm |
| Contacts | 2 x 22, gold plated, pitch 0.156 inch |

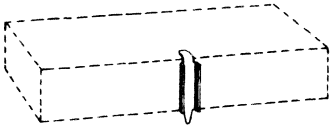
# EXPERIMENTERS' PRINTED-WIRING BOARDS

These experimenters' printed-wiring boards (with extractor) are very suitable for circuit blocks of the 100 kHz- and 1-Series.
They fit the mounting chassis 4322 026 38240.




| | | |
|---|---|---|
| Catalogue number | 4322 026 38630 | 4322 026 38690 |
| Material | phenolic resin bonded paper | glass epoxy |
| Grid pitch | 5.08 mm (0.2 inch) | |
| Holes | diameter 1.3 mm; on both sides of the board are copper lands around each hole | |
| Contacts | 2 x 23, gold plated, pitch 0.2 inch | |

# LOCKING TAG



Circuit blocks of the 100 kHz- and 1-Series mounted parallel to the printed-wiring board can be secured rigidly by means of this small tag, which permits soldering in a standard 1.3 mm diameter hole. The minimum supply quantity is 1000 pieces.

# STICKERS

These are drawing symbols of circuit blocks printed on self-adhesive, transparent material. They can be used for fast preparation of system drawings. The drawing symbols are as shown on the data sheets of the relevant circuit blocks.
The stickers are available in rolls, each containing 1000 drawing symbols of the same type of circuit block. Each sticker can be separately detached from the roll, without cutting.

| for circuit block of type | catalog number of a roll with 1000 stickers |
|---|---|
| FF 1 | 4322 026 35780 |
| FF 2 | 4322 026 35790 |
| FF 3 | 4322 026 35800 |
| FF 4 | 4322 026 35810 |
| 2.3.N 1 | 4322 026 35820 |
| 2.2.N 1 | 4322 026 35830 |
| 2.3.P 1 | 4322 026 35840 |
| 2.2.P 1 | 4322 026 35850 |
| 2.PL 1 | 4322 026 35860 |
| 2.PL 2 | 4322 026 35880 |
| EF 1/IA 1 | 4322 026 35890 |
| 2.EF 1 | 4322 026 35900 |
| 2.IA 1 | 4322 026 35910 |
| 2.EF 2 | 4322 026 35920 |
| 2.IA 2 | 4322 026 35930 |
| 2.GI 1 | 4322 026 34620 |
| PS 1 | 4322 026 35950 |
| PS 2 | 4322 026 36820 |
| PR 1 | 4322 026 36830 |
| OS 1 | 4322 026 35960 |
| OS 2 | 4322 026 35980 |
| PD 1 | 4322 026 30710 |
| PA 1 | 4322 026 07760 |

# Circuit blocks

# 1-Series

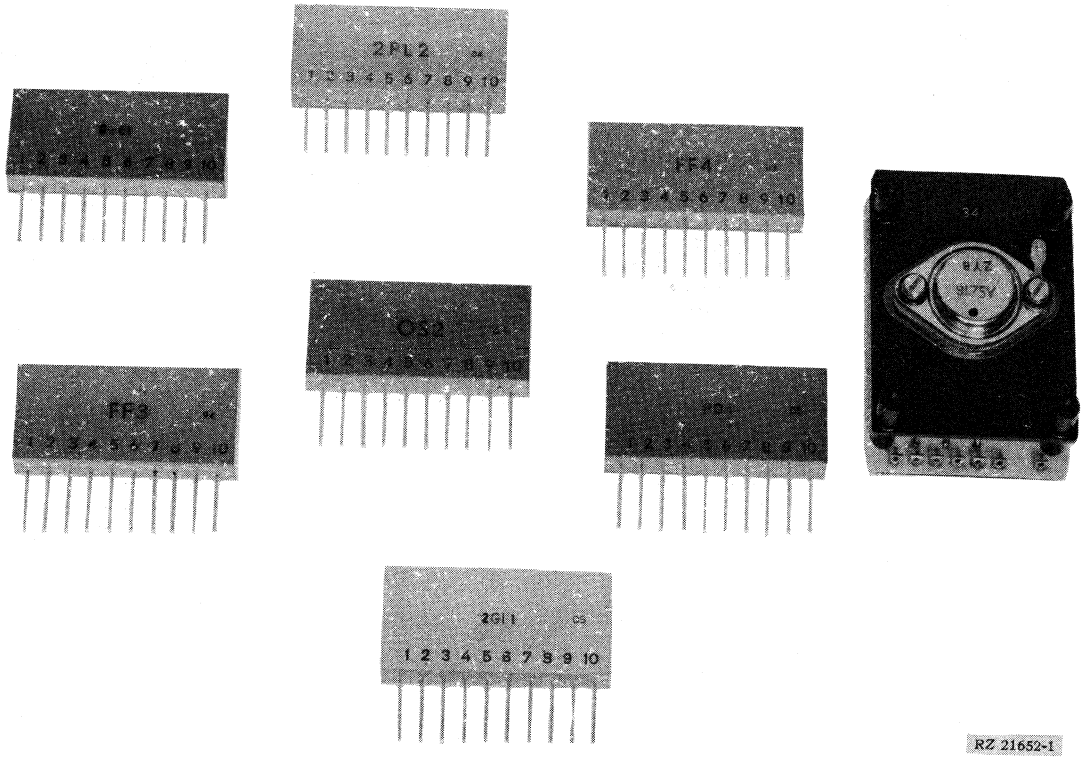
# INTRODUCTION

The 1-Series of circuit blocks presents a range of logic circuits to be applied in general purpose and special purpose data handling systems as well as for industrial measuring and instrumentation.
The 1-Series offers a complete range consisting of various logic elements together with all necessary auxiliary units including one-shot multivibrator, input and output devices, pulse shapers, etc.
Frequently occurring functions such as counters, shift registers, numerical indicator tube drivers, etc. can be supplied ready made, assembled on printed-wiring boards.
In this series the following units and assembled panels are available:

| description | colour | abbreviation | catalog number | page |
|---|---|---|---|---|
| Flip-flop | red | FF3 | 2722 001 00021 | B15 |
| Flip-flop | red | FF4 | 2722 001 00031 | B19 |
| Dual negative gate | orange | 2.3N1 | 2722 001 01001 | B23 |
| Dual negative gate | orange | 2.2N1 | 2722 001 01011 | B25 |
| Dual pulse logic | orange | 2.PL2 | 2722 001 03011 | B27 |
| Dual gate inverter | yellow | 2.GI1 | 2722 001 08001 | B31 |
| Pulse shaper | green | PS2 | 2722 001 11011 | B49 |
| Positive reset unit | blue | PR1 | 2722 001 22001 | B55 |
| One-shot multivibrator | green | OS2 | 2722 001 10011 | B59 |
| Pulse driver | green | PD1 | 2722 001 13011 | B65 |
| Printed-wiring board | | PDA1 | 4322 026 34710 | B109 |
| Power amplifier | | PA1 | 2722 032 00011 | B71 |
| Printed-wiring board | | PAA1 | 4322 026 33630 | B107 |
| Dual decade counter | | 2.DCA2 | 2722 009 00011 | B75 |
| Reversible counter | | BCA1 | 2722 009 00021 | B81 |
| Decade counter and numerical indicator tube driver assembly | | DCA3 | 2722 009 00031 | B87 |
| Dual numerical indicator tube driver assembly | | 2.ID1 | 2722 009 05001 | B95 |

Moreover all accessories for a quick and easy construction of equipment are available e.g. power supplies, printed-wiring boards, etc., see section "ACCESSORIES FOR CIRCUIT BLOCKS 1-SERIES".

In conjunction with 1-Series circuit blocks a number of static input and output devices can be used, see "INPUT/OUTPUT DEVICES".


2FL2
FF4
OS2
FF3
2GI1
RZ 21652-1

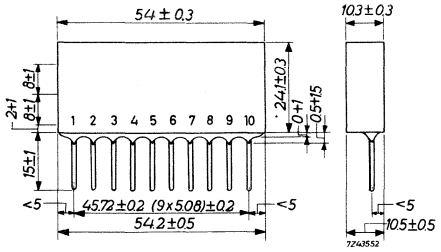
Easy-to-use loading table and simple loading rules, particularly for mixed loads, enables the system design to be completed quickly. Due to the fact that driven blocks only represent a load in the conducting state of the driving transistor, the required input d.c.- and transient currents of driven blocks are additive.

All circuits are compatible with little circuit diversity permitting simple and direct interconnections of the blocks within the range.

Input- and output currents of the blocks are designed in a way that external components are unnecessary with the exception of diodes.

The uniformity of the terminal location reduces the time for interwiring the blocks and facilitates the design of printed-wiring boards.

# CONSTRUCTION

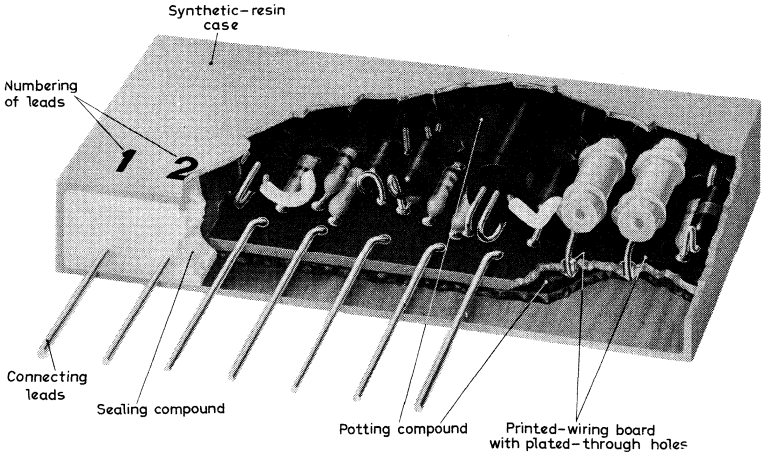



Weight:
approximately 20 g

Dimensional drawing of the circuit block

The dimensions of all 1-Series circuit blocks are approximately 54 mm x 24 mm x 11 mm. Out of one side of 54 mm x 11 mm emerge ten wire terminals of 0.7 mm diameter and 15 mm length. The distances between the wires are 5.08 mm (0.2 in) in accordance with the I.E.C. standard hole grid for printed-wiring boards.

The blocks are colour-coded, a different colour being used for each group of functions.




Cut-away view of a circuit block

The construction of a 1-Series circuit block can easily be seen in the cut-away view.

The electronic components, of which the circuit is made up (transistors, diodes, resistors, capacitors) are mounted on a printed-wiring board. This board is provided with plated-through holes to ensure reliable joints due to the large contact area of soldered contacts. The connecting leads are also mounted on the printed-wiring board.

Protection against mechanical shock and vibration is provided by the resilient potting compound, whilst atmospheric influences are excluded by the sealing compound, by which the synthetic resin case is hermetically closed.

For the sake of reference the connecting leads are numbered 1 to 10.

# CHARACTERISTICS

For all circuit blocks the following temperature range is specified:

| | |
|---|---|
| Operating | −20 to +60 °C |
| Storage | −25 to +75 °C |

The maximum pulse repetition frequency is 100 kHz for triggered logic applications.

The standard power supply voltages are

+6 V ±5 % ($V_p$) and −6 V ±5 % ($V_N$)

The power dissipation of the blocks is 20 to 100 mW.

Logic levels:

| | | |
|---|---|---|
| binary "1" | max. | $V_N$ |
| | min. | 0.7 $V_N$ |
| binary "0" | max. | −0.2 V |
| | min. | 0 V |

The general logic functions AND, OR, NOT and MEMORY can be performed with the two basic units of the range, viz. the gate inverter and the flip-flop respectively.

# TEST SPECIFICATIONS

Before and during manufacture samples of circuit blocks are regularly subjected to the following tests.

(1) Shock test and vibration test according to method 202A and 201A of MIL-STD-202, terminals tested on strength, tests on mounting, soldering, lacquer and coding.

(2) Corrosion test (salt haze), according to method 101A of MIL-STD-202 (condition B, 48 hours).

(3) Temperature cycling test, according to method 102A of MIL-STD-202 (5 cycles from $-25\ ^{o}C$ to $+65\ ^{o}C$).

(4) Dip test, according to method 104A of MIL-STD-202 (2 cycles $65\ ^{o}C/20\ ^{o}C$, condition B, NaCl).

(5) Accelerated humidity test, according to method 106A of MIL-STD-202 (10 cycles $65\ ^{o}C$).

(6) Long-term humidity test (units not operating), according to I.E.C. 68, C IV ($40\ ^{o}C$, relative humidity 90% to 95%, duration longer than 2000 hours, functional marginal measurements after 250, 1000 etc. hours).

(7) As item 6, but units operating under the most unfavourable electrical conditions.

(8) Long-term test at maximum temperature ($60\ ^{o}C$), units operating under the most unfavourable electrical conditions. Duration and measurements as item 6.

# INPUT AND OUTPUT DATA

INPUT DATA

| unit | terminal | note | d.c. current (mA) | transient load (mA) |
|---|---|---|---|---|
| FF3 | $A_1$ or $A_2$ | | 0.88 | 4.0 |
| | $A_1$ + $A_2$ | | 1.75 | 4.5 |
| | W | see note a | 0.9 | |
| FF4 | $G_1$ or $G_2$ | to open gate<br>gate open | <br>1.75 | 1.6 |
| | A | one gate closed<br>both gates closed | 1.75<br>1.75 | 4.5<br>1.0 |
| | W | see note a | 0.9 | |
| 2.PL2 | $G_1$ or $G_2$ | to open gate<br>gate open | <br>1.75 | 1.6 |
| | $A_1$ or $A_2$ | gate open<br>gate closed | 0.88<br>0.88 | 4.0<br>0.5 |
| 2.GI1 | EG | via diode OA95 | 1.0 | 3.0 |
| 2.2N1/ 2.3N1 | W | see note b | 0.52 | 0.37 |
| OS2 | A | | 1.3 | 1.4 |
| PD1 | A | | 1.7 | 1.5 |
| | G | to open gate<br>gate open | <br>1.75 | 1.2 |
| PR1 | W | | 0.1 | 0.08 |
| PS2 | W | | 0.7 | 0.75 |
| PA1 | W | | 2.5 | 1.3 |

Notes

a. Only to be driven by PR 1 via a diode OA 85/OA 95.

b. The input requirements also hold for the preset switches 1248 N (catalog number 4311 027 82221) and 1242 N (catalog number 4311 027 82211).

OUTPUT DATA

| unit | terminal | note | | d.c. current (mA) | transient load (mA) |
|---|---|---|---|---|---|
| FF3, FF4 | Q | | | 6 | 14 |
| GI 1 | Q | preceded by | AND | 15 | 9 |
| | | | AND - AND | 8 | 4.5 |
| | | | AND - OR | 8 | 4.5 |
| GI 1 - GI 1 | Q | preceded by | AND - AND | 25 | 22.5 |
| | | | AND - OR | 25 | 22.5 |
| | | connected as | set-reset FF | 9 | 9 |
| | | | non-inverting ampl. | 40 | 27 |
| | | | relay driver | 65 | |
| OS2 | $Q_1$ | | | 18 | 25 |
| | $Q_2$ | | | 6 | 21 |
| PD1 | Q | | | 65 | 90 |
| PS2 | Q | | | 20 | 13.7 |
| PR1 | Q | | | 15 | |
| | | terminals 3 and 4 interconnected | | 30 | |
| | | terminals 5 and 4 interconnected | | 40 | |
| PA1 | Q | | | 600 | |

Note

For driving the numerical indicator tubes ZM 1000, ZM 1020, ZM 1040 or ZM 1080 two assembled printed-wiring boards, 2.ID 1 and DCA 3, are available. The input requirements are specified in the individual sheets.

LOADING RULES

1. Verify that the sum of the required d.c. input currents of the driven units does not exceed the available d.c. output current of the driving unit.
2. When however, A-inputs are incorporated in the driven units, the transient loads must also be verified.
3. The verifications mentioned above hold for operations at the worst combination of supply voltage tolerances (6 V ±5 %) and ambient temperature between −20 °C and +60 °C.
4. W-inputs of FF3 and FF4 are to be used as extension inputs for the 2.PL2 and for positive-reset. For the latter purpose the positive reset unit PR1, designed for various loadings and driver circuits can be used.

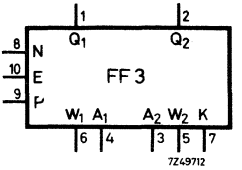
# FLIP-FLOP

Colour: red

The unit FF3 contains a transistor bi-stable multivibrator circuit. The transistors are medium-speed switching types.

The circuit constitutes a memory function when driven by means of a d.c. level or a positive-going trigger signal, and it can also be used as a binary scale-of-two when the trigger inputs are interconnected.

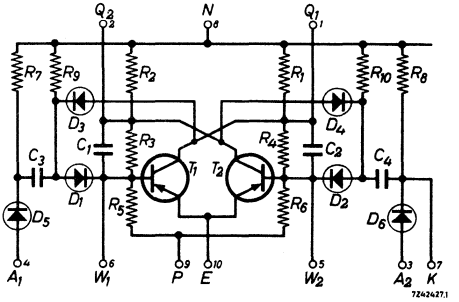
| | | |
|---|---|---|
| Frequency range | : | 0 - 100 kHz |
| Ambient temperature range: | | -20 to +60 °C |
| Weight | : | approx. 20 g |




Drawing symbol

## CIRCUIT DATA

Terminal




1 = $Q_1$ = output 1

2 = $Q_2$ = output 2

3 = $A_2$ = trigger input 2

4 = $A_1$ = trigger input 1

5 = $W_2$ = d.c. input 2

6 = $W_1$ = d.c. input 1

7 = K = terminal for external trigger input

8 = N = supply -6 V

9 = P = supply +6 V

10 = E = common supply 0 V

Power Supply

Terminal 8 : $V_N$ = -6 V ± 5 %, $-I_N$ = 8.8 mA } Nominal value

9 : $V_P$ = 6 V ± 5 %, $I_P$ = 0.6 mA } of the current

10 : $V_E$ = 0 V common

Notes

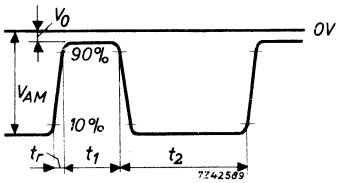
- The data given apply to the most adverse supply voltages for a combination of units, namely $V_N$=-5.7V and $V_P$=6.3V.
- The temperatures -20 °C and +60 °C, and the tolerances on the supply voltages are absolute limiting values.
- When a current is flowing towards the unit, the positive sign is used.

## INPUT DATA

### Input Signal Requirements

Trigger Input Signal (A terminals)

A positive-going voltage step is applied to terminal $A_1$ or $A_2$, or to both terminals interconnected in the case of binary scale-of-two applications. This voltage step drives the transistor $T_1$ ($T_2$) into the non-conducting state.
To terminal K external diodes can be connected (in the same sense as diode $D_6$) to provide the pulse-gate, corresponding with terminal $A_2$, with extra trigger inputs or condition inputs.




Voltage

| | | | | |
|---|---|---|---|---|
| $V_{AM}$ | = | min. | -0.7 | $V_N$ |
| | = | max. | - | $V_N$ |
| $-V_o$ | = | min. | 0 | V |
| | = | max. | 0.2 | V |

| | | $A_1$ or $A_2$ | $A_1$ and $A_2$ interconnected |
|---|---|---|---|
| Required direct current | $I_{AD}$ = | min. 0.88 mA | min. 1.75 mA |
| Required current during the transient averaged over: 0.4 µs | $I_{AT}$ = | min. 5 mA | min. 6 mA |
| 0.7 µs | = | min. 4 mA | min. 4.5 mA |

| | | | | |
|---|---|---|---|---|
| Rise time | $t_r$ | = | max. | 0.7 µs |
| Pulse duration | $t_1$ | = | min. | 1 µs |
| | $t_2$ | = | min. | 8 µs |
| Input noise level | $V_n$ | = | max. | 1 V peak to peak |

DC Input Signal (W terminals)

A d.c. voltage level is applied to terminal $W_1$ or $W_2$. A positive voltage drives the transistor $T_1$ ($T_2$) into the non-conducting state and a negative voltage drives it into the conducting state

| | | | | |
|---|---|---|---|---|
| Transistor conducting | | | | |
| Current | $-I_W$ | = | min. | 0.6 mA ($-V_W$ = max. 0.4 V) |
| limiting value | | = | max. | 15 mA |
| Transistor non-conducting | | | | |
| Voltage | $V_W$ | = | min. | 0.2 V |
| limiting value | | = | max. | 10 V |
| Current | $I_W$ | = | min. | 0.9 mA |

OUTPUT DATA

Voltages and currents

Transistor conducting

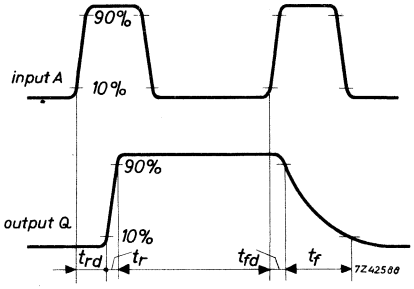
| | | | | |
|---|---|---|---|---|
| Voltage | $-V_Q$ | = | max. | 0.2 V |
| Available direct current | $-I_{QD}$ | = | max. | 6 mA |
| Available current during the transient | | | | |
| averaged over: 0.4 µs | $-I_{QT}$ | = | max. | 11 mA |
| 0.7 µs | | = | max. | 14 mA |

Transistor non-conducting

| | | | | |
|---|---|---|---|---|
| Voltage | $-V_Q$ | = | min. | -0.7 $V_N$ |
| Available direct current | $I_{QD}$ | = | max. | 0.7 mA |

## Switching and delay times

These data are for orientation only and refer to an input signal as specified under INPUT DATA.




| | | Unit unloaded | Unit max. loaded |
|---|---|---|---|
| Rise delay | $t_{rd}$ = | max. 1.0 µs | max. 1.1 µs |
| Rise time | $t_{r}$ = | max. 0.3 µs | max. 0.7 µs |
| Fall delay | $t_{fd}$ = | max. 0.8 µs | max. 0.8 µs |
| Fall time | $t_{f}$ = | max. 1.7 µs | max. 1.7 µs |

# FLIP-FLOP

Colour: red

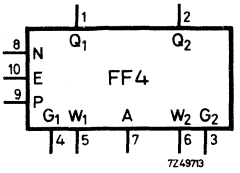
The unit FF4 contains a transistor bi-stable multivibrator circuit. The transistors are medium-speed switching types.

The circuit constitutes a memory function when driven by means of a d.c. level or a positive-going trigger signal. In the case of trigger drive, the switching of the flip-flop can be controlled by a d.c. level applied to the built-in gate circuits (e.g. in shift registers).

Frequency range : see INPUT DATA

Ambient temperature range : -20 to +60 °C

Weight : approx. 20 g

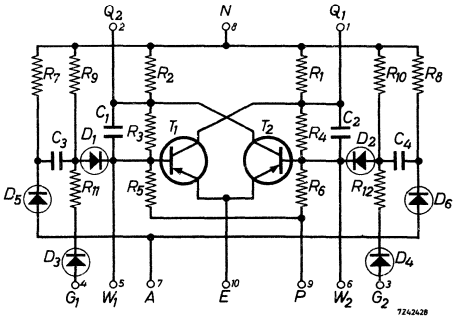



Drawing symbol

CIRCUIT DATA

Terminal

1 = $Q_1$ = output 1
2 = $Q_2$ = output 2
3 = $G_2$ = gate input 2
4 = $G_1$ = gate input 1
5 = $W_1$ = d.c. input 1
6 = $W_2$ = d.c. input 2
7 = A = trigger input
8 = N = supply -6 V
9 = P = supply +6 V
10 = E = common supply 0 V




Power Supply

Terminal 8 : $V_N$ = -6 V ± 5 %, $-I_N$ = 8.8 mA } Nominal value
9 : $V_P$ = +6 V ± 5 %, $I_P$ = 0.6 mA } of the current
10 : $V_E$ = 0 V common

Notes

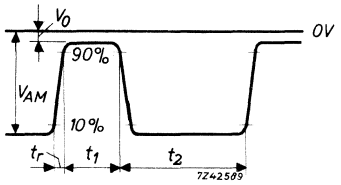
- The data given apply to the most adverse supply voltages for a combination of units, namely $V_N = -5.7$ V and $V_P = 6.3$ V.
- The temperatures -20 °C and +60 °C, and the tolerances on the supply voltages are absolute limiting values.
- When a current is flowing towards the unit, the positive sign is used.

## INPUT DATA

### Input Signal Requirements

Trigger Input Signal (A terminal)

A positive-going voltage step is applied to terminal A. This voltage step drives the transistor $T_1(T_2)$ into the non-conducting state if the corresponding gate has been opened by an appropriate gate input signal on terminal $G_1(G_2)$.




| | | | | |
|---|---|---|---|---|
| Voltage | $V_{AM}$ | = min. | -0.7 | $V_N$ |
| | | max. | - | $V_N$ |
| | $-V_o$ | = min. | 0 | V |
| | | max. | 0.2 | V |
| Required direct current | $I_{AD}$ | = min. | 1.75 | mA |
| Required current during the transient | | | | |
| averaged over: 0.4 µs | $I_{AT}$ | = min. | 6 | mA |
| 0.7 µs | | min. | 4.5 | mA |
| Rise time | $t_r$ | = max. | 0.7 | µs |
| Pulse duration | $t_1$ | = min. | 3 | µs |
| | $t_2$ | = min. | 11 | µs |
| Input noise level | $V_n$ | = max. | 1 V peak to peak | |

DC Input signal (W terminals)

A d.c. voltage level is applied to terminal $W_1$ or $W_2$. A positive voltage drives the transistor $T_1(T_2)$ into the non-conducting state and a negative voltage drives it into the conducting state.

| | | |
|---|---|---|
| Transistor conducting | | |
| Current | $-I_W$ = min. 0.6 mA | ($-V_W$ = max. 0.4 V) |
| limiting value | = max. 15 mA | |
| Transistor non-conducting | | |
| Voltage | $V_W$ = min. 0.2 V | |
| limiting value | = max. 10 V | |
| Current | $I_W$ = min. 0.9 mA | |

Gate Input Signal (G terminals)

A d.c. voltage level is applied to terminal $G_1(G_2)$. Transistor $T_1(T_2)$ is driven into the non-conducting state by the trigger input signal (A terminal) if the corresponding gate is opened by an appropriate gate input signal.

| | | gate open | gate closed |
|---|---|---|---|
| Voltage | $-V_G$ | = min. 0 V | min. $V_{AM}$ |
| | | max. 0.2 V | max. - $V_N$ |
| Required gate current caused by negative transient of $V_{AM}$ | $I_{GD}$ | = min. 1.75 mA | min. 1.2 mA |

| | | to open gate | to close gate |
|---|---|---|---|
| Required average current during the positive transient of $V_G$ | $I_{GT}$ | = min. 1.6 mA | – |
| Gate setting time | | | |
| when the gate input level changes at random: | $t_{GS}$ | = min. 17 µs | min. 25 µs |
| when the gate input level changes within 2 µs after the positive going edge of the trigger signal: | $t_{GS}$ | = min. 11 µs | min. 11 µs |

Note: The latter applies to a shift register configuration so that the max. shift frequency is approximately 70 kHz.

During triggering the G levels should not be at zero voltage level simultaneously.

The gate setting time is the required waiting time between the last G level change and the potitive going edge of the trigger pulse.

OUTPUT DATA

Voltages and currents

Transistor conducting

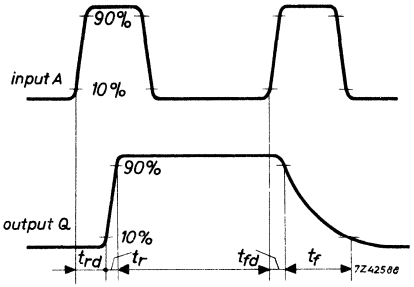
| | | | | |
|---|---|---|---|---|
| Voltage | $-V_Q$ | = max. | 0.2 | V |
| Available direct current | $-I_{QD}$ | = max. | 6 | mA |
| Available current during the transient | | | | |
| averaged over: 0.4 µs | $-I_{QT}$ | = max. | 11 | mA |
| 0.7 µs | | = max. | 14 | mA |

Transistor non-conducting

| | | | | |
|---|---|---|---|---|
| Voltage | $-V_Q$ | = min. | -0.7 | $V_N$ |
| Available direct current | $I_{QD}$ | = max. | 0.7 | mA |

Switching and delay times

These data are for orientation only and refer to an input signal as specified under INPUT DATA.




| | | Unit unloaded | | Unit max. loaded | |
|---|---|---|---|---|---|
| Rise delay | $t_{rd}$ | = max. 1.0 | µs | max. 1.1 | µs |
| Rise time | $t_r$ | = max. 0.3 | µs | max. 0.7 | µs |
| Fall delay | $t_{fd}$ | = max. 0.8 | µs | max. 0.8 | µs |
| Fall time | $t_f$ | = max. 1.7 | µs | max. 1.7 | µs |

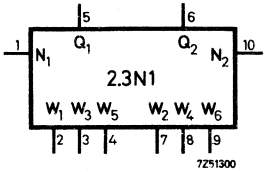
# DUAL NEGATIVE GATE

Colour: orange

The unit 2.3N1 contains two three-input germanium-diode gates, that perform an AND logical operation on negative input-voltage signals.

The two gate circuits are identical and can be used separately or combined into a multiple-input gate by interconnecting the output terminals $Q_1$ and $Q_2$. In this latter case only one negative supply terminal should be used.

| | |
|---|---|
| Pulse repetition frequency range: | 0-100 kHz |
| Ambient temperature range: | -20 to +60 °C |
| Weight: | approx. 20 g |

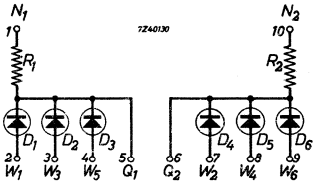



Drawing symbol

CIRCUIT DATA

**Terminal**

1 = $N_1$ = supply -6 V (1)
2 = $W_1$ = input 1
3 = $W_3$ = input 3
4 = $W_5$ = input 5
5 = $Q_1$ = output 1
6 = $Q_2$ = output 2
7 = $W_2$ = input 2
8 = $W_4$ = input 4
9 = $W_6$ = input 6
10 = $N_2$ = supply -6 V (2)



Power Supply

Terminal 1: $V_{N1} = -6V \pm 10\%$, $-I_{N1} = 0\text{-}0.5mA$ [1]) } Nominal value of the current

10: $V_{N2} = -6V \pm 10\%$, $-I_{N2} = 0\text{-}0.5mA$ [1]) }

INPUT DATA

Input Signal Requirements [2])

Voltage: Under all circumstances normally encountered when the unit is used in conjunction with other circuit blocks: $V_{Wn} = 0.1$ to $0.5V$ more positive than $V_Q$ dependent on the input current $I_{Wn}$.

Current: To be supplied to terminal $W_n$ having the least negative voltage level. For $V_{Wn} = 0$ volt and $I_Q = 0mA$: $I_{Wn}$ = max. 0.48mA [1]) + max. 0.04mA [1]) for every W terminal at a negative voltage level.

OUTPUT DATA

Output Signal Characteristics [2])

Voltage: see INPUT DATA

Load current $I_Q$ = max. $\frac{-V_N + V_Q}{13}$ mA [1])

Output Impedance

When $V_Q$ is positive-going, the output impedance approximates the output impedance of the driving circuit. When $V_Q$ is negative-going, the output impedance is max. 13kΩ.

LIMITING VALUES

Current through conducting diode $I_{Wc}$ = max. 10mA

Voltage between terminals N and W = max. 30V

[1]) The sign is positive when the current flows towards the circuit.

[2]) These data apply to the most adverse working condition for a combination of units, namely to a supply voltage $V_N = -5.4V$. Unless differently specified, all the voltage and current figures quoted represent absolute maximum values.

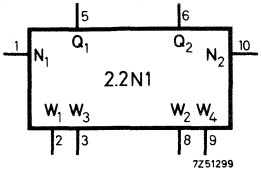
# DUAL NEGATIVE GATE

Colour: orange

The unit 2.2N 1 contains two two-input germanium-diode gates that perform an AND logical operation on negative input voltage signals.

The two gate circuits are identical and can be used separately or combined into a multiple-input gate by interconnecting the output terminals $Q_1$ and $Q_2$. In this latter case, only one negative supply terminal should be used.

| | |
|---|---|
| Pulse repetition frequency range: | 0–100 kHz |
| Ambient temperature range: | −20 to +60 °C |
| Weight: | approx. 20 g |




Drawing symbol

CIRCUIT DATA

Terminal

1 = $N_1$ = supply −6V (1)

2 = $W_1$ = input 1

3 = $W_3$ = input 3

4 = not connected

5 = $Q_1$ = output 1

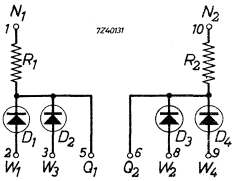
6 = $Q_2$ = output 2

7 = not connected

8 = $W_2$ = input 2

9 = $W_4$ = input 4

10 = $N_2$ = supply −6V (2)




Power Supply

Terminal 1: $V_{N1} = -6V \pm 10\%$, $-I_{N1} = 0\text{–}0.5\,mA$ [1])

10: $V_{N2} = -6V \pm 10\%$, $-I_{N2} = 0\text{–}0{,}5\,mA$ [1])

} Nominal value of the current

[1]) The sign is positive when the current flows towards the circuit.

INPUT DATA

Input Signal Requirements [2])

Voltage: Under all circumstances normally encountered when the unit is used in conjunction with other circuit blocks: $V_{Wn}$ = 0.1 to 0.5 V more positive than $V_Q$ dependent on the input current $I_{Wn}$.

Current: To be supplied to terminal $W_n$ having the least negative voltage level. For $V_{Wn}$ = 0 volt and $I_Q$ = 0 mA: $I_{Wn}$ = max. 0.48 mA [1]) + max. 0.04 mA [1]) for every W terminal at a negative voltage level.

OUTPUT DATA

Output Signal Characteristics [2])

Voltage: See INPUT DATA

Load current $I_Q = \text{max.} \frac{-V_N + V_Q}{13}$ mA [1])

Output Impedance

When $V_Q$ is positive-going, the output impedance approximates the output impedance of the driving circuit. When $V_Q$ is negative-going, the output impedance is max. 13 kΩ.

LIMITING VALUES

Current through conducting diode $I_{Wc}$ = max. 10 mA

Voltage between terminals N and W = max. 30 V

[1]) The sign is positive when the current flows towards the circuit

[2]) These data apply to the most adverse working condition for a combination of units, namely to a supply voltage $V_N$ = -5.4 V. Unless differently specified, all the voltage and current figures quoted represent absolute maximum values.

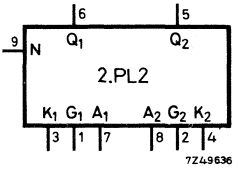
# DUAL PULSE LOGIC

Colour: orange

The unit 2.PL2 contains two identical pulse gates which are controlled by a d.c. voltage level.

The circuits are normally used in conjunction with flip-flop circuits. With the dual pulse logic a second pair of a.c. inputs are formed for a flip-flop FF3, or in combination with flip-flops FF4 a bi-directional shift register can be made. In these applications the 2.PL2 output terminals are to be connected directly to the flip-flop d.c. input terminals.

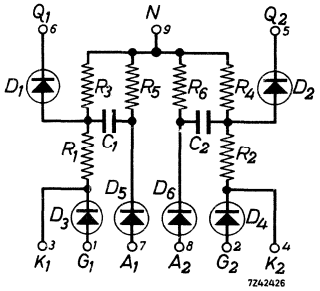
| | |
|---|---|
| Frequency range | : see INPUT DATA |
| Ambient temperature range | : -20 to +60 °C |
| Weight | : approx. 20 g |




Drawing symbol

CIRCUIT DATA

Terminal 1 = $G_1$ = gate input 1
2 = $G_2$ = gate input 2
3 = $K_1$ = terminal for external gate input
4 = $K_2$ = terminal for external gate input
5 = $Q_2$ = output 2
6 = $Q_1$ = output 1
7 = $A_1$ = trigger input 1
8 = $A_2$ = trigger input 2
9 = N = supply -6 V
10 = not connected




Power Supply

Terminal 9 : $V_N$ = -6 V ± 5 %, $-I_N$ = 0-2.5 mA Nominal value of the current

Notes

- The data given apply to the most adverse supply voltages for a combination of units, namely $V_N$=-5.7V and $V_P$=6.3V.
- The temperatures -20 °C and +60 °C, and the tolerances on the supply voltages are absolute limiting values.
- When a current is flowing towards the unit, the positive sign is used.

INPUT DATA

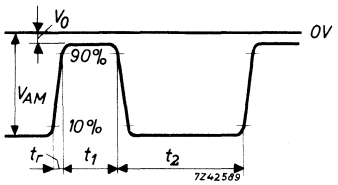
These data are dependent on the driven circuit, the values given apply to use of the dual pulse logic in conjunction with flip-flops FF3 or FF4.

Input Signal Requirements

Trigger Input Signal (A terminals)

A positive going voltage step is applied to terminal $A_1$ or $A_2$ or to both terminals interconnected.

This voltage step passes the pulse gate if it has been opened by an appropriate gate input signal on terminal $G_1$($G_2$).




| | | | | | | |
|---|---|---|---|---|---|---|
| Voltage | $V_{AM}$ | = min. | -0.7 | $V_N$ | | |
| | | = max. | - | $V_N$ | | |
| | $-V_o$ | = min. | 0 | V | | |
| | | = max. | 0.2 | V | | |
| | | | $A_1$ or $A_2$ | | $A_1$ and $A_2$ interconnected | |
| Required direct current | $I_{AD}$ | = min. | 0.88 | mA | min. 1.75 | mA |
| Required current during the transient | | | | | | |
| averaged over: 0.4 µs | $I_{AT}$ | = min. | 5 | mA | min. 6 | mA |
| 0.7 µs | | = min. | 4 | mA | min. 4.5 | mA |

| | | | |
|---|---|---|---|
| Rise time | $t_r$ | = max. 0.7 | µs |
| Pulse duration | $t_1$ | = min. 3 | µs |
| | $t_2$ | = min. 11 | µs |
| Input noise level | $V_n$ | = max. 1 | V peak to peak |

Gate Input Signal (G terminals)

A d.c. voltage level is applied to terminal $G_1$ ($G_2$).

The trigger input signal (terminal $A_1$($A_2$) passes if the corresponding gate is opened by an appropriate gate input signal.

To terminal $K_1$($K_2$) external diodes can be connected (in the same sense as diode $D_3$($D_4$)), to provide the corresponding pulse gate with extra condition inputs.

| | | gate open | gate closed |
|---|---|---|---|
| Voltage | $-V_G$ | = min. 0 V | min. $V_{AM}$ |
| | | = max. 0.2 V | max. - $V_N$ |
| Required gate current causedby negative transient of $V_{AM}$ | $I_{GT}$ | = min. 1.75 mA | min. 1.2 mA |
| | | to open gate | to close gate |
| Required average current during the positive transient of $V_G$ | $I_{GT}$ | = min. 1.6 mA | |
| Gate setting time | | | |
| when the gate input level changes at random | $t_{GS}$ | = min. 17 µs | min. 25 µs |
| when the gate input level changes within 2 µs after the positive going edge of the trigger signal | $t_{GS}$ | = min. 11 µs | min. 11 µs |

Note: The latter applies to a shift register configuration so that the max. shift frequency is approximately 70 kHz

During triggering the G levels should not be at zero voltage level simultaneously.

The gate setting time is the required waiting time between the last G level change and the positive going edge of the trigger pulse.

OUTPUT DATA

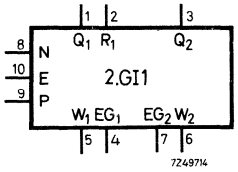
When used in conjunction with flip-flops FF3 and FF4, the output terminals ($Q_1$ and $Q_2$) are directly connected to the flip-flop d.c. input terminals ($W_1$ and $W_2$).

# DUAL GATE INVERTER

The 2.GI 1 is to be considered as the back bone of the 1-Series circuit blocks with which all logic configurations can be realised. Moreover the 2.GI 1 can perform other important functions which are specified below.

The unit 2.GI 1 contains two gate inverter circuits; the terminals W and EG have normally to be interconnected externally. The gating function is obtained by connecting diodes externally to the terminal EG.
The circuit performs a NAND function on the negative high level. The terminals $R_1$ and $Q_1$ are normally interconnected.
When collector-OR logic is employed, terminal $R_1$ can be left floating. The logic operation is performed by connecting both collectors Q to the collector resistor of $TR_2$. Herewith the AND-OR operation can be obtained. Up to four collectors may be interconnected with one collector resistor.
The inverter circuits can also be preceded by a double diode logic configuration to perform the AND-AND as well as the Factored-AND operation. For these applications a VDR, asymmetric type 2322 574 90007 has to be connected externally between the terminals W and EG; the gating diodes are to be connected to terminal EG. Furthermore the following major functions can be realised as well:

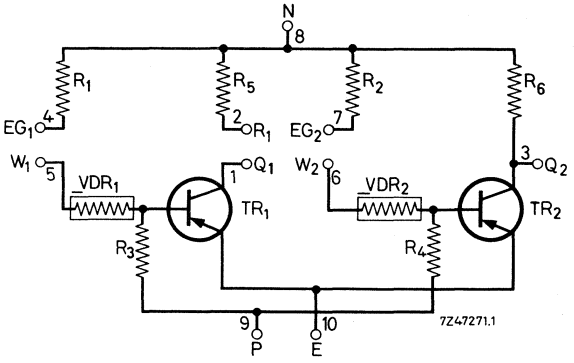
- a set-reset flip-flop by cross-connecting the inputs and outputs of both gate inverter circuits via diodes type OA85/OA95, to be mounted externally
- a non-inverting amplifier with increased output loadability
- a relay driver, by interconnecting the two inverter circuits in series.




Drawing symbol

CIRCUIT DATA

Terminal
1 = $Q_1$ = output 1
2 = $R_1$ = connection collector resistor
3 = $Q_2$ = output 2
4 = $EG_1$ = extension gate input 1
5 = $W_1$ = d.c. input 1
6 = $W_2$ = d.c. input 2
7 = $EG_2$ = extension gate input 2
8 = N = supply −6 V
9 = P = supply +6 V
10 = E = common supply 0 V



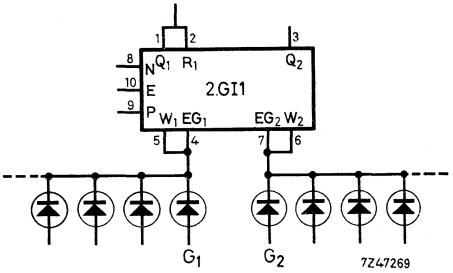

Power supply

Terminal 8 : $V_N$ = −6 V ± 5 %
9 : $V_P$ = +6 V ± 5 %
10 : $V_E$ = 0 V common

$-I_N$ = 2 to 4.2 mA } nominal value
$I_P$ = 0.22 mA } of the current

Notes
- The data given apply to the most adverse supply voltages for a combination of units, namely $V_N$ = −5.7 V and $V_P$ = 6.3 V.
- The temperatures −20 °C and +60 °C and the tolerances on the supply voltages are absolute limiting values.
- When a current is flowing towards the unit, the positive sign is used.

DUAL NAND or DUAL NOR




Circuit diagram with interconnections to be made externally

Input requirements

Input at G:

| | | |
|---|---|---|
| Transistor conducting | (output level "negative low") | |
| Voltage | $-V_G$ = min. | -0.7 $V_N$ |
| | max. | $-V_N$ |
| Transistor non-conducting | (output level "negative high") | |
| Voltage | $-V_G$ = min. | 0 V |
| | max. | 0.2 V |
| Required direct current | $I_{GD}$ = min. | 1 mA |
| Required transient current averaged over 0.7 $\mu$s | $I_{GT}$ = min. | 3 mA |

Type of diodes and maximum number connected in parallel at terminals EG: 11 x OA85/OA95.

Output data

| | | |
|---|---|---|
| Transistor non-conducting | (output level "negative high") | |
| Voltage | $-V_Q$ = approx. | $V_N$ |
| Transistor conducting | (output level "negative low") | |
| Voltage | $-V_Q$ = min. | 0 V |
| | max. | 0.2 V |

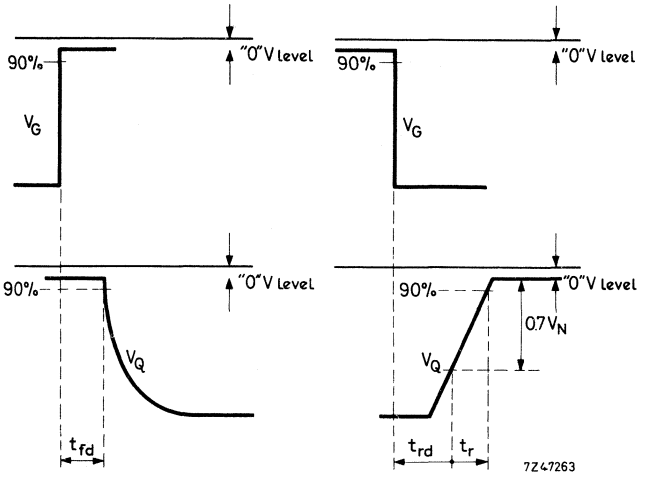
Available direct current

| | | |
|---|---|---|
| R connected to Q | $-I_{QD}$ = max. | 15 mA |
| in collector-OR configuration | max. | 10 mA |
| R not connected to Q | max. | 11.3 mA |

Available transient current averaged over 0.7 $\mu$s

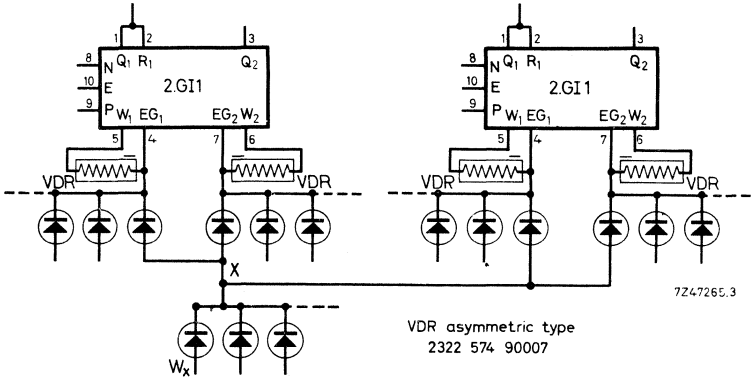
| | | |
|---|---|---|
| R connected to Q | $-I_{QT}$ = max. | 9.0 mA |
| R not connected to Q | max. | 9.7 mA |

Time data




For further data see Table 2, page B48

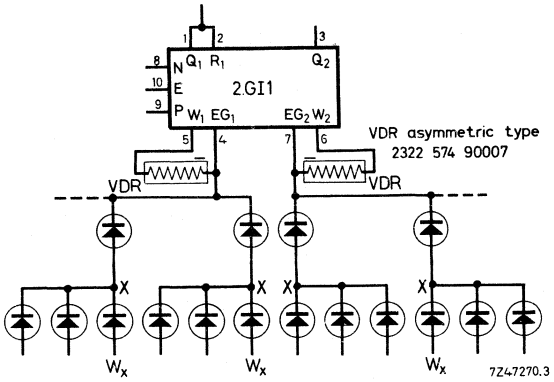
FACTORED-AND-GI




Circuit diagram with interconnections to be made externally

4 separate GI circuits, each which may have 10 input diodes in parallel, may be driven simultaneously by a gate with 10 diodes in parallel.
A gate resistor between point X and $V_N$ decreases the rise delay time $t_{rd}$ (see Time data under AND-AND-GI)

AND-AND-GI




Circuit diagram with interconnections to be made externally

To each EG terminal 25 parallel input diodes may be connected. Each of these input diodes may be driven by a gate with 10 input diodes in parallel.
A gate resistor between points X and $V_N$ decreases the rise delay time $t_{rd}$ (see Time data)

Input requirements

Input at terminals $W_X$:

Transistor conducting (all terminals $W_X$ at "negative high" level)

| | |
|---|---|
| Voltage | $-V_{WX}$ = min. −0.7 $V_N$<br>max. $-V_N$ |

Transistor non-conducting (one of the terminals $W_X$ at "0" V level)

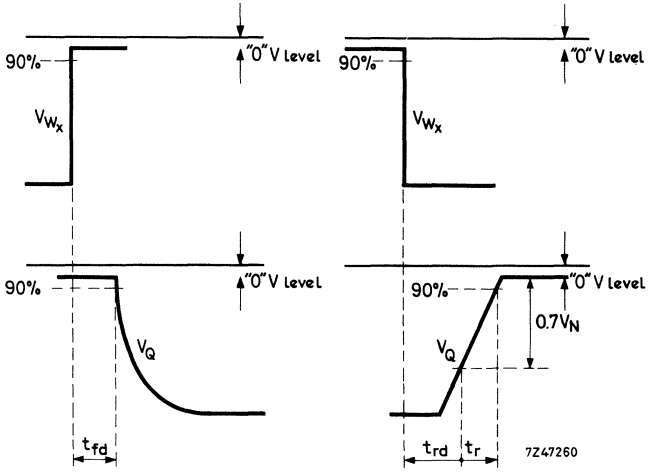
| | |
|---|---|
| Voltage | $-V_{WX}$ = min. 0 V<br>max. 0.2 V |
| Required direct current | Sum of GI d.c. input currents [1] |
| Required transient current averaged over 0.7 $\mu$s | Sum of GI transient input currents [2] |

[1] When a gate resistor between point X and $V_N$ is used, the negative gate input current has to be added.

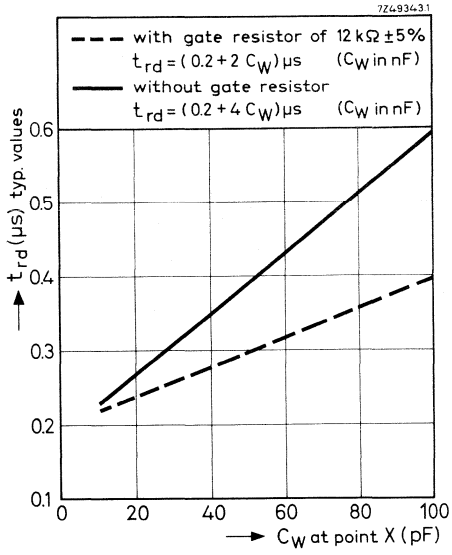
[2] When a gate resistor is used, 0.7 x d.c. input current of the negative gate has to be added.

Output data

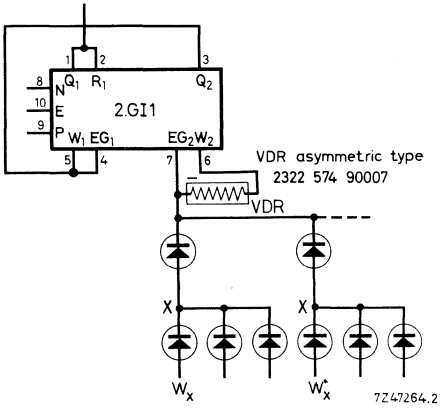
| | |
|---|---|
| Transistor non-conducting | (output level "negative high") |
| Voltage | $-V_Q$ = approx. $V_N$ |
| Transistor conducting | (output level "negative low") |
| Voltage | $-V_Q$ = min. 0 V |
| | max. 0.2 V |
| Available direct current | $-I_{QD}$ = max. 8 mA |
| in collector - OR configuration | max. 4.5 mA |
| Available transient current averaged over 0.7 $\mu$s | $-I_{QT}$ = max. 4.5 mA |




For further data see Table 2, page B48.




AND-AND-GI-GI




Circuit diagram with interconnections to be made externally

When AND-AND or Factored-AND is employed and $Q_2$ is connected to $EG_1$ an increased loadability can be obtained from $Q_1$. The output voltage at $Q_1$ is not inverted with respect to the input voltage at $W_X$.
A gate resistor between points X and $V_N$ decreases the fall delay time $t_{fd}$ (see Time data).

Input requirements

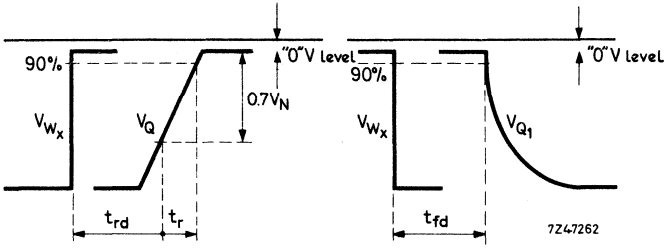
See preceding paragraph.

Output data

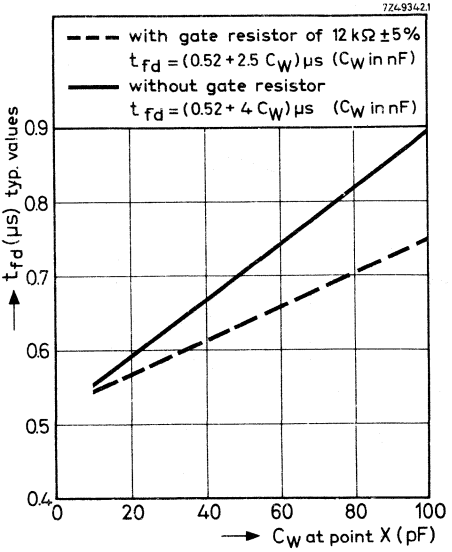
Output $Q_1$

| | | | |
|---|---|---|---|
| Transistor non-conducting | (output level "negative high") | | |
| Voltage | $-V_{Q_1}$ = approx. | | $V_N$ |
| Transistor conducting | (output level "negative low") | | |
| Voltage | $-V_{Q_1}$ = min. | 0 | V |
| | max. | 0.2 | V |
| Available direct current | $-I_{Q_1D}$ = max. | 25 | mA |
| Available transient current averaged over 0.7 $\mu$s | $-I_{Q_1T}$ = max. | 22.5 | mA |

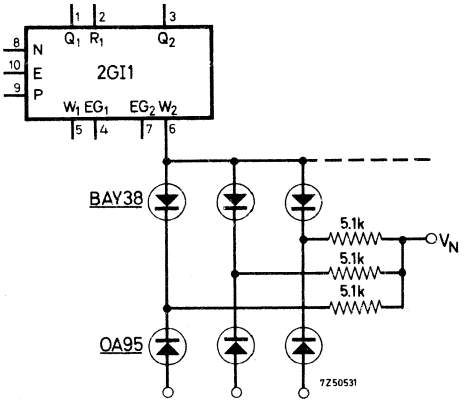
Time data




For further data see Table 2, page B48.




AND-OR-GI (1)




Used where long switching delays can be tolerated.

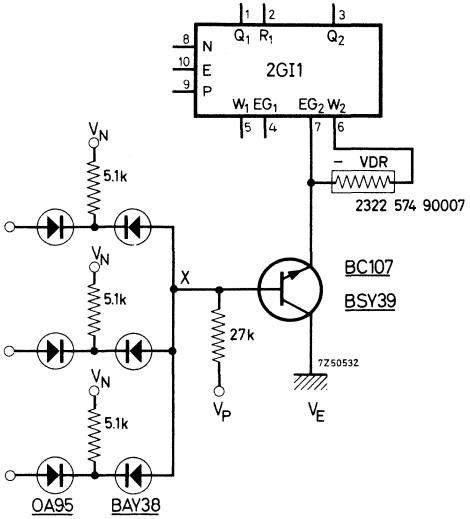
Input requirements

See DUAL NAND or DUAL NOR.

Output data

See AND-AND-GI and Table 1, page B47.
For time data see Table 2, page B48.

AND-OR-GI (2)




Used where short delays are essential.

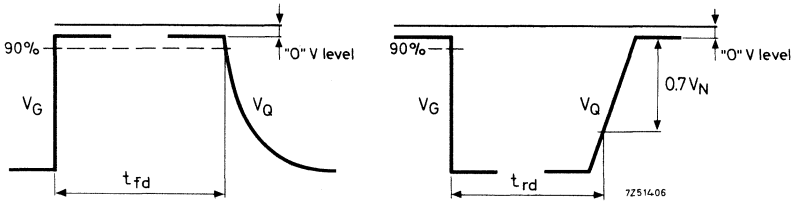
Input data

See DUAL NAND or DUAL NOR.

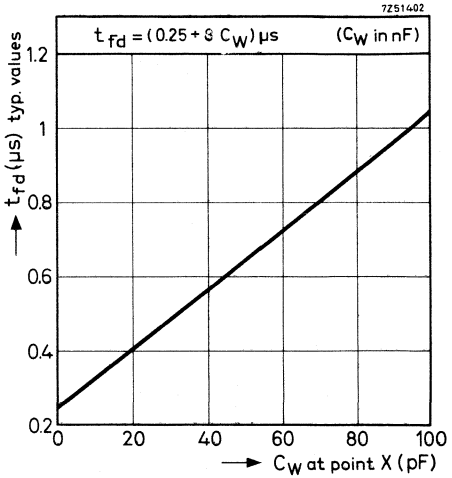
Output data

See AND-AND-GI and Table 1, page B47.

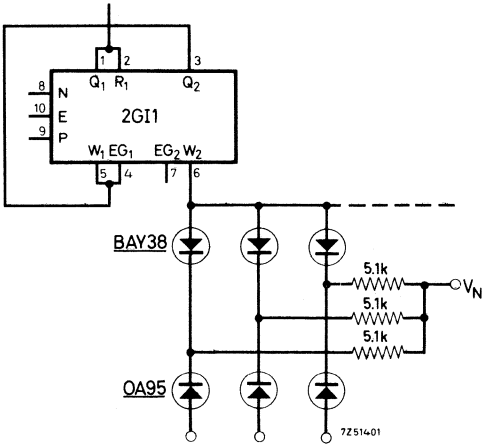
Time data




For further data see Table 2, page B48.




AND-OR-GI-GI (1)




Circuit diagram with interconnections to be made externally

Used where long switching delays are tolerated.

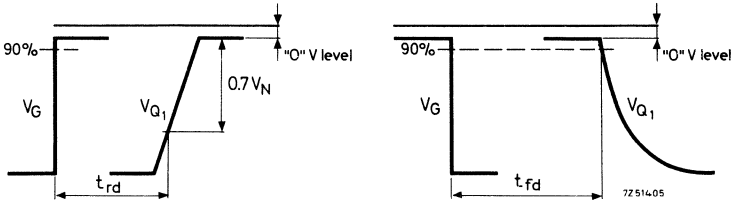
Input requirements

See DUAL NAND or DUAL NOR.

Output data

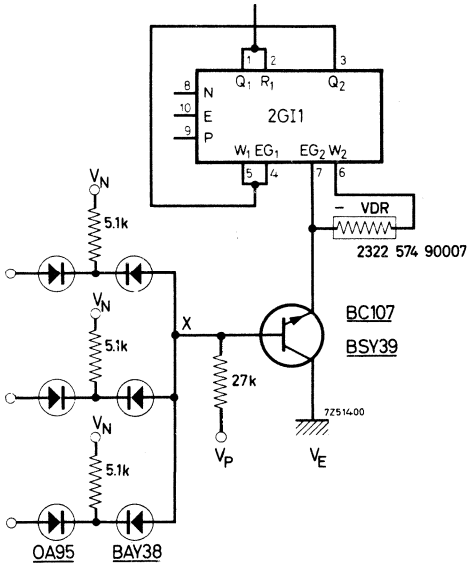
See AND-AND-GI-GI.

Time data




For further data see Table 2, page B48.

AND-OR-GI-GI (2)




Circuit diagram with interconnections to be made externally

Used where short delays are essential.

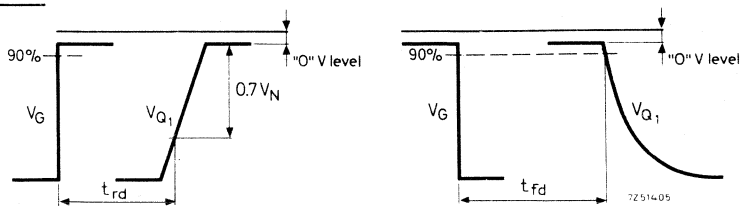
Input requirements

See DUAL NAND or DUAL NOR.

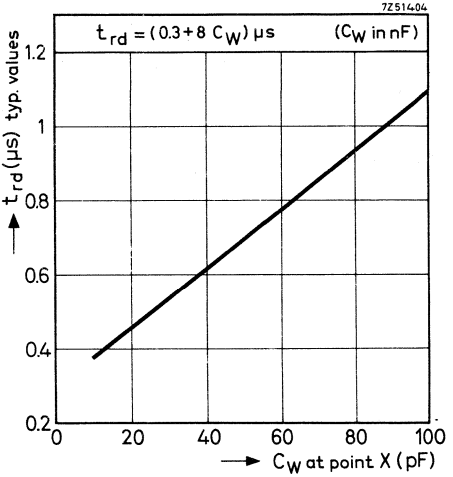
Output data

See AND-AND-GI-GI.

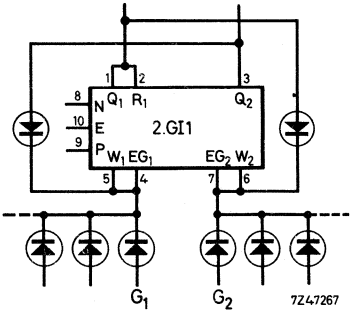
Time data




For further data see Table 2, page B48.




SET-RESET FLIP-FLOP




Circuit diagram with interconnections to be made externally

Upon application of the "0" V level to one of the diode inputs, the corresponding output Q resumes the "negative high" level, and the other output the "0" V level. The "negative high" level applied to an input is inoperative.

Input requirements

Input at G:

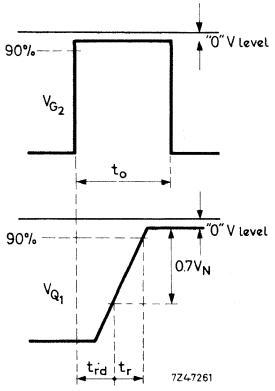
| | | | |
|---|---|---|---|
| Transistor conducting | (output level "negative low") | | |
| Voltage | $-V_G$ = min. | -0.7 | $V_N$ |
| | max. | | $-V_N$ |
| Transistor non-conducting | (output level "negative high") | | |
| Voltage | $-V_G$ = min. | 0 | V |
| | max. | 0.2 | V |
| Required direct current | $I_{GD}$ = min. | 1 | mA |
| Required transient current averaged over 0.7 $\mu$s | $I_{GT}$ = min. | 3 | mA |

Type of diodes and maximum number connected in parallel at terminal EG: 10 x OA85/OA95.

Output data

| | | | |
|---|---|---|---|
| Transistor non-conducting | (output level "negative high") | | |
| Voltage | $-V_Q$ = approx. | | $V_N$ |
| Transistor conducting | (output level "negative low") | | |
| Voltage | $-V_Q$ = min. | 0 | V |
| | max. | 0.2 | V |
| Available direct current | $-I_{QD}$ = max. | 9 | mA |
| Available transient current averaged over 0.7 $\mu$s | $-I_{QT}$ = max. | 9 | mA |

Time data



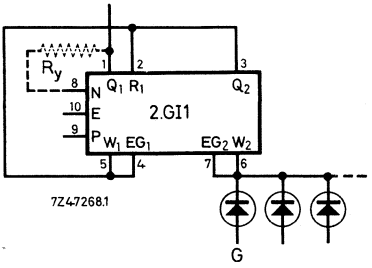
$t_{rd}$ = typ. 0.5 $\mu$s (delay from $G_2$ to $Q_1$, or $G_1$ to $Q_2$, with a square wave input signal)

$t_r$ = max. 0.7 $\mu$s (at maximum transient load e.g. 3 x GI1 or 2 FF3/FF4)

= max. 1.5 $\mu$s (loaded with 9 x GI1)

$t_o$ = min. 2 $\mu$s

NON-INVERTING AMPLIFIER or RELAY DRIVER




Circuit diagram with interconnections to be made externally

When used as non-inverting amplifier an external resistor $R_y$ = 2.2 k$\Omega$ ± 2 % is needed between $Q_1$ and $V_N$.

Input requirements

Input at G:

| | | | | |
|---|---|---|---|---|
| Output transistor non-conducting | (output level "negative high") | | | |
| Voltage | $-V_G$ | = min. | 0.7 | $V_N$ |
| | | max. | - | $V_N$ |
| Transistor conducting | (output level "negative low") | | | |
| Voltage | $-V_G$ | = min. | 0 | V |
| | | max. | 0.2 | V |
| Required direct current | $I_{GD}$ | = min. | 1 | mA |
| Required transient current averaged over 0.7 $\mu$s | $I_{GT}$ | = min. | 3 | mA |

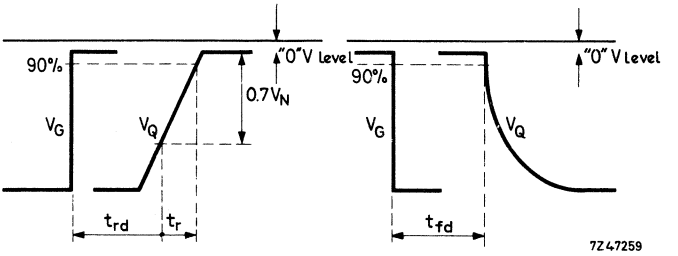
Type of diodes and maximum number connected in parallel at terminal EG: 11 x OA85/OA95.

Output data (as non-inverting amplifier)

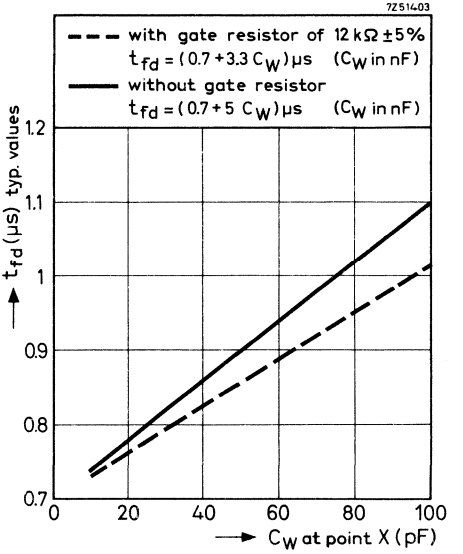
Output $Q_1$ :

| | | | |
|---|---|---|---|
| Transistor non-conducting | (output level "negative high") | | |
| Voltage | $-V_{Q_1}$ = approx. | $V_N$ | |
| Transistor conducting | (output level "negative low") | | |
| Voltage | $-V_{Q_1}$ = min. | 0 | V |
| | max. | 0.2 | V |
| Available direct current | $-I_{Q_1D}$ = max. | 40 | mA |
| Available transient current averaged over 0.7 $\mu$s | $-I_{Q_1T}$ = max. | 27 | mA |

Time data




For further data see Table 2, page B48.



Output data (as relay driver)

Output $Q_1$ :

| | |
|---|---|
| Transistor non-conducting | (output level "negative high") |
| Voltage | $-V_{Q_1}$ = abs. max. 15 V |
| Transistor conducting | (output level "negative low") |
| Voltage | $-V_{Q_1}$ = min. 0 V<br>max. 0.25 V |
| Available direct current | $-I_{Q_1D}$ = max. 65 mA |

SURVEY OF OUTPUT DATA

Table 1

| applied configuration | preceded by | | | |
|---|---|---|---|---|
| | AND | | AND-AND<br>Factored-AND<br>AND-OR (1)<br>AND-OR (2) | |
| | $-I_{QD}$ (mA) | $-I_{QT}$ (mA) | $-I_{QD}$ (mA) | $-I_{QT}$ (mA) |
| GI | 15 | 9 | 8 | 4.5 |
| GI-collector-OR | 10 | 9 | 4.5 | 4.5 |
| GI-GI | 25 | 22.5 | 25 | 22.5 |
| non-inverting amplifier | 40 | 27 | 40 | 27 |

Table 2 SURVEY OF TIME DATA

| applied configuration | preceded by | $t_{fd}$, typical values ($\mu$s) | | $t_{rd}$, typical values ($\mu$s) | | $t_r$ max ($\mu$s) at maximum d.c. load | $t_r$ max ($\mu$s) at maximum transient load |
|---|---|---|---|---|---|---|---|
| GI | AND | 0.3 | | 0.2 | | 1.5 | 1.5 |
| | AND-AND Factored-AND | 0.3 | | with gate resistor | (0.2+2 $C_W$) | 1.5 | 1.5 |
| | | | | without gate resistor | (0.2+4 $C_W$) | | |
| | AND-OR (1) | (2.5+0.4 n) | | 0.2 | | 1.5 | 1.5 |
| | AND-OR (2) | (0.25+8 $C_W$) | | 0.3 | | 1.5 | 1.5 |
| GI-collector-OR | AND | 0.3 | | 0.2 | | 1.5 | 1.5 |
| | AND-AND Factored-AND | 0.3 | | with gate resistor | (0.2+2 $C_W$) | 1.5 | 1.5 |
| | | | | without gate resistor | (0.2+4 $C_W$) | | |
| GI-GI | AND | 0.5 | | 0.4 | | 1.5 | 1.5 |
| | AND-AND Factored-AND | with gate resistor | (0.52+2.5 $C_W$) | 0.3 | | 1.5 | 1.5 |
| | | without gate resistor | (0.52+4 $C_W$) | | | | |
| | AND-OR (1) | 0.5 | | (3+0.4 n) | | 1.5 | 1.5 |
| | AND-OR (2) | 0.7 | | (0.3+8 $C_W$) | | 1.5 | 1.5 |
| non-inverting amplifier | AND | 0.5 | | 0.3 | | 1.5 | 1.5 |
| | AND-AND Factored-AND | with gate resistor | (0.7+3.3 $C_W$) | 0.3 | | 1.5 | 1.5 |
| | | without gate resistor | (0.7+5 $C_W$) | | | | |
| | AND-OR (1) | 0.6 | | (3+0.4 n) | | 1.5 | 1.5 |
| | AND-OR (2) | 0.7 | | (0.3+8 $C_W$) | | 1.5 | 1.5 |

Note n = number of inputs, switching from "1" to "0" level simultaneously. $C_W$ in nF.

# PULSE SHAPER

Colour : green

This unit contains a Schmitt trigger followed by an inverter amplifier. An input signal of a magnitude exceeding the thresholds (tripping levels) of the unit, is re-shaped and inverted into the standard d.c. level at the output. The output voltage transients are short and suitable for driving other circuit blocks at their trigger inputs (A).

The terminals A, W, $X_1$ and $X_2$ are provided in order to be able to use the PS 2 for the following purposes:

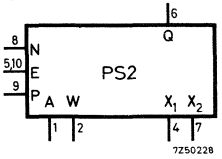
- as a pulse shaper, driven by an external source
- as a relaxation oscillator
- as a crystal controlled oscillator
- as a pulse shaper, driven by circuit blocks of the 100 kHz or 1-Series.

In the last application the number of inputs can be increased by connecting diodes type AAY 21/OA 85/OA 95 to the externally interconnected terminals A and W. The maximum number of diodes is 10.

Pulse repetition frequency range : 0 to 100 kHz

Ambient temperature range : −20 to +60 °C

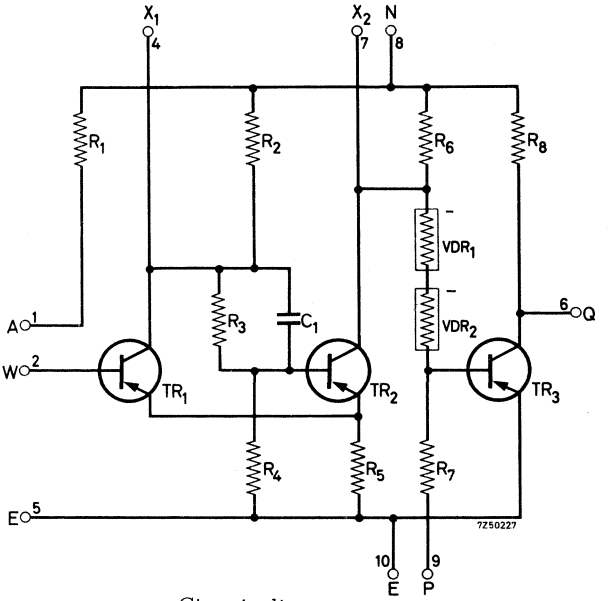
Weight : approx. 20 g




drawing symbol

CIRCUIT DATA

Terminal 1 = A = to be interconnected with terminal 2 for internal driving purposes
2 = W = input
3 = not connected
4 = $X_1$ = internally connected
5 = E = common supply 0 V (interconnected with terminal 10)
6 = Q = output
7 = $X_2$ = internally connected
8 = N = supply −6 V
9 = P = supply +6 V
10 = E = common supply 0 V




Circuit diagram

Power supply

Terminal 8 = $V_N$ = −6 V ±5 %, $-I_N$ = 3.2 - 7.5 mA } nominal value
9 = $V_P$ = +6 V ±5 %, $I_P$ = 0.19 mA } of the current
10 = $V_E$ = 0 V common

Notes

- The data given apply to the most adverse supply voltages for a combination of units, namely $V_N$ = −5.7 V and $V_P$ = +6.3 V.
- The temperatures −20 °C and +60 °C, and the tolerances on the supply voltages are absolute limiting values.
- When a current is flowing towards the unit, the positive sign is used.

INPUT DATA

Unit driven by a non-standard circuit (external source)

Internal resistance ($R_i$) of the driving circuit

$R_i$ = max. 12 kΩ ($T_{amb}$ = min. 0 °C)
$R_i$ = max. 8 kΩ ($T_{amb}$ = min. −20 °C)

Input voltage to be applied to terminal W:

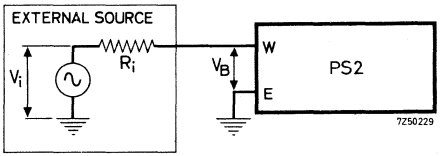
ON threshold (transistor $TR_3$ conducting)

| | operating | limiting value |
|---|---|---|
| Voltage | $-V_W$ = min. −0.4 $V_N$ | = −7.5 V |
| Current | $-I_W$ = max. 0.1 mA | = 15 mA |

OFF threshold (transistor $TR_3$ non-conducting)

| | operating | limiting value |
|---|---|---|
| Voltage | $-V_W$ = max. −0.17 $V_N$ | = −10 V |
| Current | $I_W$ = max. 0.05 mA (at $-V_W$ = 0.2 V) | |
| | = max. 0.1 mA (at $V_W$ = 10 V) | |

Hysteresis (difference between ON and OFF tripping levels)

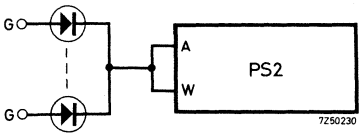



The hysteresis is affected by the internal resistance ($R_i$) of the driving circuit (external source). The relation is given by the following formula:

| $T_{amb}$ = min. 0 °C | $T_{amb}$ = min. −20 °C |
|---|---|
| $\Delta V_i$ = min. (0.07 $V_N$ − 0.033 $R_i$) | $\Delta V_i$ = min. 0.07 $V_N$ − 0.05 $R_i$) |
| $\Delta V_B = \frac{\Delta V_i}{1 + 0.057\ R_i}$ | $\Delta V_B = \frac{\Delta V_i}{1 + 0.071\ R_i}$ |

($R_i$ in kΩ and V in volt)

Unit driven by circuit blocks of the 1-Series




For this operation terminal A has to be connected to terminal W and the input voltage $V_G$ has to be applied via a diode, type AAY 21/OA 85/OA 95. The maximum number of parallel diodes is 10.

Transistor $TR_3$ conducting (output level "negative low")

| | | | |
|---|---|---|---|
| Voltage | $-V_G$ | = max. $-V_N$<br>= min. $-0.7\ V_N$ | |

Transistor $TR_3$ non-conducting (output level "negative high")

| | | | |
|---|---|---|---|
| Voltage | $-V_G$ | = min. 0<br>= max. 0.2 | V<br>V |
| Required direct current | $I_{GD}$ | = max. 0.7 | mA |
| Required transient current<br>averaged over 0.4 $\mu$s<br>averaged over 0.7 $\mu$s | $I_{GT}$ | = max. 1.1<br>= max. 0.75 | mA<br>mA |

OUTPUT DATA

Transistor $TR_3$ conducting (output level "negative low")

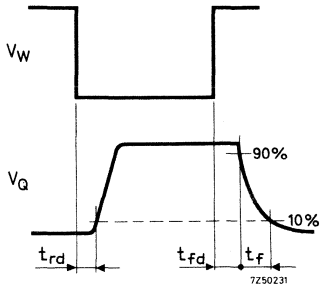
| | | | |
|---|---|---|---|
| Voltage | $-V_Q$ | = max. 0.2<br>= min. 0 | V<br>V |
| Available direct current | $-I_{QD}$ | = max. 20 | mA |
| Available transient current<br>averaged over 0.4 $\mu$s<br>averaged over 0.7 $\mu$s | $-I_{QT}$ | = max. 8<br>= max. 13.7 | mA<br>mA |

Transistor $TR_3$ non-conducting (output level "negative high")

| | | | |
|---|---|---|---|
| Voltage | $V_Q$ | = max. $V_N$ | |
| Current | $I_{QD}$ | = max. 0.65 (at $V_Q = 0.7\ V_N$) | mA |

Switching and delay times (when unit is used in combination with 1-Series circuit blocks)

A square wave input signal is assumed with an amplitude of min. $-0.7\ V_N$




Unit fully loaded

| | |
|---|---|
| Rise delay | $t_{rd}$ = max. 0.7 $\mu$s |
| Fall delay | $t_{fd}$ = max. 1.2 $\mu$s |
| Fall time | $t_f$ = max. 0.7 $\mu$s |

Note

- If for a particular application a capacitor is required between terminal W (2) and earth, use should be made of terminal 5 in order to avoid noise on the common earth point which could disturb the proper operation of the unit.

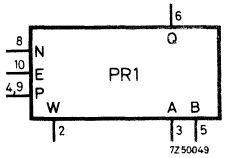
# POSITIVE RESET UNIT

Colour: blue

This unit is intended for resetting purposes of flip-flops FF 1, FF 2, FF 3 and FF 4. When a "negative low" level is applied to the input terminal (W), the unit produces a positive reset signal at its output terminal (Q). The time, that the reset level will be present, is determined by the driving circuit.
In general a reset time of maximum 2 $\mu$s per flip-flop is required when a chain of flip-flops is to be reset.
Up to 15 flip-flops can be reset without external interconnections. By interconnecting the terminals A and P the maximum number of flip-flops that can be reset is 30; by interconnecting the terminals B and P maximum 40 flip-flops can be reset simultaneously.

To reset a flip-flop the output terminal (Q) of the PR1 has to be connected to an input terminal (W) of a flip-flop via a diode OA 85 or OA 95 (anode to Q).

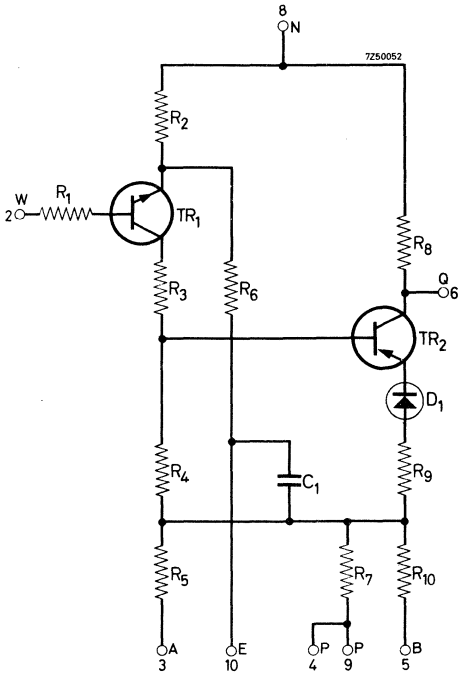
| | |
|---|---|
| Ambient-temperature range | −20 to +60 °C |
| Weight | approx. 20 g |




Drawing symbol

CIRCUIT DATA

Terminal 1 = not connected
2 = W = input
3 = A = to be interconnected with terminal 4 for resetting maximum 30 flip-flops
4 = P = supply + 6 V (internally connected to terminal 9)
5 = B = to be interconnected with terminal 4 for resetting maximum 40 flip-flops
6 = Q = output
7 = not connected
8 = N = supply −6 V
9 = P = supply +6 V
10 = E = common supply 0 V




Circuit diagram

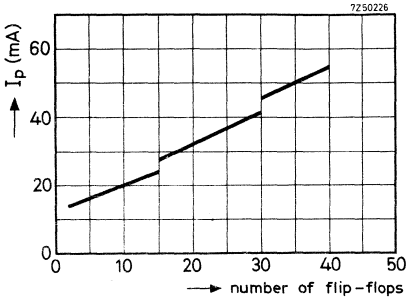
Power supply

Voltages

Terminal 8 : $V_N$ = −6 V ± 5%
9 : $V_P$ = +6 V ± 5%
10 : $V_E$ = 0 V common

Currents (at nominal voltage)

| | $I_N$ | $I_P$ |
|---|---|---|
| W-input at "1" level | −3.5 mA | 1.1 mA |
| W-input at "0" level | −7.5 mA | see diagram on next page. |




Notes

- The data given apply to the most adverse supply voltages for a combination of units, namely $V_N = -5.7$ V and $V_P = +6.3$ V.
- The temperatures −20 °C and +60 °C, and the tolerances on the supply voltages are absolute limiting values.
- When a current is flowing towards the unit, the positive sign is used.

INPUT DATA

Input signal (W-terminal)

A "negative low" level applied to the input terminal (W) produces a positive reset signal at the output terminal (Q).

Transistor TR2 conducting (reset condition)

| | | | |
|---|---|---|---|
| Voltage | $-V_W$ | = min. 0 | V |
| | | = max. 0.2 | V |
| limiting value | $V_W$ | = max. 6.5 | V |
| Required direct current | $I_{WD}$ | = min. 0.1 | mA |
| Required transient current averaged over 0.7 μs | $I_{WT}$ | = min. 0.08 | mA |

Transistor TR2 non-conducting

| | | | |
|---|---|---|---|
| Voltage | $-V_W$ | = min. 0.7 | $V_N$ |
| | | = max. | $V_N$ |

OUTPUT DATA

Transistor TR2 conducting (reset condition)

| | | | |
|---|---|---|---|
| Voltage | $V_Q$ | = min. 1.0 | V |
| Available direct current | $I_{QD}$ | = min. 15 | mA |
| A and P interconnected | | = min. 30 | mA |
| B and P interconnected | | = min. 40 | mA |

Transistor TR2 non-conducting

| | | | |
|---|---|---|---|
| Voltage | $-V_Q$ | = min. 0.5 | V |
| | | = max. | $V_N$ |

# ONE-SHOT MULTIVIBRATOR

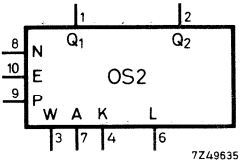
Colour : green

The unit OS2 contains a monostable multivibrator circuit equipped with medium-speed switching type transistors.

When a positive-going voltage step is applied to terminal A, the circuit generates a pulse at the Q-terminals.
The duration of the output pulse is determined by the value of:

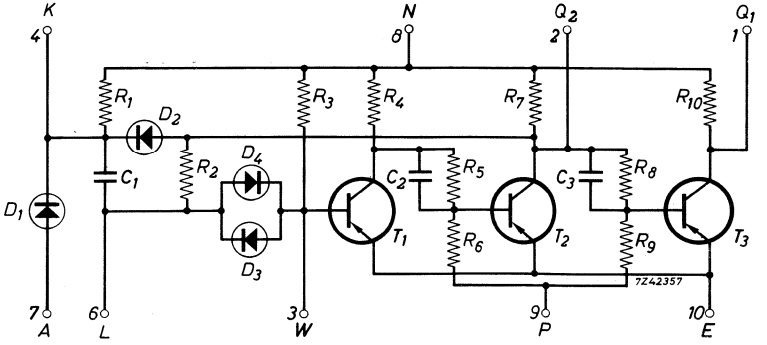
(a) the external capacitance parallel to $C_1$ between the terminals K and L (for pulses longer than the intrinsic value);
(b) the external resistance between the terminals $Q_1$ and W (for pulses shorter than the intrinsic value).

| | |
|---|---|
| Frequency range | 0 - 100 kHz |
| Permissible ambient temperature | -20 to +60 °C |
| Weight | approx. 20 g |




Drawing symbol

CIRCUIT DATA



Terminals

| | | | |
|---|---|---|---|
| 1 = $Q_1$ | = output 1 | 6 = L | = for external capacitor |
| 2 = $Q_2$ | = output 2 | 7 = A | = trigger input |
| 3 = W | = d.c. input | 8 = N | = supply (-6 V) |
| 4 = K | = for external capacitor | 9 = P | = supply (+6 V) |
| 5 = not connected | | 10 = E | = common of supply (0 V) |

Power supply

| | | |
|---|---|---|
| 8 : $V_N$ = -6 V ± 5 %, | $-I_N$ = 8.8 mA | nominal value |
| 9 : $V_P$ = +6 V ± 5 %, | $I_P$ = 0.4 mA | |
| 10 : $V_E$ = 0 V common | | |

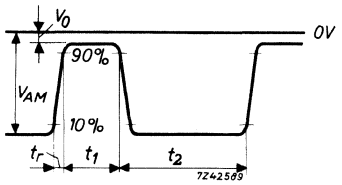
Notes

- The data given apply to the most adverse supply voltages for a combination of units, namely $V_N$ = -5.7 V and $V_P$ = 6.3 V.
- The temperatures -20 °C and +60 °C, and the tolerances on the supply voltages are absolute limiting values.
- When a current is flowing towards the unit, the positive sign is used.

## INPUT REQUIREMENTS

Trigger input signal (A terminal)

A positive-going voltage pulse is applied to terminal A. The leading edge of this voltage pulse drives by means of the transistor $T_1$ the transistor $T_2$ into the conducting, and the transistor $T_3$ into the non-conducting state.




Voltage levels

| | | | |
|---|---|---|---|
| $V_{AM}$ | = min. | -0.7 | $V_N$ |
| | = max. | | $-V_N$ |
| $-V_o$ | = min. | 0 | V |
| | = max. | 0.2 | V |

| | | | | |
|---|---|---|---|---|
| Required current during the transient | | | | |
| averaged over: 0.4 µs | $I_{AT}$ | = min. | 2.4 | mA |
| 0.7 µs | | = min. | 1.4 | mA |
| Required direct current 1) | $I_{AD}$ | = min. | 1.3 | mA |
| Rise time | | | | |
| without external capacitor | $t_r$ | = max. | 0.4 | µs |
| with a capacitor of min. 200 pF between terminals K and L | $t_r$ | = max. | 0.7 | µs |
| Duration of driving pulse | $t_1$ | = min. | 1 | µs |
| Recovery time | $t_2$ | = min. | 6 | µs 2) |
| when the duration of the output pulse ($t_o$) exceeds 7.5 µs | $t_2$ | = min. | 0.8 | $t_o$ 2) |
| Input noise level | $V_n$ | = max. | 1 | V peak to peak |

OUTPUT DATA

Voltages and currents

| Transistor conducting | | Output $Q_1$ | Output $Q_2$ |
|---|---|---|---|
| Voltage | $-V_Q$ | = max. 0.2 V | max. 0.2 V |
| Available direct current | $-I_{QD}$ | = max. 18 mA | max. 6 mA |
| Available current during the transient | | | |
| averaged over: 0.4 µs | $-I_{QT}$ | = max. 19 mA | max. 15 mA |
| 0.7 µs | | = max. 25 mA | max. 21 mA |

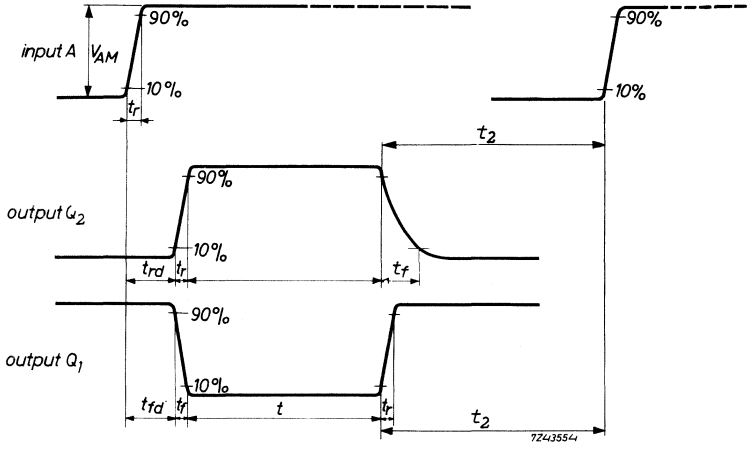
| Transistor non-conducting | | Output $Q_1$ | Output $Q_2$ |
|---|---|---|---|
| Voltage | $-V_Q$ | = min. $-0.7\,V_N$ | min. $-0.7\,V_N$ |
| Available direct current | $I_{QD}$ | = max. 0.7 mA | max. 0.25 mA |

1) This is the current flowing to the input of the OS2 during the input pulse after decay of the output pulse, if the duration of the input pulse is longer.

2) The recovery time $t_2$ is starting at the trailing edge ot $V_A$ when $t_1 > t_o$ and at the trailing edge of $V_{Q2}$ when $t_o > t_1$

## Switching and delay times

These data refer to an input signal as specified under "Input Data".




| Unit unloaded | | Output $Q_1$ | Output $Q_2$ |
|---|---|---|---|
| Rise delay | $t_{rd}$ = | - | $t_{rA}$ + max. 0.4 µs |
| Rise time | $t_r$ = | max. 0.2 µs | max. 0.2 µs |
| Fall delay | $t_{fd}$ = | $t_{rA}$ + max. 0.5 µs | - |
| Fall time | $t_f$ = | max. 0.4 µs | max. 3 µs |

## Duration of the output pulse

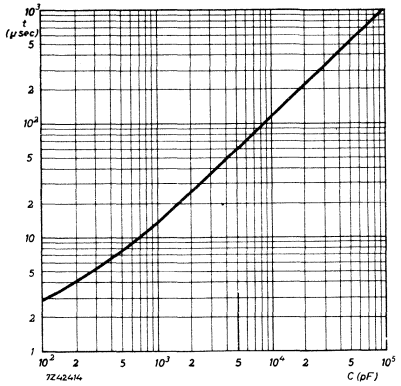
Unit unloaded

| | |
|---|---|
| Intrinsic value | $t_o$ = max. 4 µs |
| With resistor of 12 kΩ [1] between terminals $Q_1$ and W | $t_o$ = max. 2 µs |

With a capacitor between terminals K and L, at an ambient temperature of 25 °C and supply voltages $V_N$ = -6 V and $V_P$ = +6 V, see figure given below.

For larger capacitances log t is proportionate to log C.

[1]) minimum permissible value




Stability of pulse duration

A variation of the supply voltage $V_N$ of 5 % varies the pulse duration by less than 1 % in the same direction.

The influence of a variation of the supply voltage Vp of 5 % is negligible.

An increase in ambient temperature by 1 °C gives a reduction of the pulse duration of less than 0.5 % and vice versa.

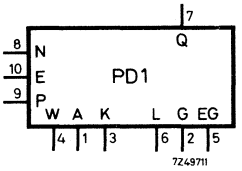
Note. In case an electrolytic capacitor is used for $C_{ext}$ care should be taken that its + terminal is connected to terminal 6.

# PULSE DRIVER

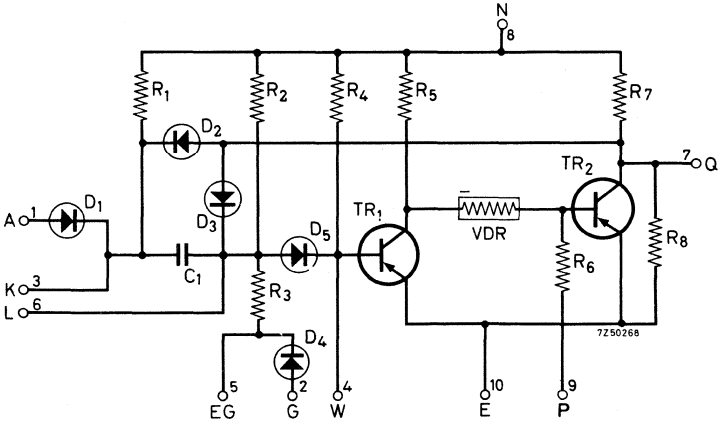
Colour: green

The unit PD1 contains a monostable multivibrator with a built-in trigger gate. It is mainly intended as a clock source, delivering trigger pulses for a great number of flip-flops FF1, FF2, FF3, and FF4 or as a counter driver.
The trigger gate can be controlled by a d.c. voltage level applied to terminal G.
The number of condition inputs can be extended with the aid of external diodes OA85/OA95 at the extension input E.G.
When a positive-going voltage step is applied to terminal A, the unit generates a pulse at the output (Q)-terminal, provided the gate is open.
The duration of the output pulse can be increased by means of an external capacitor between the terminals K and L (for pulses longer than the intrinsic value, e.g. necessary when driving a FF4 or 2PL2).
For mounting in the chassis 4322 026 38240 a printed-wiring board PDA 1, catalogue number 4322 026 34710, is available. On this standard printed-wiring board up to four PD 1's can be mounted (see section "ACCESSORIES FOR CIRCUIT BLOCKS 1-SERIES").

| | | |
|---|---|---|
| Frequency range | : | see INPUT DATA |
| Permissible ambient temperature | : | -20 to +60 °C |
| Weight | : | approx. 20 g |




Drawing symbol



## CIRCUIT DATA

Terminal
1 = A = trigger input
2 = G = gate input
3 = K = for external capacitor
4 = W = d.c. input
5 = EG = extension gate input
6 = L = for external capacitor
7 = Q = output
8 = N = supply -6 V
9 = P = supply +6 V
10 = E = common supply 0 V

### Power supply

Terminal 8: $V_N$ = -6 V ± 5 %, $-I_N$ = 26 mA ($T_1$ conducting)
= 51 mA ($T_2$ conducting)
9: $V_P$ = +6 V ± 5 %, $I_P$ = 0.4 mA
10: $V_E$ = 0 V common

Notes

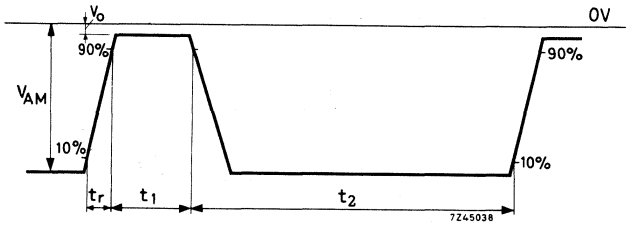
- The data given apply to the most adverse supply voltages for a combination of units, namely $V_N$ = -5.7 V and $V_P$ = 6.3 V.
- The temperatures -20 °C and +60 °C, and the tolerances on the supply voltages are absolute limiting values.
- When a current is flowing towards the unit, the positive sign is used.

## INPUT DATA

### Input Signal Requirements

Trigger Input Signal (A terminal)

A positive-going voltage step is applied to input terminal A. This voltage step generates a pulse at the output Q if the gate has been opened by an appropriate gate input signal on terminal G.




Voltage

$V_{AM}$ = min. -0.7 $V_N$
= max. - $V_N$
$-V_o$ = min. 0 V
= max. 0.2 V

| | |
|---|---|
| Required direct current | $I_{AD}$ = min. 1.7 mA |
| Required average current during the transient | $I_{AT}$ = min. 1.5 mA (practically independent of rise time) |
| Rise time | $t_r$ = max. 0.7 µs |
| Pulse duration | $t_1$ = min. 1 µs |
| Recovery time | $t_2$ = min. 6 µs (without external capacitor) |
| | $t_2$ = min. 11 µs (with $C_{EXT}$ = 1000 pF between terminals K and L) |
| Note | Type of diodes and maximum number to be connected in parallel at terminal K: 6 x OA85/OA95. |

Input Impedance:

Equivalent to a capacitance of 500 pF.

Gate Input Signals (G-terminals)

A d.c. voltage level is applied to terminal G. A "negative low" voltage opens the gate.

| | | Gate open | Gate closed |
|---|---|---|---|
| Voltage | $-V_G$ | = min. 0 V | min. - 0.7 $V_N$ |
| | | max. 0.2 V | max. - $V_N$ |
| Required gate current caused by negative transient of $V_A$ | $I_{GD}$ | = min. 1.75 mA | min. 0.5 mA |
| Required average current during the positive transient of $V_G$ | $I_{GT}$ | = min. 1.2 mA | |

Gate Setting Times:

| When the gate changes at random: | | to open gate | to close gate |
|---|---|---|---|
| Without external capacitor | $t_{gs}$ | = min. 8.5 µs | min. 25 µs |
| With an external capacitor of 1000 pF between K and L | | = min. 24 µs | 75 µs |

| | | to open gate | to close gate |
|---|---|---|---|
| When the gate level changes within 1 µs after the positive going edge of the trigger signal: | | | |
| Without external capacitor | $t_{gs}$ | = min. 6 µs | 0 |
| With external capacitor of 1000 pF between K and L | | = min. 11 µs | 0 |

Notes

- The gate setting time is the time the gate (G)-signal shall be present in advance to open the gate for the trigger (A) -signal.
- The absolute maximum value of the external capacitor is 1000 pF.
- Type of diodes and maximum number to be connected in parallel at terminal EG: 6 x OA85/OA95.

W-terminal (base connection transistor T1):

Transistor $T_1$ non-conducting:

| | |
|---|---|
| Voltage limiting value | $V_W$ = min. 0.2 V<br>$V_W$ = max. 2.5 V<br>These voltages may be applied for max. 5 µs and a max.freq. of 100 kHz |

Transistor $T_1$ conducting:

| | |
|---|---|
| Current (limiting value) | $-I_W$ = max. 2 mA<br>(at $-V_W$ = max. 0.5 V) |

Up to max.6 output-Q terminals of pulse logic units 2.PL2 may be connected to the W-input terminal of the PD 1 each via a resistor of 560 Ω ± 5%.

OUTPUT DATA

Voltages and Currents

Transistor conducting:

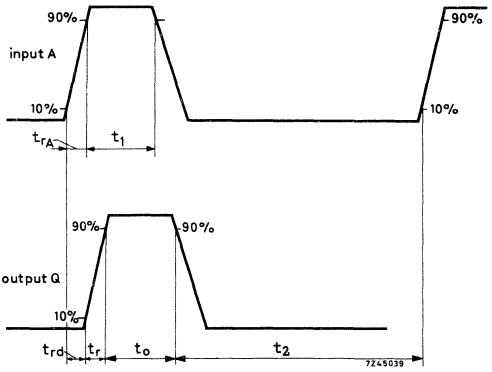
| | | | |
|---|---|---|---|
| Voltage | $-V_Q$ | = max. 0.2 | V |
| Available direct current | $-I_{QD}$ | = max. 65 | mA |
| Available current during the transient: averaged over 0.7 µs | $-I_{QT}$ | = max. 90 | mA |

Transistor non-conducting:

Voltage $-V_Q$ = min. - 0.7 $V_N$
= max. - 0.84 $V_N$

Switching and Delay Times:

These data are for orientation only and refer to an input signal as specified under INPUT DATA.




$t_{rd} = t_{rA} + 0.2$ µs
(fully loaded)

| Unit max. loaded with: | $t_r + t_o$: | ext. capacitor between terminals K and L: |
|---|---|---|
| 20 x FF1 or FF2 | max. 1.5 µs | none |
| 5 x FF3 | min. 1.2 µs | none |
| 20 x FF3 | max. 2 µs | none |
| 20 x FF4 (at 70 kHz) | max. 4 µs | $C_{ext}$ = 1000 pF ± 5% (absolute max. value of $C_{ext}$). |

The recovery time $t_2$ is starting at the trailing edge of $V_A$ when $t_1 > t_o$ and at the trailing edge of $V_Q$ when $t_o > t_1$ ($t_1$ = duration of input pulse $V_A$).

The typical output pulse duration of an unloaded pulse driver PD 1, triggered via a PL 2 unit (at 70 kHz): $t_r + t_o = 3.2$ µs.

# POWER AMPLIFIER

The PA1 consists of an n-p-n/p-n-p transistor amplifier circuit, designed to be used as a power amplifier in the range of circuit blocks. The amplifier is non-inverting, and can be driven directly by the circuit blocks FF1, FF2, FF3, FF4, GI1, IA1, IA2 and OS2

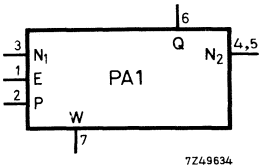
The output loadability is 600 mA at 60 V (abs. max. values). The built-in diode across the output terminals protects the output transistor against voltage transients which occur when the unit is driving an inductive load.

The circuit is mounted on an epoxy-paper printed-wiring board, the output transistor is provided with an aluminium heat sink.

Frequency range : 0-100 Hz

Ambient temperature range: -20 to +60 °C

Weight : approx. 60 g




CIRCUIT DATA

Terminal: 1 = E = common supply 0 V

2 = P = supply +6 V

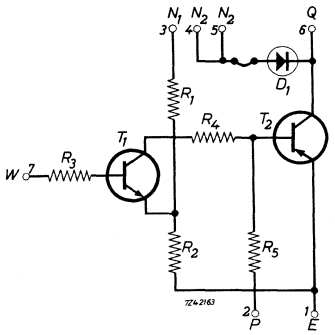
3 = N1 = supply -6 V

4 = N2 } = supply abs. max. 60 V

5 = N2 }

6 = Q = output

7 = W = input




Power Supply

Terminal: 1: $V_E$ = 0 V common

2: $V_P$ = 6 V ± 10 %, $I_P$ = max. 20 mA 1) 2)

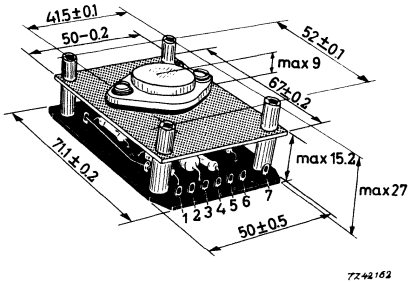
3: $V_{N1}$ = -6 V ± 10 %, $-I_{N1}$ = max. 70 mA ($T_2$ non-conducting)
= max. 110 mA ($T_2$ conducting)

4) 5) $V_{N2}$ = max. 60 V, $-I_{N2}$ = max. 600 mA 1) 2)

1) The sign is positive when the current flows towards the unit.

2) When $-V_{N2}$ is applied to the unit, care must be taken that Vp is present as well, otherwise transistor T2 may be damaged.

## MECHANICAL CONSTRUCTION




The dimensions (approx. 71 mm x 50 mm x 27 mm) and terminal location can be seen from the figure given above. Since the aluminium heat sink is insulated from the circuit, no special measures need be taken as regards mounting of the unit.

In the mounting chassis 4322 026 38240 the PA 1 is to be mounted directly on a printed-wiring board. On such a standard printed-wiring board PAA 1 up to four PA 1's can be mounted, the next position in the chassis being left empty.
To ensure proper cooling of the unit, the PA 1 has to be mounted in such a way that a free flow of air through it is guaranteed.

## INPUT DATA

Input Signal Requirements 2)

A d.c. voltage level is applied to terminal W.

Output-transistor conducting

| | | | |
|---|---|---|---|
| Voltage | $-V_w$ | = | max. 0.2 V<br>min. 0 V |
| Current | $I_w$ | = | min. 2.5 mA 1) |

Output-transistor non-conducting

| | | | |
|---|---|---|---|
| Voltage | $-V_w$ | = | min. 4.25 V |
| Limiting value | | = | max. 13.2 V |
| Current | $-I_w$ | = | min. 0.1 mA 1) |

## OUTPUT DATA

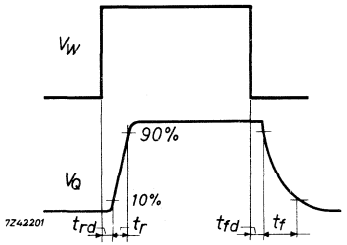
Output Signal Characteristics 2)

Output transistor conducting

| | | | |
|---|---|---|---|
| Voltage | $-V_Q$ | = | max. 0.75 V |
| Load current | $-I_Q$ | = | max. 600 mA 1) |

Output transistor non-conducting

| | | | |
|---|---|---|---|
| Voltage | $-V_Q$ | = | max. 60 V (dependent on the value of $V_{N2}$ which is abs. max. 60 V.) |
| Leakage current | $-I_Q$ | = | max. 14.5 mA 1) |




1) The sign is positive when the current flows towards the unit.

2) These data apply to the most adverse working conditions for a combination of units, namely to supply voltages $V_N$ = -5.4 V and $V_p$ = +6.6 V. Unless differently specified, all the voltage and current figures quoted represent absolute maximum values.

Switching and Delay Times (for orientation only)

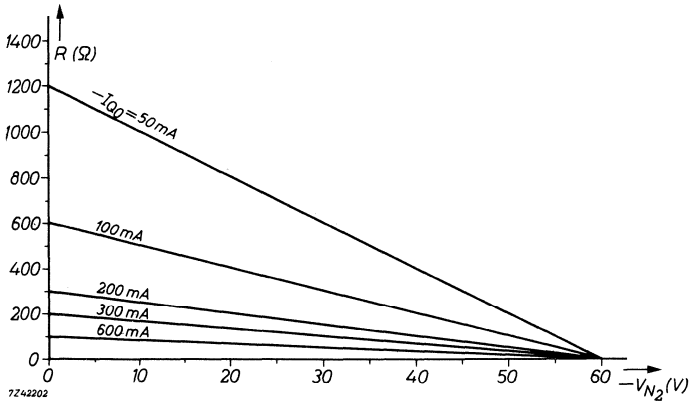
A square wave input signal is applied with an amplitude of 4.25 V, a rise time of max. 2.2 µs and a fall time of max. 2.5 µs

Unit loaded with a resistor of 100 Ω

| | | | |
|---|---|---|---|
| Rise delay | $t_{rd}$ | = max. | 15 µs |
| Rise time | $t_r$ | = max. | 120 µs |
| fall delay | $t_{fd}$ | = max. | 70 µs |
| fall time | $t_f$ | = max. | 60 µs |

Unit loaded with an inductive load

The unit is provided with a built-in diode to protect the output transistor against voltage transients which occur when an inductive load is switched. This protection is realised at the expense of a very long fall delay time of the current in this load. At supply voltages below 60 V, however, a wire jumper in series with this diode can be interchanged with a resistor to decrease this delay time.
The maximum permissible value of this resistor is given in the figure below, with the current flowing through the load at the moment of switching-off as parameter.



# DUAL DECADE COUNTER

The unit 2.DCA 2 contains two identical decade counter units, mounted on a printed wiring board. Each counter consists of four flip-flops FF3, connected to operate in the 1-2-4-8 code. To achieve this operation, it is provided with a gate-diode with the result that six of the sixteen possible positions are skipped. The flip-flops can be reset by means of a common positive signal.

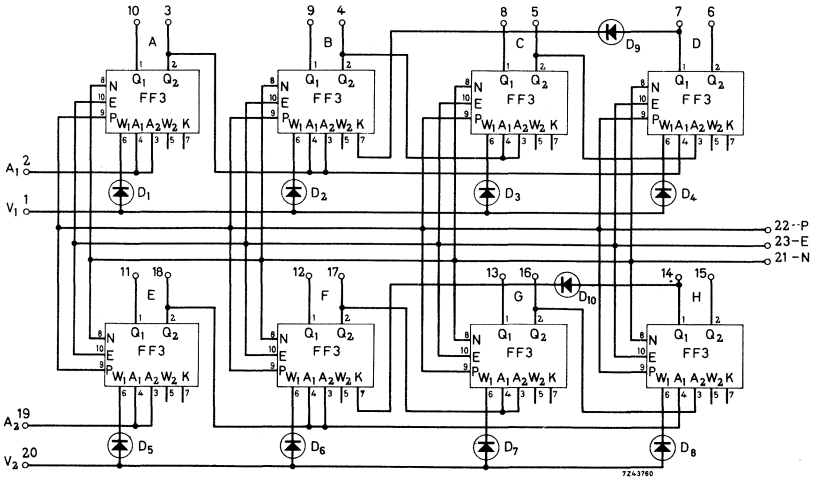
The reset diodes $D_1$ up to $D_8$ inclusive and the gate-diodes $D_9$ and $D_{10}$ are mounted on the printed wiring board as well.

The printed wiring board is provided with plated-through holes and single-sided gold-plated contacts.

With the mating connector, 2422 020 52592, not supplied with the dual decade counter, the printed wiring board of standard dimensions (121.8mm x x 180.3mm x 1.6mm) can be used directly in the standard mounting chassis, catalog number 4322 026 38240.

The fixation of the circuit blocks FF3 to the p.w. board is secured by means of locking tags, catalog number 4322 026 33690.

| | |
|---|---|
| Pulse repetition frequency range: | 0 - 100 kHz |
| Ambient temperature range: | -20 to +60 °C |
| Weight: | approx. 210 g |




Terminal

| | |
|---|---|
| 1 = $V_1$ = reset input counter 1 | 13 = $Q_{1G}$ = output 1 flip-flop G |
| 2 = $A_1$ = a.c. input counter 1 | 14 = $Q_{1H}$ = output 1 flip-flop H |
| 3 = $Q_{2A}$ = output 2 flip-flop A | 15 = $Q_{2H}$ = output 2 flip-flop H |
| 4 = $Q_{2B}$ = output 2 flip-flop B | 16 = $Q_{2G}$ = output 2 flip-flop G |
| 5 = $Q_{2C}$ = output 2 flip-flop C | 17 = $Q_{2F}$ = output 2 flip-flop F |
| 6 = $Q_{2D}$ = output 2 flip-flop D | 18 = $Q_{2E}$ = output 2 flip-flop E |
| 7 = $Q_{1D}$ = output 1 flip-flop D | 19 = $A_2$ = a.c. input counter 2 |
| 8 = $Q_{1C}$ = output 1 flip-flop C | 20 = $V_2$ = reset input counter 2 |
| 9 = $Q_{1B}$ = output 1 flip-flop B | 21 = N = common negative supply |
| 10 = $Q_{1A}$ = output 1 flip-flop A | 22 = P = common positive supply $^{-6V}_{+6V}$ |
| 11 = $Q_{1E}$ = output 1 flip-flop E | 23 = E = common supply 0V |
| 12 = $Q_{1F}$ = output 1 flip-flop F | |

Power Supply

Terminal 21: $V_N = -6V \pm 5\%$, $-I_N = 70mA$

22: $V_P = +6V \pm 5\%$, $I_P = 4.8mA$

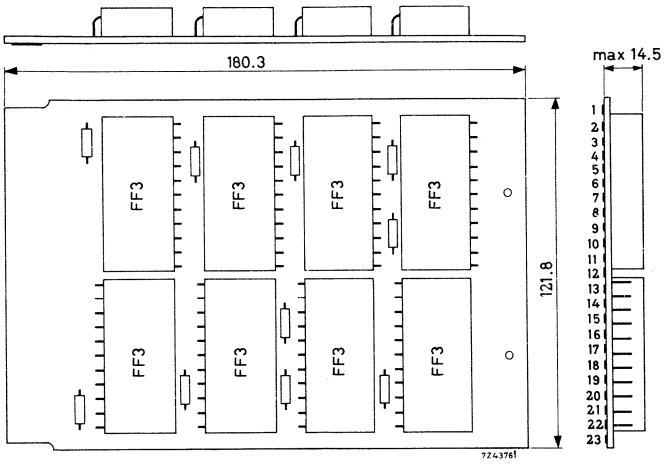
23: $V_E = 0V$

} Nominal value of the current

Notes:

- When a current is flowing towards the unit, the positive sign is used
- The data given apply to the most adverse supply voltages for a combination of units, namely
  $V_N = -5.7V$ and $V_P = +6.3V$
- The temperatures -20 °C and +60 °C, and the tolerances on the supply voltages are absolute limiting values.

Dimensions and Terminal Location

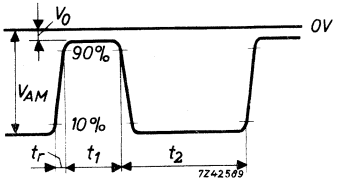



INPUT DATA

Input Signal Requirements

Trigger Input Signal ($A_1$ and/or $A_2$ terminals)

A positive-going voltage step is applied to terminal A. This voltage step advances the counter one position.



| | | | |
|---|---|---|---|
| Voltage | $V_{AM}$ | = min. | $-0.7V_N$ |
| | | = max. | $-V_N$ |
| | $-V_0$ | = min. | 0V |
| | | = max. | 0.2V |
| Required direct current | $I_{A1D}(I_{A2D})$ | = min. | 1.75mA |
| Required current during the transient averaged over 0.4μs | $I_{A1T}$ $(I_{A2T})$ | = min. | 6mA |
| 0.7μs | | = min. | 4.5mA |
| Rise time | $t_r$ | = max. | 0.7μs |
| Pulse duration | $t_1$ | = min. | 1μs |
| | $t_2$ | = min. | 8μs |
| Input noise level | $V_n$ | = max. | 1V peak to peak |

Reset Input Signal ( $V_1$ and/or $V_2$ terminals)

For resetting the counter a positive d.c.voltage is applied to terminal V. This signal causes all $Q_1$-terminals to reach a "negative-high" and all $Q_2$-terminals to reach a "negative-low" level.

Input level during reset

| | | | |
|---|---|---|---|
| Voltage | $V_{v1}$ $(V_{v2})$ | = min. | 1V |
| | | = max. | 10V |
| Current | $I_{v1}$ $(I_{v2})$ | = min. | 3.6 mA |

During counting it is recommended that terminal $V_1$ and/or $V_2$ are connected to a voltage level.

| | | | |
|---|---|---|---|
| Voltage | $-V_{v1}$ $(-V_{v2})$ | = min. | 0.4V |
| | | = max. | 15V |
| Current | $-I_{v1}$ $(-I_{v2})$ | = min. | 0.12mA (at $-V_{v1}$ $(-V_{v2})$ = 0.4V) |

OUTPUT DATA

These data apply to the various flip-flop stages.

## Output Signal Characteristics

### Transistor non-conducting

Voltage: $-V_Q$ = min. $-0.7V_N$

Available direct current $I_{QD}$ = max. 0.7mA

### Transistor conducting

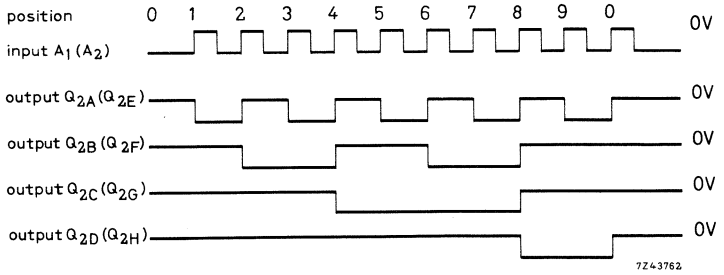
Voltage $-V_Q$ = max. 0.2V
= min. 0V

| | | output $Q_1$ | | output $Q_2$ | | | |
|---|---|---|---|---|---|---|---|
| | | Flip-Flop A-B-C E-F-G- | Flip-Flop D-H | Flip-Flop A-E | Flip-Flop B-F | Flip-Flop C-G | Flip-Flop D-H |
| max. available current during transient $-I_{QT}$ | averaged over 0.4 µs | 11mA | 11mA | 4mA | 5mA | 6mA | 11mA |
| | averaged over 0.7 µs | 14mA | 14mA | 9mA | 9.5mA | 10mA | 14mA |
| maximum available direct current $-I_{QD}$ | | 6mA | 5.1mA | 3.4mA | 4.25mA | 5.1mA | 6mA |

### Maximum Speed:

For all loads within the limits mentioned above, also applied simultaneously, the maximum counting speed of 100 kHz is guaranteed.

### Output levels during counting




The output levels at the $Q_2$-terminals are shown in the figure above.
Note that when a $Q_2$ output is at "negative-low" level the corresponding $Q_1$ output is at "negative-high" level and vice versa.
After 10 positive-going voltage steps at the input terminal $A_1$ ($A_2$), the output terminal $Q_{2D}$ ($Q_{2H}$) delivers one positive-going voltage step, whilst the decade counter has resumed its initial position, namely all $Q_2$-terminals being at 0V level.

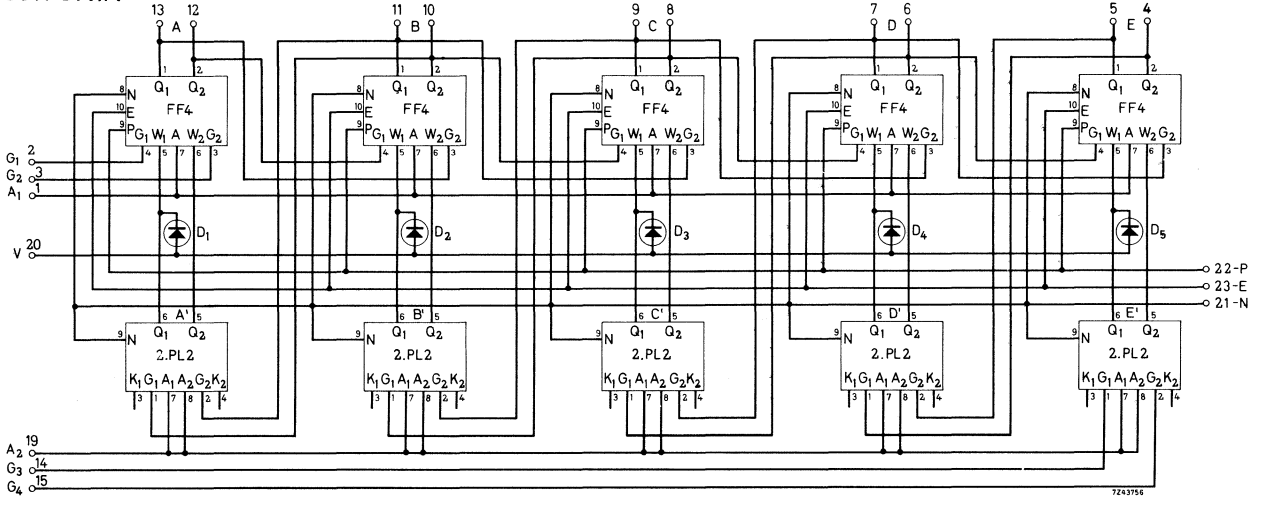
# REVERSIBLE COUNTER

The unit BCA 1 consists of five flip-flops FF4 and five dual pulse logic's 2.PL2, mounted on a printed-wiring board, interconnected to operate as a bi-directional shift register. A bi-directional decade counter can be realised by interconnecting the gate (G)-terminals of the first flip-flop with the output (Q)-terminals of the fifth flip-flop and the gate (G)-terminals of the fifth dual pulse logic with the output (Q)-terminals of the first flip-flop. These interconnections have to be made externally in such a way that the Q1- respectively Q2-terminal has to be connected with the corresponding $G_1$- respectively $G_2$-terminal.

The flip-flops can be reset by means of a common positive signal. The five reset diodes $D_1$ up to $D_5$ inclusive are mounted on the printed-wiring board as well. The printed-wiring board is provided with plated through holes and single sided gold plated contacts.
With the mating connector catalog number 2422 020 52592, not supplied with the reversible counter, this printed-wiring board of standard dimensions (121.8 mm x 180.3 mm x 1.6 mm) can be used directly in the standard mounting chassis catalog number 4322 026 38240. The fixation of the circuit blocks FF4 and 2.PL2 is secured by means of locking tags catalog number 4322 026 33690.

| | |
|---|---|
| Pulse repetition frequency range: | 0 - 70 kHz |
| Ambient temperature range: | −20 to +60 °C |
| Weight: | approx. 250 g |

## CIRCUIT DATA




Terminal

| | | | | | |
|---|---|---|---|---|---|
| 1 = $A_1$ | = a.c. input forward direction | 9 = $Q_{1C}$ | = output 1 flip-flop C | 16 = not connected | |
| 2 = $G_1$ | = gate input ($G_1$) flip-flop A | 10 = $Q_{2B}$ | = output 2 flip-flop B | 17 = not connected | |
| 3 = $G_2$ | = gate input ($G_2$) flip-flop A | 11 = $Q_{1B}$ | = output 1 flip-flop B | 18 = not connected | |
| 4 = $Q_{2E}$ | = output 2 flip-flop E | 12 = $Q_{2A}$ | = output 2 flip-flop A | 19 = $A_2$ | = a.c. input reverse direction |
| 5 = $Q_{1E}$ | = output 1 flip-flop E | 13 = $Q_{1A}$ | = output 1 flip-flop A | 20 = V | = reset input |
| 6 = $Q_{2D}$ | = output 2 flip-flop D | 14 = $G_3$ | = gate input ($G_1$) dual pulse logic E' | 21 = N | = common negative supply -6V |
| 7 = $Q_{1D}$ | = output 1 flip-flop D | | | 22 = P | = common positive supply +6V |
| 8 = $Q_{2C}$ | = output 2 flip-flop C | 15 = $G_4$ | = gate input ($G_2$) dual pulse logic E' | 23 = E | = common supply 0V |

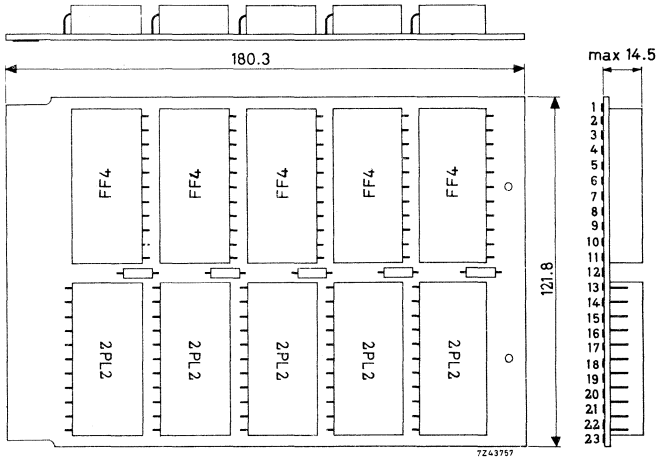
Power Supply

Terminal 21: $V_N = -6V \pm 5\%$, $-I_N = 55mA$
22: $V_P = +6V \pm 5\%$, $I_P = 3mA$
} Nominal value of the current
23: $V_E = 0V$

Notes

- When a current is flowing towards the unit, the positive sign is used
- The data given apply to the most adverse supply voltages for a combination of units, namely
  $V_N = -5.7V$ and $V_P = +6.3V$
- The temperatures $-20°C$ and $+60°C$ and the tolerances on the supply voltages are absolute limiting values

Dimensions and terminal location



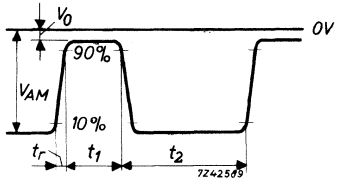

INPUT DATA

Input Signal Requirements

Trigger Input Signal ($A_1$ or $A_2$ terminal)

A positive-going voltage step is applied to terminal A. When this voltage step is applied to terminal $A_1$ the counter advances one position, when it is applied to terminal $A_2$ the counter reverses one position.

Voltage $V_{AM}$ = min. $-0.7V_N$
= max. $-V_N$
$-V_0$ = min. 0V
= max. 0.2V




| | |
|---|---|
| Required direct current | $I_{A1D}$ ($I_{A2D}$) = min. 8.8mA |
| Required current during the transient: averaged over 0.4 µs | $I_{A1T}$ ($I_{A2T}$) = min. 30mA |
| 0.7 µs | = min. 22.5mA |
| Rise time | $t_r$ = max. 0.7 µs |
| Pulse duration | $t_1$ = min. 3 µs |
| | $t_2$ = min. 11 µs |
| Input noise level | $V_n$ = max. 1V p-p |

Gate Input Signal ($G_1$ and $G_2$ or $G_3$ and $G_4$ terminals)

A d.c. voltage level is applied to these G-terminals

| | gate open | gate closed |
|---|---|---|
| Voltage | $-V_G$ = min. 0V | min. $V_{AM}$ |
| | = max. 0.2V | max. $-V_N$ |
| Required gate current caused by negative transient of $V_{AM}$ | $I_{GD}$ = min. 1.75mA | min. 1.2 mA |
| Required average current during the positive transient of $V_G$ | $I_{GT}$ = min. 1.6mA | |
| Gate setting time | | |
| when the gate input level changes at random | $t_{GS}$ = min. 17 µs | min. 25 µs |
| when the gate input level changes within 2 µs after the positive going edge of the trigger signal | $t_{GS}$ = min. 11 µs | min. 11 µs |

Notes

- The latter applies to the shift register configuration so that the max. shift frequency is approximately 70 kHz
- During triggering the G levels should not be at zero voltage level simultaneously
- The gate setting time is the required waiting time between the last G level change and the positive-going edge of the trigger pulse

Reset Input Signal (V-terminal)

For resetting the counter a positive d.c. voltage is applied to terminal V. This signal causes all $Q_1$-terminals to reach a "negative high" and all $Q_2$-terminals to reach a "negative low" level.

Input Level during Reset

| | |
|---|---|
| Voltage | $V_v$ = min. 1 V |
| | = max. 10 V |
| Current | $I_v$ = min. 4.5 mA |

During shifting it is recommended that terminal V is connected to a voltage level:

| | |
|---|---|
| Voltage | $-V_v$ = min. 0.4 V |
| | = max. 15 V |
| Current | $-I_v$ = min. 0.15 mA (at $-V_v$ = 0.4 V) |

OUTPUT DATA

These data apply to the various flip-flop stages:

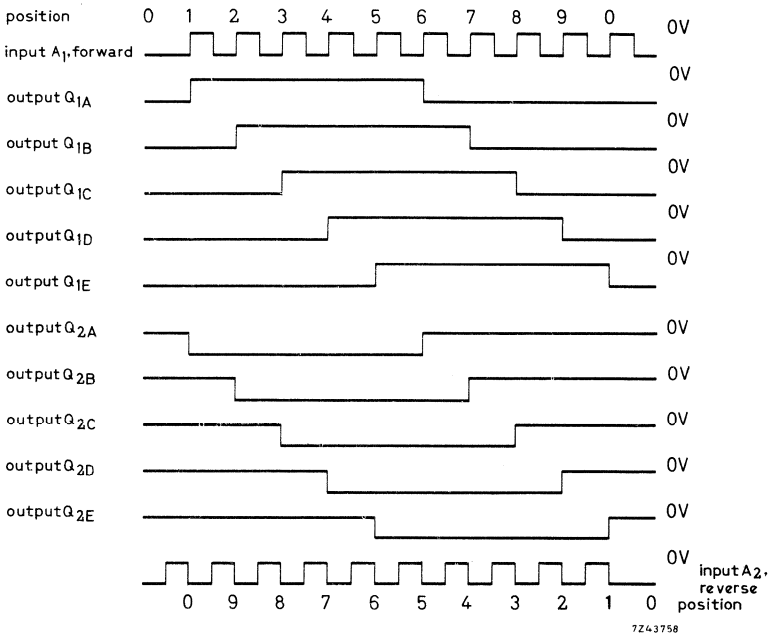
Output Signal Characteristics

| | |
|---|---|
| Transistor non-conducting | |
| Voltage | $-V_Q$ = min. $-0.7V_N$ |
| Available direct current | $I_{QD}$ = max. 0.7 mA |
| Transistor conducting | |
| Voltage | $-V_Q$ = max. 0.2 V |
| | = min. 0 V |

| | | flip-flops B-C-D | flip-flops A-E |
|---|---|---|---|
| available current during the transient $-I_{QT}$ | averaged over 0.4 µs | max. 8 mA | max. 9.4 mA |
| | averaged over 0.7 µs | max. 11 mA | max. 12.4 mA |
| available direct current $-I_{QD}$ | | max. 3.75 mA | max. 4.25 mA |

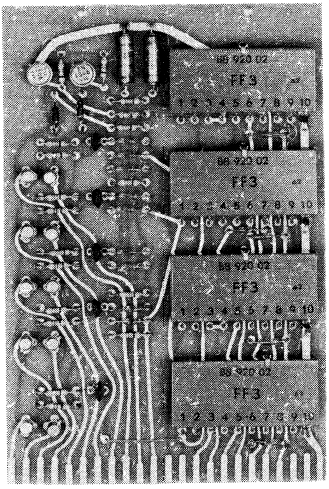
These current data apply to the unit, operating as a bi-directional shift register. When the unit is interconnected to form a bi-directional decade counter the lowest current values of $-I_{QT}$ and $-I_{QD}$ are valid for all flip-flops.

Output levels during counting, when the unit is externally interconnected to form a bi-directional decade counter. To this end terminals 2 and 5, 3 and 4, 12 and 15, 13 and 14 have to be connected.
The output levels at the Q-terminals can be taken from the figure below.




Note that after 10 positive-going voltage steps at the input terminal $A_1$ ($A_2$), the output terminal $Q_{2E}$ ($Q_{2A}$) delivers one positive-going voltage step, whilst the decade counter has retaken its initial position, namely all $Q_2$-terminals being at 0V level.

# DECADE COUNTER AND NUMERICAL INDICATOR TUBE DRIVER ASSEMBLY



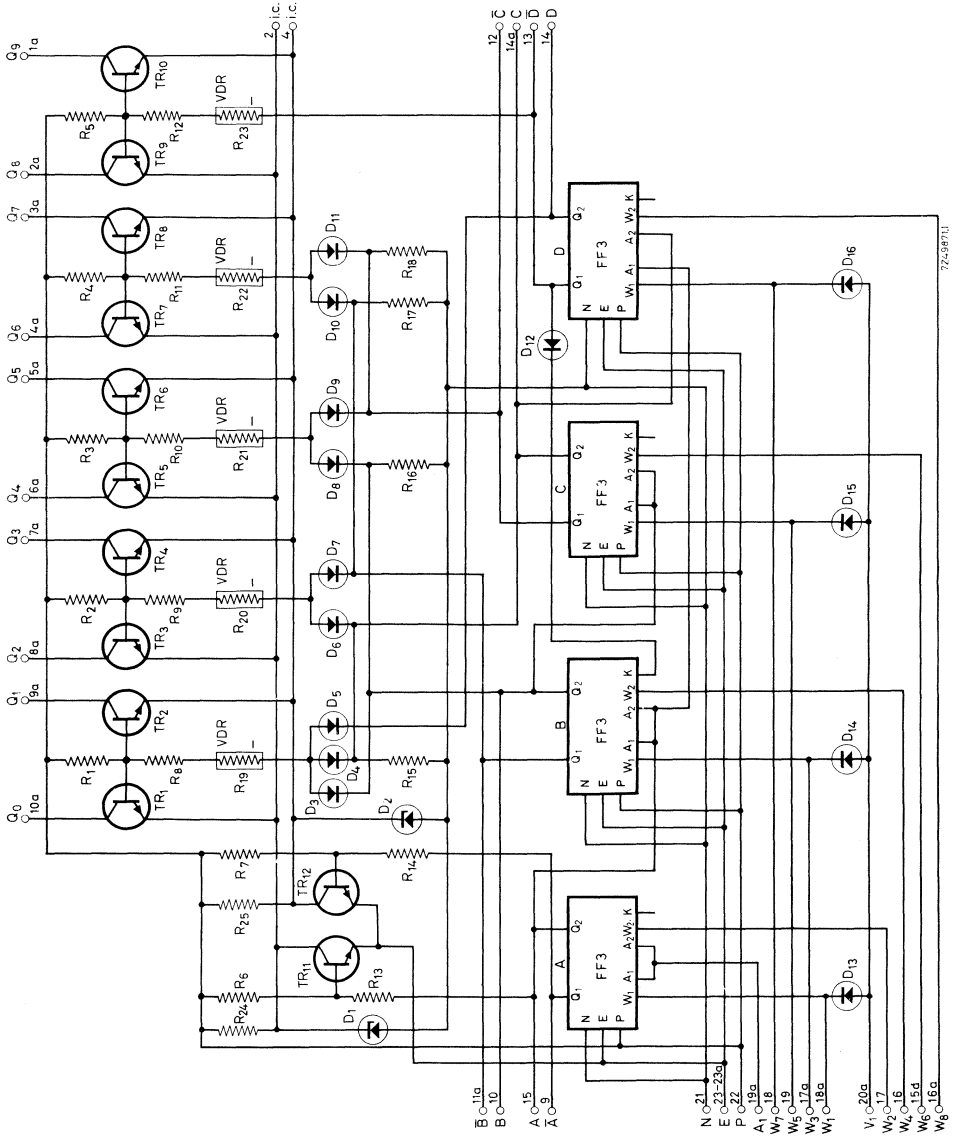

RZ 22603-6

This assembly contains one decade counter together with the decoding and driving circuits for the numerical indicator tubes ZM 1000, ZM 1020, ZM 1040 or ZM 1080, mounted on a printed-wiring board.
The counter consists of four flip-flops FF 3 (catalog number 2722 001 00021), connected to operate in the 1-2-4-8 code. The flip-flops can be reset by means of a common positive signal; the reset diodes $D_1$ up to and including $D_4$ are mounted on the printed-wiring board as well.

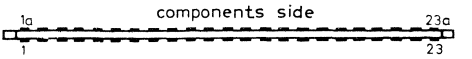
The printed-wiring board, provided with plated-through holes and double-sided goldplated contacts, is made of glass-epoxy material.
With the mating connector, catalog number 2422 020 52591, (not supplied with the DCA3), this printed-wiring board of standard dimensions (121.8 mm x 180.3 mm x 1.6 mm), can be used directly in the standard mounting chassis (catalog number 4322 026 38240).
The circuit blocks FF 3 are secured to the printed-wiring board by means of locking tags (catalog number 4322 026 33690).

| | | |
|---|---|---|
| Pulse repetition frequency range | : | 0 - 100 kHz |
| Ambient-temperature range | : | −20 to +60 °C |
| Weight | : | approx. 150 g |

CIRCUIT DATA



Terminals




1 = not connected
2 = internal connection
3 = not connected
4 = internal connection
5 = not connected
6 = not connected
7 = not connected
8 = not connected
9 = $\overline{A}$ = $Q_{1A}$ = output 1 flip-flop A
10 = B = $Q_{2B}$ = output 2 flip-flop B
11 = not connected
12 = $\overline{C}$ = $Q_{1C}$ = output 1 flip-flop C
13 = $\overline{D}$ = $Q_{1D}$ = output 1 flip-flop D
14 = D = $Q_{2D}$ = output 2 flip-flop D
15 = A = $Q_{2A}$ = output 2 flip-flop A
16 = $W_4$ = $W_2$ of flip-flop B
17 = $W_2$ = $W_2$ of flip-flop A
18 = $W_7$ = $W_1$ of flip-flop D
19 = $W_5$ = $W_1$ of flip-flop C
20 = not connected
21 = N = common negative supply −6 V
22 = P = common positive supply +6 V
23 = E = common supply 0 V

1a = $Q_9$ = digit number 9
2a = $Q_8$ = digit number 8
3a = $Q_7$ = digit number 7
4a = $Q_6$ = digit number 6
5a = $Q_5$ = digit number 5
6a = $Q_4$ = digit number 4
7a = $Q_3$ = digit number 3
8a = $Q_2$ = digit number 2
9a = $Q_1$ = digit number 1
10a = $Q_o$ = digit number 0
11a = $\overline{B}$ = $Q_{1B}$ = output 1 flip-flop B
12a = not connected
13a = not connected
14a = C = $Q_{2C}$ = output 2 flip-flop C
15a = $W_6$ = $W_2$ of flip-flop C
16a = $W_8$ = $W_2$ of flip-flop D
17a = $W_3$ = $W_1$ of flip-flop B
18a = $W_1$ = $W_1$ of flip-flop A
19a = $A_1$ = a.c. input counter
20a = $V_1$ = reset input counter
21a = not connected
22a = not connected
23a = E = common supply 0 V

Power supply

Terminal 21 : $V_N$ = −6 V ±5 %, $-I_N$ = 42 mA } nominal value
22 : $V_P$ = +6 V ±5 %, $I_P$ = 8.8 mA } of the current
23 = 23A : $V_E$ = 0 V

Notes

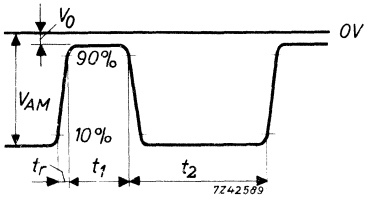
- The data given apply to the most adverse supply voltages for a combination of units, namely $V_N$ = −5.7 V and $V_P$ = +5.7 V.
- The temperatures −20 °C and +60 °C and the tolerances on the supply voltages are absolute limiting values.
- When a current is flowing towards the unit, the positive sign is used.

INPUT DATA

Input signal requirements

Trigger input signal (terminal $A_1$)

A positive-going voltage step is applied to terminal $A_1$. This voltage step advances the counter one position.




| | | | |
|---|---|---|---|
| Voltage | $V_{AM}$ | = min. | −0.7 $V_N$ |
| | | = max. | − $V_N$ |
| | $-V_0$ | = min. | 0 V |
| | | = max. | 0.2 V |
| Required direct current | $I_{A_1D}$ | = min. | 1.75 mA |
| Required current during the transient averaged over 0.4 μs | $I_{A_1T}$ | = min. | 6 mA |
| over 0.7 μs | | = min. | 4.5 mA |
| Rise time | $t_r$ | = max. | 0.7 μs |
| Pulse duration | $t_1$ | = min. | 1 μs |
| | $t_2$ | = min. | 8 μs |

Reset input signal (terminal $V_1$)

For resetting the counter a positive d.c. voltage is applied to terminal $V_1$. This signal causes all terminals $Q_1$ to reach a "negative high" and all terminals $Q_2$ to reach a "negative low" level.

Input level during reset

| | | | |
|---|---|---|---|
| Voltage | $V_{V_1}$ | = min. | 1 V |
| | | = max. | 10 V |
| Current | $I_{V_1}$ | = min. | 3.6 mA |

During counting it is recommended that terminal $V_1$ is connected to a voltage level.

| | | | |
|---|---|---|---|
| Voltage | $-V_{V_1}$ | = min. | 0.4 V |
| | | = max. | 10 V |
| Current | $-I_{V_1}$ | = min. | 0.12 mA (at $-V_{V_1}$ = 0.4 V) |

D.C. input (terminals W)

A d.c. voltage level is applied to terminals $W_1$ up to and including $W_8$. A positive voltage drives the corresponding transistor into the non-conducting state and a negative voltage drives the transistor into the conducting state.

Transistor conducting

| | | | |
|---|---|---|---|
| Current | $-I_W$ | = min. | 0.6 mA ($-V_W$ = max. 0.4 V) |
| | | = max. | 15 mA |

Transistor non-conducting

| | | | |
|---|---|---|---|
| Voltage | $V_W$ | = min. | 0.2 V |
| | | = max. | 10 V |
| Current | $I_W$ | = min. | 0.9 mA |

OUTPUT DATA

Decade counter section

The outputs of the counter (A, $\overline{A}$, B, $\overline{B}$, etc.) may furthermore be loaded with two gate invertors GI or two negative AND-gates. Output D of the last flip-flop is then still capable to drive a next decade.
A, B, C and D are the outputs of the flip-flops which are at 0 V level, when the decade is set on digit number 0.

Output transistor conducting

Voltage $-V_Q$ = min. 0 V, max. 0.2 V

| | | A | $\overline{A}$ | B | $\overline{B}$ | C | $\overline{C}$ | D | $\overline{D}$ |
|---|---|---|---|---|---|---|---|---|---|
| Available direct current (in mA) | $-I_{QD}$ = | 3.4 | 6 | 2.15 | 3.9 | 3 | 3.9 | 6 | 5.1 |
| Available transient current averaged over 0.7 $\mu$s (in mA) | $-I_{QT}$ = | 9 | 14 | 8.4 | 12.9 | 8.9 | 12.9 | 14 | 14 |

Output transistor non-conducting

Voltage $-V_Q$ = min. 0.7 $V_N$, max. $V_N$

| | | A | $\overline{A}$ | B | $\overline{B}$ | C | $\overline{C}$ | D | $\overline{D}$ |
|---|---|---|---|---|---|---|---|---|---|
| Available direct current (in mA) | $I_{QD}$ = | 0.1 | 0.13 | 0.1 | 0.1 | 0.1 | 0.1 | 0.13 | 0.1 |

Numerical indicator tube driver

The outputs $Q_0$ (terminal 10a) up to and including $Q_9$ (terminal 1a) have to be connected to the pins $k_0$ up to and including $k_9$ of the numerical indicator tube ZM 1000, ZM 1020, ZM 1040 or ZM 1080.
The anode of these tubes has to be connected via a resistor $R_a$ to the high voltage power supply $V_b$.

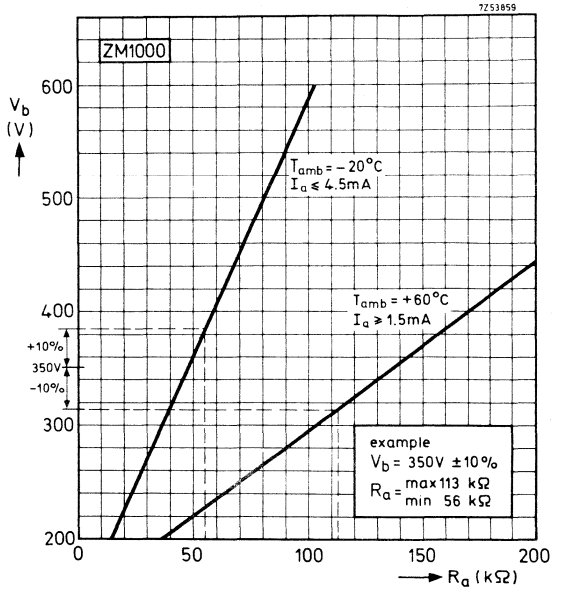
Output transistor conducting

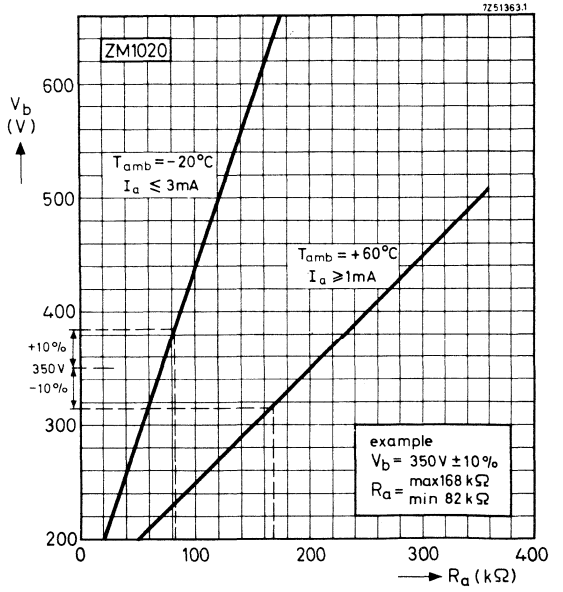
Voltage $V_Q$ = max. 3.2 V

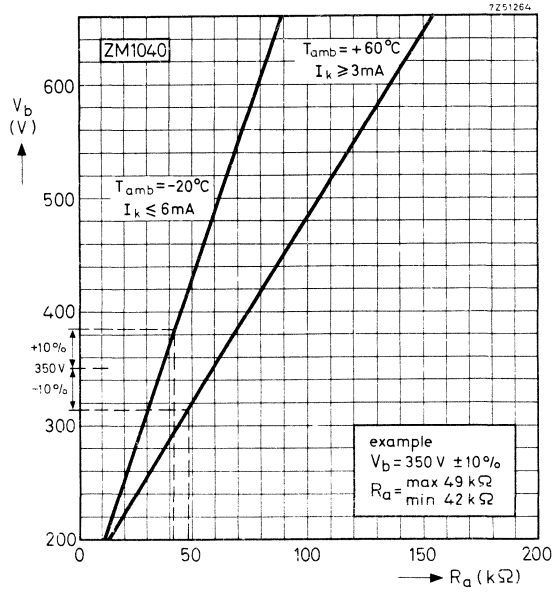
Current $I_Q$ = max. 6 mA

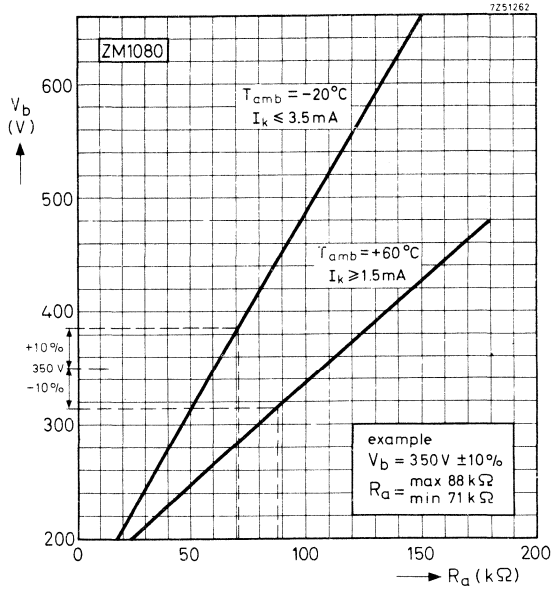
The available output current ($I_Q$) of the ten numerical outputs $Q_0$ up to and including $Q_9$ is sufficient to deliver the required current for the numerical indicator tube ZM 1000, ZM 1020, ZM 1040 or ZM 1080.

The relation between the permitted value and tolerances of the high voltage supply $V_b$ and the corresponding anode series resistor $R_a$ for the various indicator tubes over the whole temperature range is given in the following graphs.


7Z53859
ZM1000
$V_b$ (V)
600
500
400
300
200
+10%
350V
-10%
$T_{amb} = -20°C$
$I_a \leq 4.5mA$
$T_{amb} = +60°C$
$I_a \geq 1.5mA$
example
$V_b$ = 350V ±10%
$R_a$ = max 113 kΩ
min 56 kΩ
0
50
100
150
200
$R_a$ (kΩ)

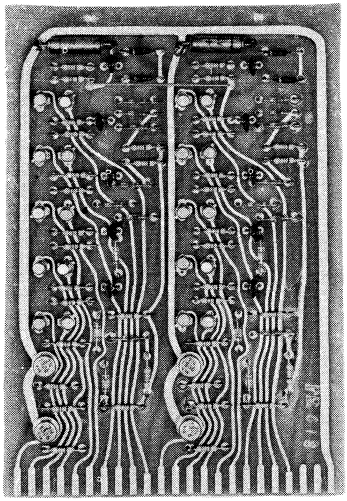

7Z51363.1
ZM1020
$V_b$ (V)
600
500
400
300
200
+10%
350V
-10%
$T_{amb} = -20°C$
$I_a \leq 3mA$
$T_{amb} = +60°C$
$I_a \geq 1mA$
example
$V_b$ = 350V ±10%
$R_a$ = max 168 kΩ
min 82 kΩ
0
100
200
300
400
$R_a$ (kΩ)




Wiring capacitance at each Q-output: max. 500 pF

# DUAL NUMERICAL INDICATOR TUBE DRIVER ASSEMBLY



RZ 22603-8

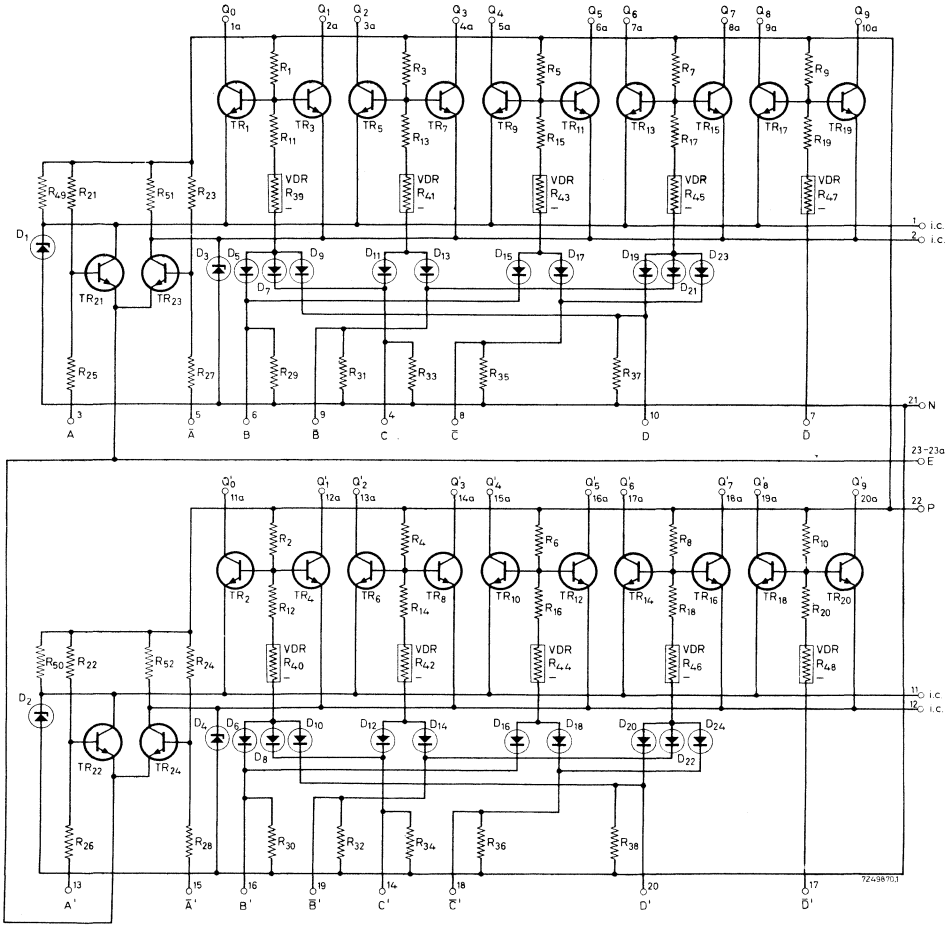
This assembly contains two BCD-to-decimal decoding and driving circuits for the numerical indicator tubes ZM 1000, ZM 1020, ZM 1040 or ZM 1080, mounted on a printed-wiring board.
The 2.ID 1 has been designed to operate in conjunction with decade counters in the 1-2-4-2 (jump at 8) or 1-2-4-8 code, e.g. the dual decade counter assembly 2.DCA 2 (catalog number 2722 009 00011).

The inputs A, $\overline{A}$, B, $\overline{B}$, C, $\overline{C}$, D, $\overline{D}$ and A', $\overline{A'}$, B', $\overline{B'}$, C', $\overline{C'}$, D', $\overline{D'}$ have to be connected to the corresponding outputs of the four flip-flops of the decade counter.
The inputs A, B, C, D and A', B', C', D' have to be at the "0" level for the digit number 0 to be indicated.

The printed-wiring board, provided with plated-through holes and double-sided goldplated contacts, is made of glass-epoxy material. With the mating connector (catalog number 2422 020 52591), not supplied with the 2.ID 1, this printed-wiring board of standard dimensions (121.8 mm x 180.3 mm x 1.6 mm) can be used directly in the standard mounting chassis (catalog number 4322 026 38240).

| | |
|---|---|
| Ambient-temperature range: | −20 to +60 °C |
| Weight | approx. 100 g |

CIRCUIT DATA




Terminals

1 = internal connection
2 = internal connection
3 = A = to be connected to output Q of first flip-flop
4 = C = to be connected to output Q of third flip-flop
5 = $\overline{A}$ = to be connected to output $\overline{Q}$ of first flip-flop
6 = B = to be connected to output Q of second flip-flop
7 = $\overline{D}$ = to be connected to output $\overline{Q}$ of fourth flip-flop
8 = $\overline{C}$ = to be connected to output $\overline{Q}$ of third flip flop
9 = $\overline{B}$ = to be connected to output $\overline{Q}$ of second flip-flop
10 = D = to be connected to output Q of fourth flip-flop

} decade counter 1

11 = internal connection
12 = internal connection
13 = A' = to be connected to output Q of first flip-flop
14 = C' = to be connected to output Q of third flip-flop
15 = $\overline{A'}$ = to be connected to output $\overline{Q}$ of first flip-flop
16 = B' = to be connected to output Q of second flip-flop
17 = $\overline{D'}$ = to be connected to output $\overline{Q}$ of fourth flip-flop
18 = $\overline{C'}$ = to be connected to output $\overline{Q}$ of third flip-flop
19 = $\overline{B'}$ = to be connected to output $\overline{Q}$ of second flip-flop
20 = D' = to be connected to output Q of fourth flip-flop
} decade counter 2
21 = N = common negative supply −6 V
22 = P = common positive supply +6 V
23 = 23a = E = common supply 0 V

1a up to and including 10a = numerical outputs $Q_0$ up to and including $Q_9$ to drive numerical indicator tube 1

11a up to and including 20a = numerical outputs $Q'_0$ up to and including $Q'_9$ to drive numerical indicator tube 2

Power supply

Terminal 21 : $V_N$ = −6 V ± 5%, $-I_N$ = 8.5 mA
22 : $V_P$ = +6 V ± 5%, $I_P$ = 7 mA
} nominal value of the current required for one ID 1
23 : $V_E$ = 0 V common

Notes

- The data given apply to the most adverse supply voltages for a combination of units, namely: $V_N$ = −5.7 V and $V_P$ = +6.3 V
- The temperatures −20 °C and +60 °C and the tolerances on the supply voltages are absolute limiting values.
- When a current is flowing towards the unit, the positive sign is used.

INPUT DATA

Input signal requirements (terminals A, $\overline{A}$, A', $\overline{A'}$, etc.)

Input at "0" level

Voltage $-V_I$ = min. 0 V
= max. 0.2 V

| | | A, A', $\overline{A}$, $\overline{A'}$ | B, B', $\overline{B}$, $\overline{B'}$, C, C', $\overline{C}$, $\overline{C'}$, D, D' | $\overline{D}$, $\overline{D'}$ |
|---|---|---|---|---|
| Required direct current | $I_I$ | 0 mA | 2.1 mA | 0 mA |
| Required transient current | $I_{QT}$ | 0 mA | 1.1 mA | 0 mA |

Input at negative high level

Voltage $-V_I$ = min. 0.7 $V_N$
= max. $V_N$

| | A, A', $\overline{A}$, $\overline{A'}$ | B, B', $\overline{B}$, $\overline{B'}$, C, C', $\overline{C}$, $\overline{C'}$, D, D' $\overline{D}$, $\overline{D'}$ |
|---|---|---|
| Required direct current $-I_I$ | 0.57 mA | 0.6 mA |

Input impedance equivalent to a capacitance of approx. 150 pF

Operational data

- When an ID 1 is driven from a decade counter with flip-flops operating in the 1-2-4-8 code, these flip-flops may be additionally loaded with two negative AND-gates, or with two GI's if the decade counter is equipped with FF 3 flip-flops, or with one GI if the decade counter is equipped with FF 1 flip-flops. Output D of the last flip-flop is capable of driving a following decade counter.
- A, B, C, D and A', B', C', D' must be connected to the outputs of the flip-flops which are at "0" level, when the decade counter is set on digit number 0.

OUTPUT DATA

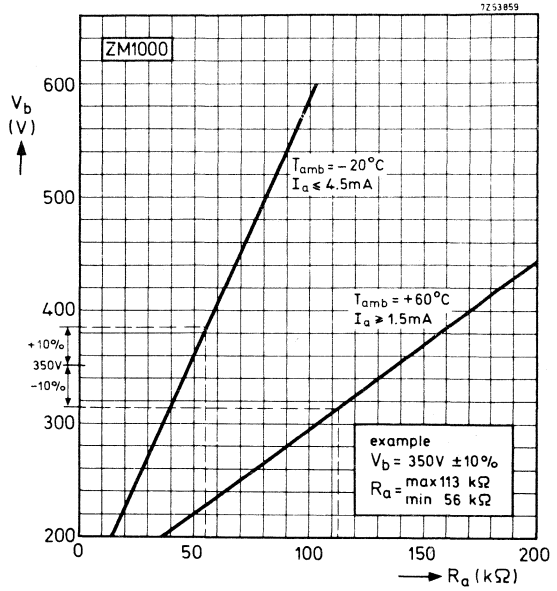
The outputs $Q_0$ up to and including $Q_9$ and $Q'_0$ up to and including $Q'_9$ have to be connected to the pins $k_0$ up to and including $k_9$ of the numerical indicator tube ZM 1000, ZM 1020, ZM 1040 or ZM 1080.
The anode of these tubes has to be connected via a resistor $R_a$ to the high voltage power supply $V_b$.

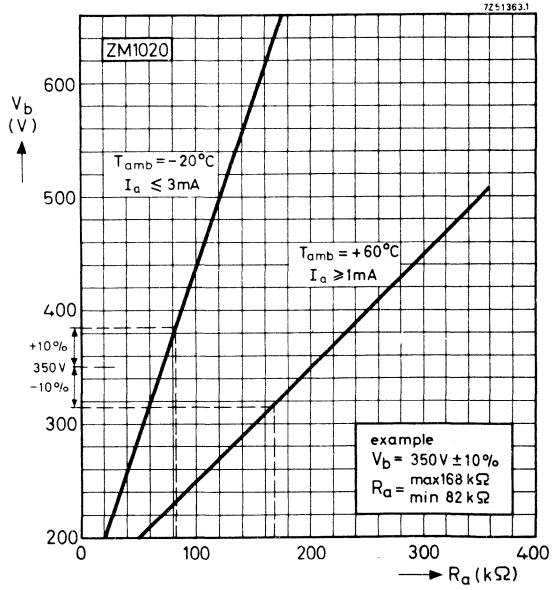
Output transistor conducting

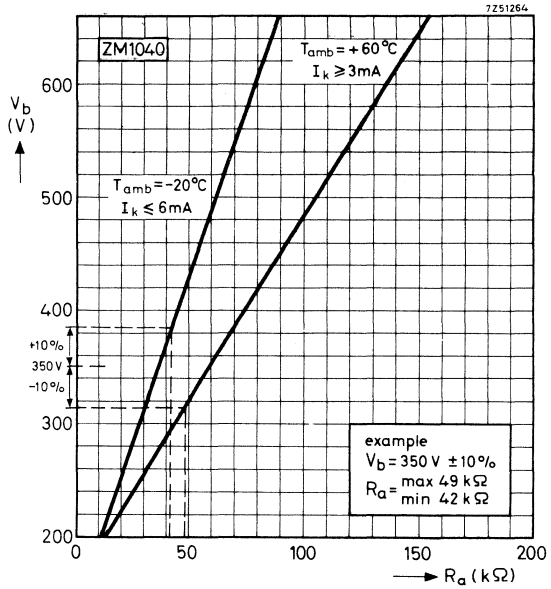
Voltage $V_Q$ = max. 3.2 V

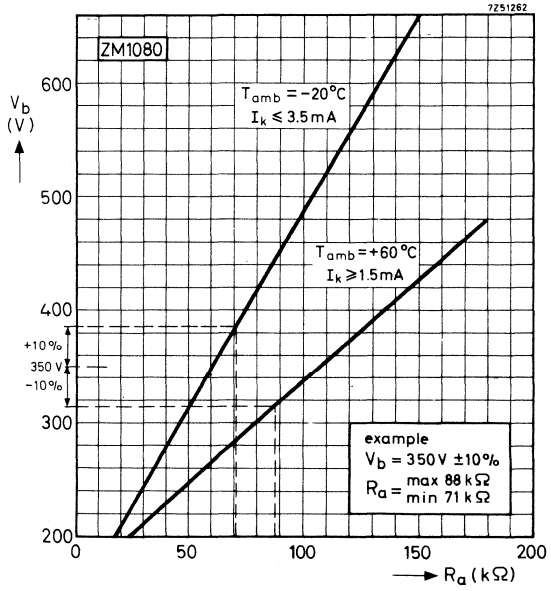
Current $I_Q$ = max. 6 mA

The available output current ($I_Q$) of the ten numerical outputs $Q_0$ (terminal 1a and 11a) up to and including $Q_9$ (terminal 10a and 20a) is sufficient to deliver the required current for the numerical indicator tube ZM 1000, ZM 1020, ZM 1040 or ZM 1080.
The relation between the permitted value and tolerances of the high voltage supply $V_b$ and the corresponding anode series resistor $R_a$ for the various indicator tubes over the whole temperature range is given in the following graphs.


7Z53859
ZM1000
$V_b$ (V)
600
500
400
300
200
+10%
350V
-10%
$T_{amb}$ = -20°C
$I_a \leq$ 4.5mA
$T_{amb}$ = +60°C
$I_a \geq$ 1.5mA
example
$V_b$ = 350V ±10%
$R_a$ = max 113 kΩ
min 56 kΩ
0
50
100
150
200
$R_a$ (kΩ)


7Z51363.1
ZM1020
$V_b$ (V)
600
500
400
300
200
+10%
350V
-10%
$T_{amb}$ = -20°C
$I_a \leq$ 3mA
$T_{amb}$ = +60°C
$I_a \geq$ 1mA
example
$V_b$ = 350V ±10%
$R_a$ = max 168 kΩ
min 82 kΩ
0
100
200
300
400
$R_a$ (kΩ)



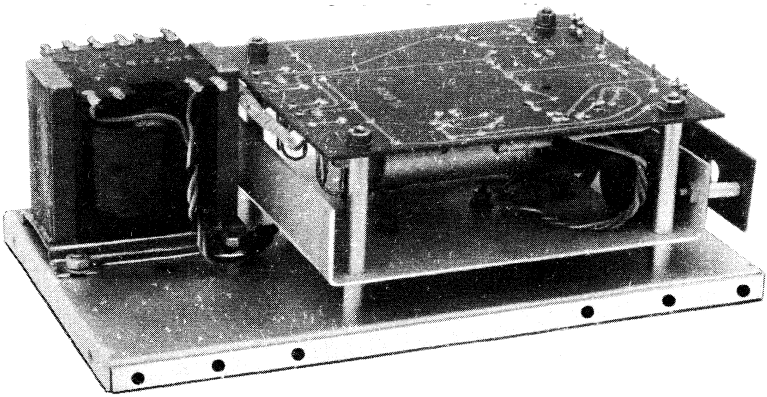




Wiring capacitance at each Q-output: max. 500 pF

# ACCESSORIES FOR CIRCUIT BLOCKS

## 1– SERIES

# POWER SUPPLY UNIT



15945/4

| | |
|---|---|
| Input voltage | 220 $V_{ac}$ and 235 $V_{ac}$ |
| Output voltage | +6 $V_{dc}$ and −6 $V_{dc}$ |

APPLICATION

This power supply unit has been designed for use with the circuit blocks of the 100 kHz- and the 1-series. However, it is also suitable as a supply for other transistorised circuits.

CONSTRUCTION

The unit is dimensioned for mounting in the standardized 19" chassis. The power supply unit fits in chassis 4322 026 38240; the base plate of the unit then replaces a side plate of the chassis. The supply unit occupies the same space as four printed-wiring boards.

| | |
|---|---|
| Dimensions | 215 x 125 x 70 mm |
| Weight | 1.5 kg |

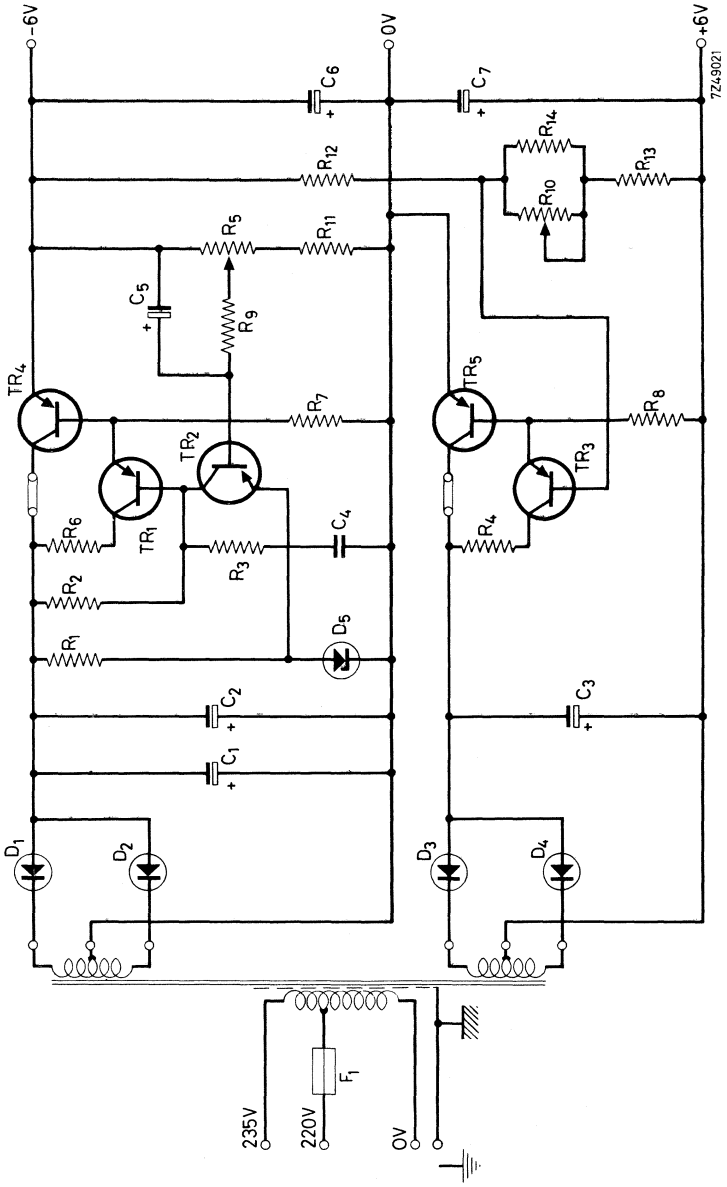
TECHNICAL PERFORMANCE

| | | |
|---|---|---|
| Input voltage | 220 $V_{ac}$ +10 %, −15 % | |
| | 235 $V_{ac}$ +10 %, −15 % | |
| Frequency | 50 to 60 | Hz |
| Fusing | 1 A fuse in the 220 V winding only | |
| −6 V output [1] | | |
| Output voltage | 6 V, adjustable ±3 % (R5, see diagram) | |
| Output current | 600 | mA |
| Stability ratio at 220 V | 450:1 | |
| Ripple voltage | 50 | $mV_{rms}$ |
| Output resistance | 0.3 | Ω |
| Output impedance at 10 kHz | 0.2 | Ω |
| Temperature coefficient | −3 | mV/deg C |
| +6 V output [1] | | |
| Output voltage | 6 V, adjustable ±3 % (R10, see diagram) | |
| Output current | 150 | mA |
| Stability ratio at 220 V | 360:1 | |
| Ripple voltage | 50 | $mV_{rms}$ |
| Output resistance | 1.5 | Ω |
| Output impedance at 10 kHz | 0.5 | Ω |
| Temperature coefficient | +6 | mV/deg C |
| Operating-temperature range | −20 to +60 | °C |
| Storage-temperature range | −20 to +75 | °C |

In systems requiring more than one power supply unit, the earth tags (marked "0 V") may be interconnected, the positive tags (marked "+6 V") and the negative tags (marked "−6 V") must remain strictly separated.

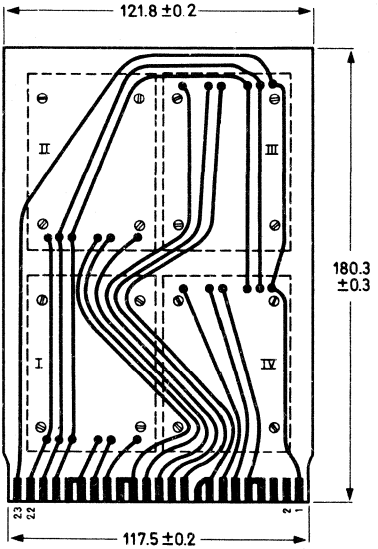
When a system is put into operation for the first time, the output voltages of the power supply units have to be adjusted to 6 V under nominal system load.

1) All values are given for full load.


-6V
0V
+6V
7249021
C6
C7
R14
R12
R10
R13
R5
R11
C5
R9
TR4
TR5
R7
R8
TR2
TR3
TR1
C4
R6
R3
R4
R2
D5
R1
C2
C3
C1
D1
D2
D3
D4
F1
235V
220V
0V

# PRINTED-WIRING BOARD FOR FOUR UNITS PA 1

This printed-wiring board fits the mounting chassis 4322 026 38240. It can be used directly with the aid of the mating connector 2422 020 52592. On this board up to four PA 1's can be mounted, the next position in the chassis being left empty.




Terminal location:

1 = E = common supply 0 V (interconnected to terminal 1)

2 = not connected

3 = not connected

4 = $N_2$, 5 = $N_2$ } supply max. 60 V

6 = Q = output PA 1

7 = W = input PA 1

} unit nr. IV

8 = $N_2$, 9 = $N_2$ } supply max. 60 V

10 = Q = output PA 1

11 = W = input PA 1

} unit nr. III

12 = W = input PA 1

13 = Q = output PA 1

14 = $N_2$, 15 = $N_2$ } supply max. 60 V

} unit nr. II

16 = W = input PA 1

17 = Q = output PA 1

18 = $N_2$, 19 = $N_2$ } supply max. 60 V

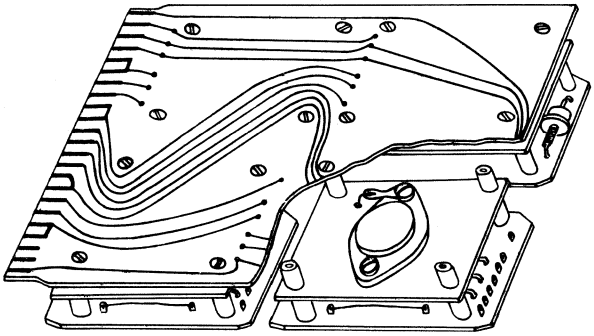
} unit nr. I

20 = $N_1$ = common supply −6 V

21 = P = common supply +6 V

22 = E = common supply 0 V

23 = E = common supply 0 V




| | |
|---|---|
| Material | glass epoxy with plated-through holes |
| Hole diameter | 1.2 mm |
| Contacts | 1 x 23, gold plated, pitch 0.2 inch |

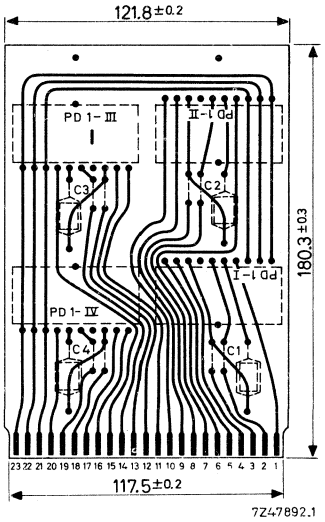
# PRINTED-WIRING BOARD FOR FOUR UNITS PD 1

This printed-wiring board with standard dimensions 121.8 mm x 180.3 mm x 1.6 mm (4.8" x 7.1" x 0.0625") is intended to accomplish the mounting of maximum four pulse driver units PD 1 (catalog number 2722 001 13011).

One printed-wiring board PDA 1 with four units PD 1 mounted on it, can be used in conjunction with three reversible counters BCA 1 (catalog number 2722 009 00021).
Two units PD 1 perform shift-pulse amplifying functions between two reversible counters BCA 1, one for the forward and one for the reverse direction.

The printed-wiring board is provided with two wire jumpers for each PD 1. In case the number of trigger- and gate-inputs has to be extended, these wire jumpers can be replaced by diodes, type OA 95. The required connections with the EG- and K-terminals of the PD 1 have already been made in the print pattern.
Furthermore the printed-wiring board is provided with two plated-through holes for each unit PD 1. In case the output-pulse duration of the PD 1 has to be increased, these holes can be used for mounting the required capacitor. The terminals of this capacitor are then directly connected to the K- and L-terminals of the concerning PD 1.

Holes are provided to secure the PD 1 rigidly to the board by means of the locking tag 4322 026 33690.
With the mating connector 2422 020 52592 the printed-wiring board can be used directly in the mounting chassis 4322 026 38240.




Terminal location:

1 = $Q_1$ = output PD 1-I
2 = $EG_1$ = extension gate input PD 1-I
3 = $K_1$ = extension trigger input PD 1-I
4 = $G_1$ = gate input PD 1-I
5 = $A_1$ = trigger input PD 1-I
6 = $Q_2$ = output PD 1-II
7 = $EG_2$ = extension gate input PD 1-II
8 = $K_2$ = extension trigger input PD 1-II
9 = $G_2$ = gate input PD 1-II
10 = $A_2$ = trigger input PD 1-II
11 = $A_3$ = trigger input PD 1-III
12 = $G_3$ = gate input PD 1-III
13 = $K_3$ = extension trigger input PD 1-III
14 = $EG_3$ = extension gate input PD 1-III
15 = $Q_3$ = output PD 1-III
16 = $A_4$ = trigger input PD 1-IV
17 = $G_4$ = gate input PD 1-IV
18 = $K_4$ = extension trigger input PD 1-IV
19 = $EG_4$ = extension gate input PD 1-IV
20 = $Q_4$ = output PD 1-IV
21 = N = common supply −6 V
22 = P = common supply +6 V
23 = E = common supply 0 V

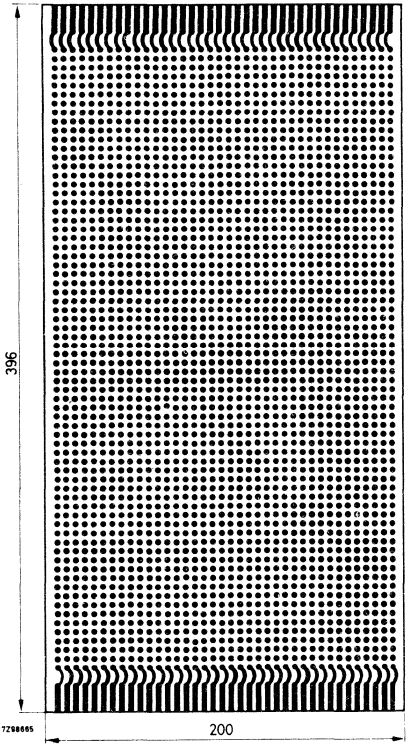
| | |
|---|---|
| Material | glass epoxy with plated-through holes |
| Hole diameter | 1.2 mm |
| Contacts | 1 x 23, gold plated, pitch 0.2 inch |

INPUT AND OUTPUT DATA

See specification of pulse driver unit PD 1 (catalog number 2722 001 13011)

# EXPERIMENTERS' PRINTED–WIRING BOARDS

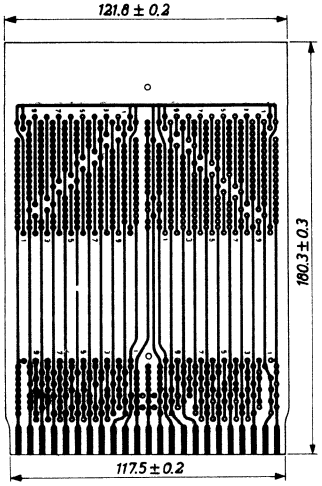
These experimenters' printed-wiring boards are very suitable for circuit blocks of the 100 kHz- and 1-Series.




| | | |
|---|---|---|
| Material | copper-clad phenolic resin bonded paper | |
| Grid pitch | 5.08 mm (0.2 inch) | |
| Contacts | gold plated, pitch 0.2 inch | |
| | single sided<br>2 x 38 | double sided<br>4 x 38 |
| Holes | with holes | – |
| Catalogue number | 4322 026 34900 | 4322 026 34910 |

# PRINTED-WIRING BOARD

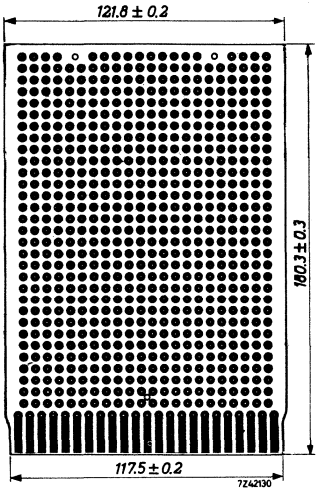
This printed-wiring board is intended for mounting circuit blocks of the 100 kHz- and 1-Series.
It fits the mounting chassis 4322 026 38240.




| | |
|---|---|
| Material | copper-clad phenolic resin bonded paper with punched holes |
| Hole diameter | 1.3 mm |
| Contacts | 1 x 23, gold plated, pitch 0.2 inch |

# EXPERIMENTERS' PRINTED—WIRING BOARD

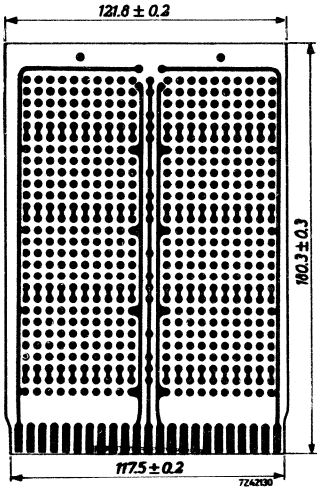
This experimenters' printed-wiring board is very suitable for circuit blocks of the 100 kHz- and 1-Series.
It fits the mounting chassis 4322 026 38240.




| | |
|---|---|
| Material | copper-clad phenolic resin bonded paper with punched holes |
| Grid pitch | 5.08 mm (0.2 inch) |
| Hole diameter | 1.3 mm |
| Contacts | 1 x 23, gold plated, pitch 0.2 inch |

# PRINTED—WIRING BOARD

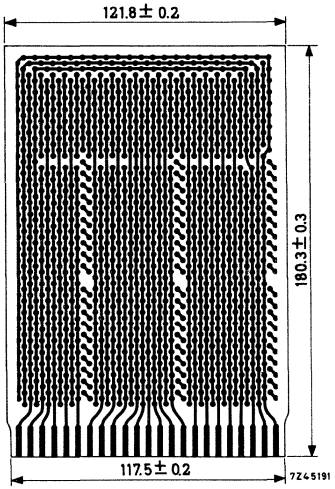
This printed-wiring board for 100 kHz- and 1-Series circuit blocks can accommodate 8 horizontally mounted blocks. Combination of circuit blocks with discrete components is easily possible on this board.
It fits the mounting chassis 4322 026 38240.




| | |
|---|---|
| Material | copper-clad phenolic resin bonded paper with plated-through holes |
| Hole diameter | 1.2 mm |
| Contacts | 1 x 23, gold plated, pitch 0.2 inch |

# PRINTED-WIRING BOARD

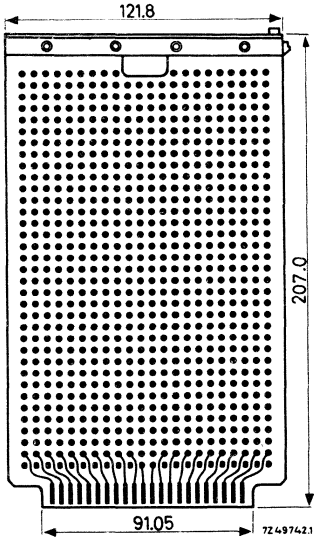
This printed-wiring board is intended for mounting circuit blocks of the 100 kHz- and 1-Series. It fits the mounting chassis 4322 026 38240.




| | |
|---|---|
| Material | copper-clad phenolic resin bonded paper with plated-through holes |
| Hole diameter | 1.2 mm |
| Contacts | 1 x 23, gold plated, pitch 0.2 inch |

# EXPERIMENTERS' PRINTED—WIRING BOARD

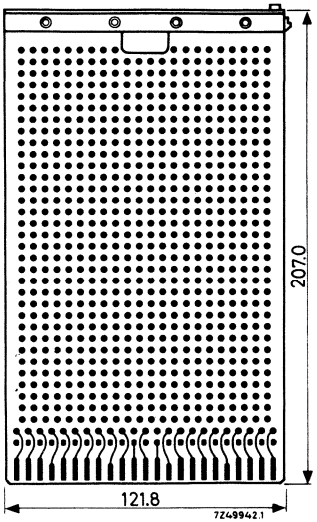
This experimenters' printed-wiring board (with extractor) is very suitable for circuit blocks of the 100 kHz- and 1-Series.
It fits the mounting chassis 4322 026 38230.




| | |
|---|---|
| Material | phenolic resin bonded paper with holes; on both sides are copper lands around each hole |
| Grid pitch | 5.08 mm (0.2 inch) |
| Hole diameter | 1.3 mm |
| Contacts | 2 x 22, gold plated, pitch 0.156 inch |

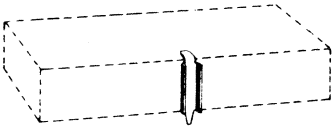
# EXPERIMENTERS' PRINTED-WIRING BOARDS

These experimenters' printed-wiring boards (with extractor) are very suitable for circuit blocks of the 100 kHz- and 1-Series.
They fit the mounting chassis 4322 026 38240.




| | | |
|---|---|---|
| Catalogue number | 4322 026 38630 | 4322 026 38690 |
| Material | phenolic resin bonded paper | glass epoxy |
| Grid pitch | 5.08 mm (0.2 inch) | |
| Holes | diameter 1.3 mm; on both sides of the board are copper lands around each hole | |
| Contacts | 2 x 23, gold plated, pitch 0.2 inch | |

# LOCKING TAG



Circuit blocks of the 100 kHz- and 1-Series mounted parallel to the printed-wiring board can be secured rigidly by means of this small tag, which permits soldering in a standard 1.3 mm diameter hole. The minimum supply quantity is 1000 pieces.

# STICKERS

These are drawing symbols of circuit blocks printed on self-adhesive, transparent material. They can be used for fast preparation of system drawings. The drawing symbols are as shown on the data sheets of the relevant circuit blocks.
The stickers are available in rolls, each containing 1000 drawing symbols of the same type of circuit block. Each sticker can be separately detached from the roll, without cutting.

| for circuit block of type | catalog number of a roll with 1000 stickers |
|---|---|
| FF 1 | 4322 026 35780 |
| FF 2 | 4322 026 35790 |
| FF 3 | 4322 026 35800 |
| FF 4 | 4322 026 35810 |
| 2.3.N 1 | 4322 026 35820 |
| 2.2.N 1 | 4322 026 35830 |
| 2.3.P 1 | 4322 026 35840 |
| 2.2.P 1 | 4322 026 35850 |
| 2.PL 1 | 4322 026 35860 |
| 2.PL 2 | 4322 026 35880 |
| EF 1/IA 1 | 4322 026 35890 |
| 2.EF 1 | 4322 026 35900 |
| 2.IA 1 | 4322 026 35910 |
| 2.EF 2 | 4322 026 35920 |
| 2.IA 2 | 4322 026 35930 |
| 2.GI 1 | 4322 026 34620 |
| PS 1 | 4322 026 35950 |
| PS 2 | 4322 026 36820 |
| PR 1 | 4322 026 36830 |
| OS 1 | 4322 026 35960 |
| OS 2 | 4322 026 35980 |
| PD 1 | 4322 026 30710 |
| PA 1 | 4322 026 07760 |

# Circuit blocks
# for
# ferrite core memory drive

# INTRODUCTION

In the development and manufacture of magnetic core memories it is essential to have a profound knowledge of the specific characteristics and requirements that are imposed on the core drive circuits.
These circuits should perform their functions with accuracy, efficiency and reliability and this can be met by a proper design and care in manufacture. The different properties of the various cores as well as their responses, dependent on the number of cores per matrix plane and the number of planes per stack, make great demands on those responsible for the design of the complete system and in particular the development of the basic circuits.

The core drive units in this series have been designed especially for properly performing the specific functions in magnetic core memories, such as the sense amplifier, the selection switch, the selection gate and the pulse generator. They should be used in conjunction with 100 kHz-series circuit blocks.

The following four circuit blocks for driving and reading core memories are available:

| description | abbreviation | catalog number | page |
|---|---|---|---|
| dual selection switch | 2.SS1 | 2722 001 14001 | C5 |
| selection gate | SG1 | 2722 001 04001 | C9 |
| pulse generator | PG1 | 2722 001 12001 | C11 |
| read amplifier | RA2A<br>RA2B | 2722 001 09011<br>2722 001 09021 | C15 |

These circuit blocks have been developed as a part of the complete range of standard 100 kHz circuit blocks. For this reason reference is made to the section "Circuit Blocks 100 kHz Series" for CONSTRUCTION and TEST SPECIFICATION.

# DUAL SELECTION SWITCH

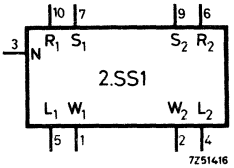
Colour: blue

The unit 2.SS1 contains two identical circuits designed to operate as current switches in series with the drive wires of a ferrite-core memory.

The switching of the n-p-n output transistor is controlled by a d.c. input level applied to a built-in pre-amplifier stage.

Frequency range : 0 - 100 kHz
Ambient temperature range:
operating 0 to 60 °C
storage -25 to 75 °C
Weight : approx. 20 g

drawing symbol




CIRCUIT DATA

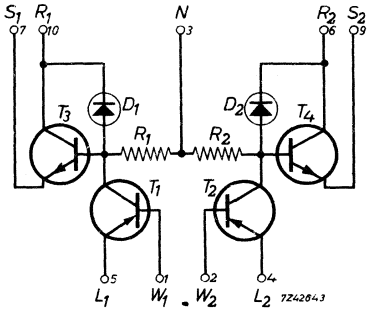



Fig 1

Terminal 1 = $W_1$ = control input 1
2 = $W_2$ = control input 2
3 = N = supply -6V
4 = $L_2$ = current supply T2
5 = $L_1$ = current supply T1
6 = $R_2$ = switch 2 in
7 = $S_1$ = switch 1 out
8 = = not connected
9 = $S_2$ = switch 2 out
10 = $R_1$ = switch 1 in

Power supply

Terminal 3 : $V_N = -6V \pm 2\%$, $-I_N = 8mA$ (nominal value)

Terminals 4 and 5 via a current stabilisation circuit (either resistor or transistor) to $V_P$.

$V_P = +6V \pm 2\%$, $I_P$ = max 25 mA each terminal

Terminals 6 and 10 : $I_{RS}$ see output data

## APPLICATION DATA

The unit is normally used in combination with other standard circuit blocks for ferrite-core memory operation.

Control input (W-terminals)

The W terminals are directly connected to the output terminals of the driving selection gate SG1.

Line input (L-terminals)*

The L terminals are connected to a current source which can be common to all selection switches operating at the same side of the core matrix (Fig 2).

For the selection switches operating at the negative supply voltage side of the matrix (terminals 5 of both units 2.SS1 in Fig 2):

Required current $I_L$ = approx. 15 mA (16 mA)**

Note - Usually a $620\Omega \pm 5\%$ ($510\Omega \pm 5\%$)** resistor is used between the inter-connected L terminals and the +6V supply.

For the selection switches operating at the positive supply voltage side of the matrix (terminals 4 of both units 2.SS1 in Fig 2):

Required current $I_L$ = approx. 23 mA (25 mA)**

Notes - Usually a grounded base transistor (e.g. type ASY 80) with a collector resistor of $47\Omega \pm 5\%$ and an emitter resistor of approx. $270\Omega \pm 5\%$ ($220\Omega \pm 5\%$)** is used between the inter-connected L terminals and the +6V supply.

* $I_L = 0mA$ $T_1$ and $T_2$ non-conducting
$I_L = 16mA$ $T_1$ conducting
$I_L = 25mA$ $T_2$ conducting
$I_L = 41mA$ $T_1$ and $T_2$ conducting

** The values between brackets are given with respect to a switch current of 310 mA.

- For memories in which the group selection principle is applied a voltage of max. 2 V can be tolerated across the drive wire during the switching-on of the drive current.

Output (R- and S-terminals)

The output terminals are connected in series with a group of drive wires.

Selection switch conducting

Current $I_{RS}$ = max. 250 mA (310 mA) **

Voltage $V_{RS}$ = max. 0.8 V peak

Selection switch non-conducting

Current $I_{RS}$ = max. 0.1 mA

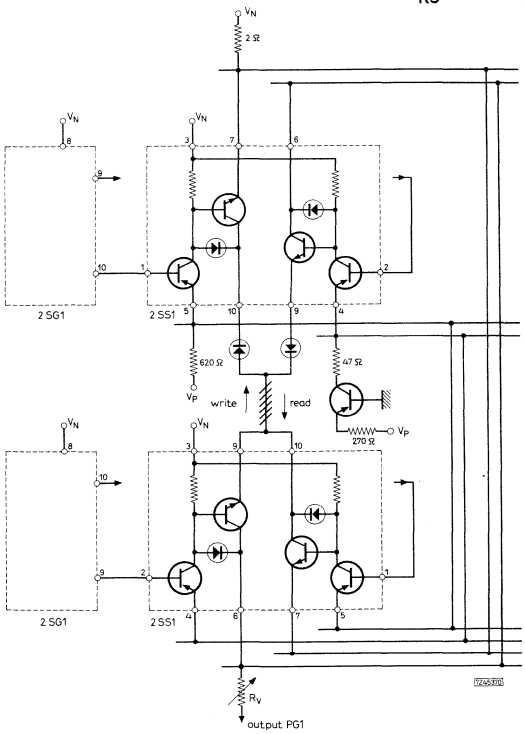



Fig.2

Notes
- When a current is flowing towards the unit, the positive sign is used.
- Unless differently specified, all voltage and current figures quoted represent absolute limiting values.

** The values between brackets are given with respect to a switch current of 310 mA.

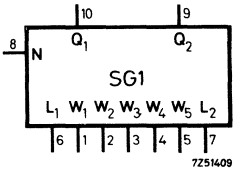
# SELECTION GATE

Colour: orange

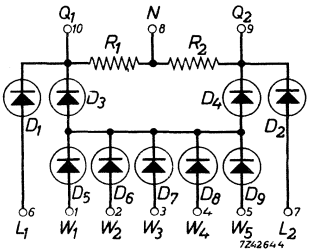
The unit SG1 is designed to perform a two-level AND operation between address register and selection switches in ferrite-core memories.
The W input AND gate which decodes the selection register information, is followed by a twin two-input AND gate to perform the Read/Write control function.

Frequency range : 0 - 100 kHz
Ambient temperature range:
operating 0 to +60 °C
storage -25 to +75 °C
Weight : approx. 20 g

drawing symbol




CIRCUIT DATA




Terminal 1 = $W_1$ = address - selection input 1
2 = $W_2$ = address - selection input 2
3 = $W_3$ = address - selection input 3
4 = $W_4$ = address - selection input 4
5 = $W_5$ = address - selection input 5
6 = $L_1$ = Read/Write control input 1
7 = $L_2$ = Read/Write control input 2
8 = N = supply -6 V
9 = $Q_2$ = output 2
10 = $Q_1$ = output 1

Power supply

Terminal 8 : $V_N = -6V \pm 2\%$, $-I_N = 2mA$ (nominal value)

APPLICATION DATA

The unit is normally used in combination with the dual selection switch 2.SS 1 and other circuit blocks for ferrite-core memory operation.

Selection input (W-terminals)

The W terminals are connected to the flip-flops in the address selection register. Depending on the size of the memory, this connection is done directly or via adequate amplifier stages.

| | |
|---|---|
| Voltage | $-V_W$ = max 0.2V |
| Required current | $I_W$ = min 1 mA at $V_W = 0V$ |

Read/Write control input (L-terminals)

The $L_1$ and $L_2$ terminals are connected to opposite voltage levels, normally derived from a Read/Write control flip-flop. Depending on the memory capacity, the interconnected $L_1$ respectively $L_2$ terminals are driven directly or via a 2.IA1 - 2.IA2 amplifier chain.

| | |
|---|---|
| Voltage | $-V_L$ = max 0.2 V |
| Required current | $I_L$ = min 1 mA at $V_L = 0V$ |

Output (Q-terminals)

The Q terminals are directly connected to the W terminals of the driven dual selection switch (2.SS1).

Notes
- When a current is flowing towards the unit, the positive sign is used.
- Unless differently specified, all voltage and current figures quoted represent absolute limiting values.

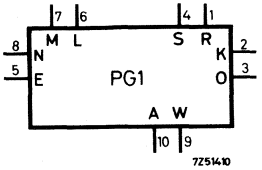
# PULSE GENERATOR

Colour: green

The unit PG 1 has been designed to operate as a drive current switch for the drive (X and Y) wires and the inhibit (Z) wires of a ferrite-core memory.

The switching of the n-p-n output transistor is controlled by an input level change applied to a built-in pre-amplifier stage.

| | | |
|---|---|---|
| Frequency range | : | 0 - 100 kHz |
| Ambient temperature range: | | |
| operating | | - 20 to + 60 °C |
| storage | | - 25 to + 75 °C |
| Weight | : | approximately 20 g |




drawing symbol

CIRCUIT DATA

Terminal 1 = R = drive current input
2 = K = to be connected to terminal 4*
3 = O = to be connected to terminal 4*
4 = S = drive current output
5 = E = common supply 0 V
6 = L = terminal for external capacitor
7 = M = supply - 6 V*
8 = N = supply - 6 V*
9 = W = d.c. input
10 = A = trigger input

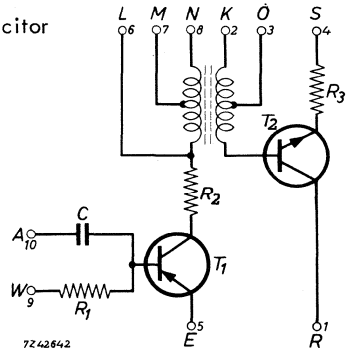



Fig 1 7Z42642

* Depending on the application, see Fig 4 and table "Switching and delay times".

Power supply

Terminal 5: $V_E$ = 0V common
7 or 8: $V_N$ = -6V ± 2%, $-I_N$ = 50mA (nominal value)

Terminal 3 and 4 or 2 and 4: see Fig 3a or b, $-I_S$ } see output data PG 1
Terminal 1 : see Fig 3a or b, $I_R$ }

APPLICATION DATA

The unit is normally used in combination with other standard circuit blocks, for ferrite-core memory operation.

Input circuit PG 1

The PG 1 is normally triggered by the Q-output of an IA 1 or IA 2 inverter amplifier by connecting this output to input terminal A. For proper functioning a diode must be connected between the terminals A and W (cathode to terminal A), see Fig 2. A positive going input signal applied to the PG 1, switches the output transistor into the conducting state.

Driving requirements of the PG 1

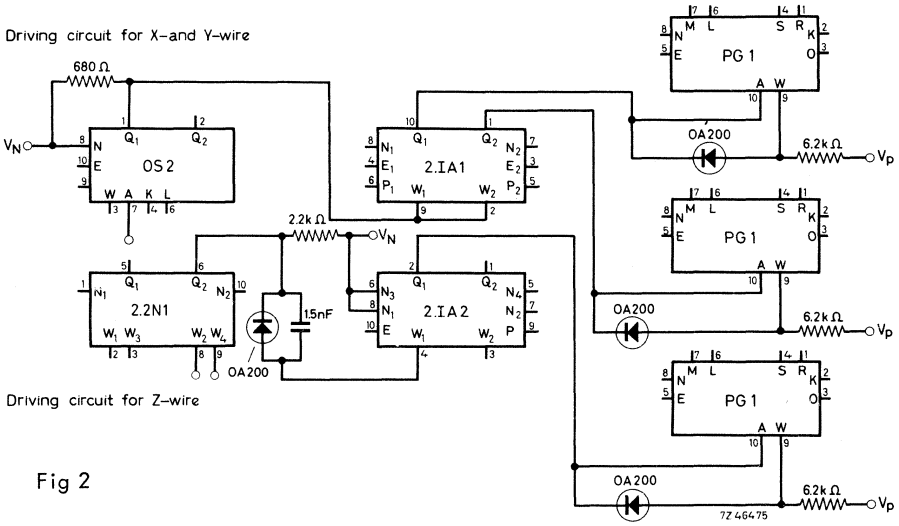



Fig 2

Output data PG 1

The output terminals R and S are connected in series with a group of X and Y wires or a Z wire.

Pulse generator conducting

| | temperature | - 20 °C | 0 °C | 60 °C |
|---|---|---|---|---|
| Current | $I_{RS}$ max | 250 mA | 310 mA | 250 mA |
| Voltage | $V_{RS}$ max | 1.5 $V_{peak}$ | 1.7 $V_{peak}$ | 1.5 $V_{peak}$ |

For temperatures between - 20 °and + 60 ° the maximum values for $I_{RS}$ can be found by linear interpolation.

Pulse generator non-conducting

Current $I_{RS}$ = max 2.5 mA
at $V_{RS}$ = max 15 $V_{peak}$

To adapt the current $I_{RS}$ to the drive current requirements of the X, Y and Z wires an external resistor has to be inserted in the circuit in series with the above mentioned wires. Two alternative circuits are given below.

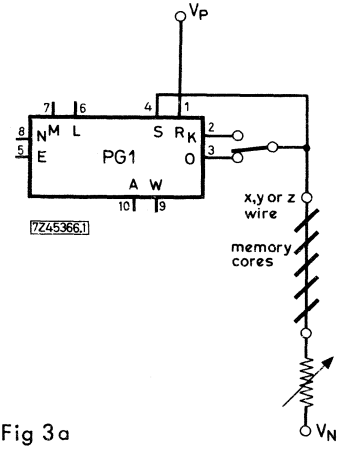



Fig 3a

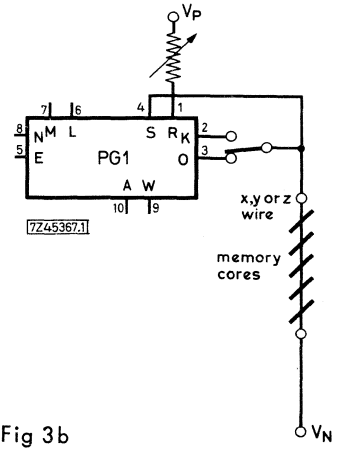



Fig 3b

Switching and delay times (for orientation only)

The duration of the output pulse depends on the duration of the input pulse. When short output pulses are required $V_N$ has to be connected to the terminals 3, 4 and 7 (Fig. 4a) and for wider output pulses to 2, 4 and 8 (Fig. 4b).

The switching and delay times given below, apply for the driving circuits shown in Fig. 4a and 4b.

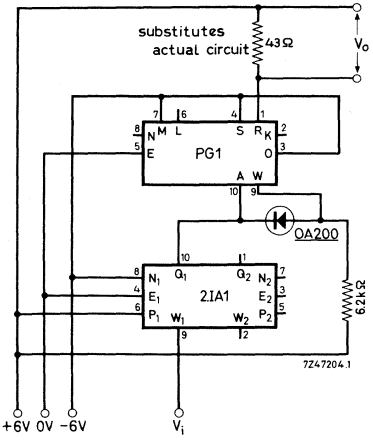
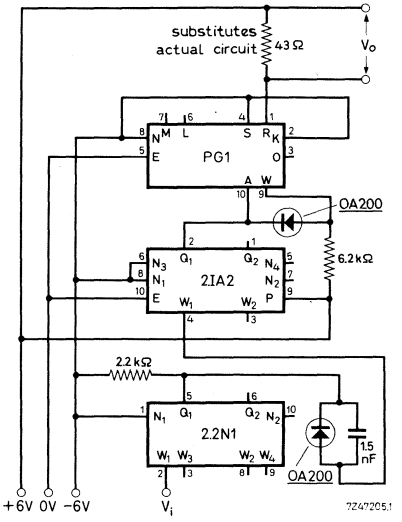
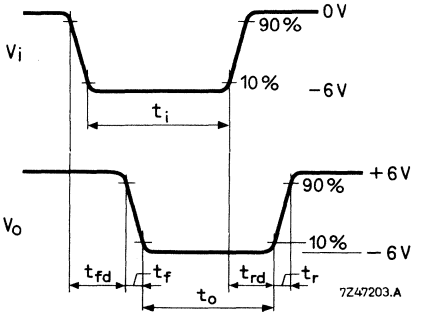



Fig. 4a DRIVING CIRCUIT FOR X-AND Y WIRE




DRIVING CIRCUIT FOR Z-WIRE Fig. 4b

| | | Fig. 4a | Fig. 4b | |
|---|---|---|---|---|
| Input pulse duration | $t_i$ | 2 | 4 | µs |
| Repetition frequency | $f_i$ | 100 | 50 | kHz |
| Fall delay | $t_{fd}$ = max | 0.2 | 0.2 | µs |
| Fall time | $t_f$ = max | 0.1 | 0.1 | µs |
| Output pulse duration | $t_o$ = min | -- | -- | |
| Rise delay | $t_{rd}$ = max | 1 | 1 | µs |
| Rise time | $t_r$ = max | 0.1 | 0.1 | µs |




Notes
- When a current is flowing towards the unit, the positive sign is used.
- Unless differently specified, all voltage and current figures quoted represent absolute limiting values.

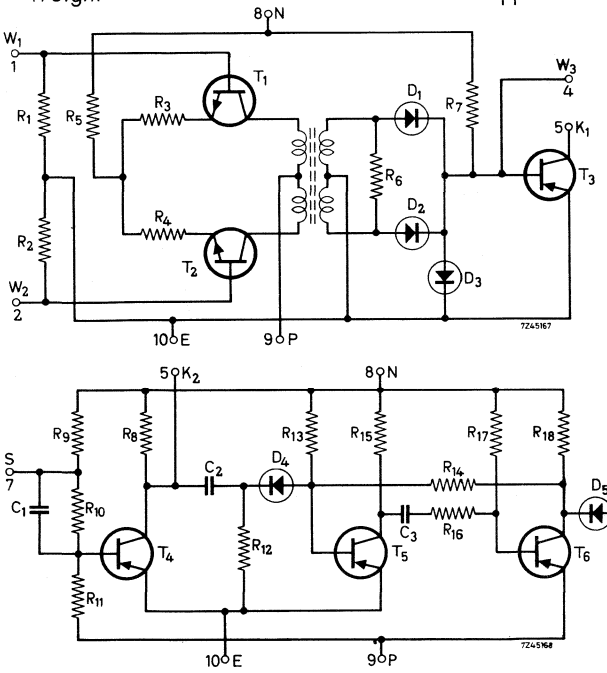
# READ AMPLIFIER

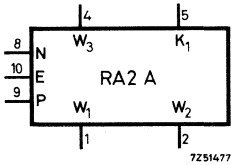
Colour : yellow

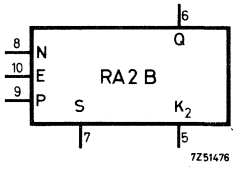
This read - or sense amplifier, consisting of two circuit blocks of standard dimensions called RA 2 A and RA 2 B, is designed to amplify the signals originating from the sense wire of ferrite-core memories.
The unit RA 2 A, to which the sense voltage is applied, contains a pre-amplifier circuit and a full wave rectifier circuit.
The input is balanced, so either positive going or negative going input signals can be applied.
Its output signal is applied to the input of the second unit RA 2 B, which contains a strobing circuit as well as a pulse stretching circuit. The output of the RA 2 B can be used directly to set a flip-flop of the 100 kHz range on its W-input terminal.

Ambient temperature range:

| | |
|---|---|
| operating | 0 to + 60 °C |
| storage | - 25 to + 75 °C |
| Weight | approx. 2 × 20 g |




Drawing symbols

Terminal Location

RA 2 A:

Terminal 1 = $W_1$ } input
2 = $W_2$ }
3 = not connected
4 = $W_3$ = terminal for external resistor
5 = $K_1$ = to connect to terminal 5 of RA 2 B
6 = not connected
7 = not connected
8 = N = supply -6V
9 = P = supply +6V
10 = E = common supply 0V

RA 2 B:

Terminal 1 = not connected
2 = not connected
3 = not connected
4 = not connected
5 = $K_2$ = to connect to terminal 5 of RA 2 A
6 = Q = output
7 = S = input STROBE pulse
8 = N = supply -6V
9 = P = supply +6V
10 = E = common supply 0V

Power Supply

RA 2 A:

Terminal 8 = $V_N$ = -6V ± 5%, $-I_N$ = 12.8 mA } nominal values
9 = $V_P$ = +6V ± 5%, $I_P$ = 11.5 mA }
10 = $V_E$ = 0V common

RA 2 B:

Terminal 8 = $V_N$ = -6V ± 5%, $-I_N$ = 15.3 mA } nominal values
9 = $V_P$ = +6V ± 5%, $I_P$ = 9.1 mA }
10 = $V_E$ = 0V common

Notes
- The data given apply to the most adverse supply voltages for a combination of units, namely $V_N$ = -5.7V and $V_P$ = + 6.3V.
- The temperatures 0 °C and +60 °C, and the tolerances on the supply voltages are absolute limiting values.
- When a current is flowing towards the unit, the positive sign is used.

INPUT DATA

Input impedance between $W_1$ and $W_2$ terminals: approx. 250 Ω

Input voltage:

W-terminals:

Transistor $T_3$ conducting : $V_{W_1W_2}$ = max 8.5 mV
Transistor $T_3$ non-conducting: $V_{W_1W_2}$ = min 27 mV

The sensitivity of the read amplifier RA 2 A can be adjusted with the aid of an external resistor between terminal $W_3$ and $V_N$ or $V_P$. The resistor connected to $V_N$ decreases the sensitivity (absolute min. value is 1.6 kΩ), whilst the resistor connected to $V_P$ increases the sensitivity (absolute min. value is 15 kΩ). This permits a sensitivity adjustment to match the threshold level of the read amplifier (where transistor $T_3$ starts to conduct) to the output sense voltage of a certain memory stack.

S-terminals:

Transistor $T_4$ conducting : $-V_S$ = min. 3.24V, $I_S$ = max. 100 µA
= max. $-V_N$
Transistor $T_4$ non-conducting: $-V_S$ = max. 0.85V
= min. 0V , $I_S$ = max. 2.5 mA

OUTPUT DATA

When $K_1$ - terminal of the RA 2 A is connected to the $K_2$ - terminal of the RA 2 B, transistor $T_6$ of the latter will be in the non-conducting state, as soon as transistor $T_3$ of RA 2 A as wel as transistor $T_4$ of RA 2 B have reached their cut-off state. This situation is required for setting a FF1, FF2, FF3 or FF4 on its input W - terminal.

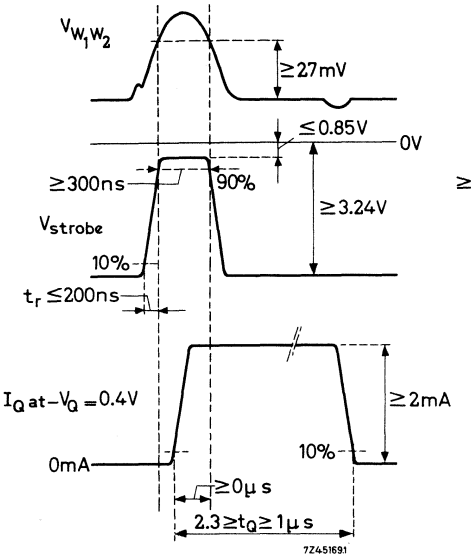
Transistor $T_6$ of RA 2 B non-conducting:

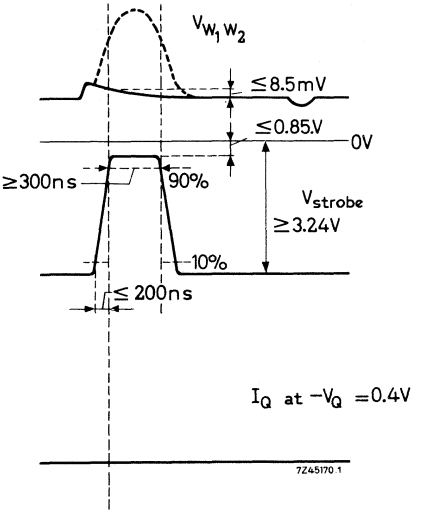
Voltage $-V_Q$ = min. 0.4V (at $I_Q$ = 2 mA)
Duration of the output pulse $t_Q$ = min. 1.0 µs
= max. 2.3 µs

Transistor $T_6$ of RA 2 B conducting:

Max. permissible voltage at output terminal Q is + 5V
At $-V_Q$ = 0.4V $-I_Q$ = max. 70 µA

The figure below elucidates the two situations, namely transistor $T_6$ of the RA 2 B conducting or cut-off. Its state is determined by the fact whether the input voltage $V_{W_1W_2}$ and the strobe pulse $V_S$ meet their respective minimum requirements.

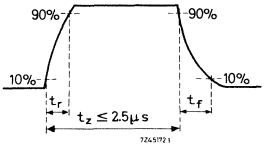


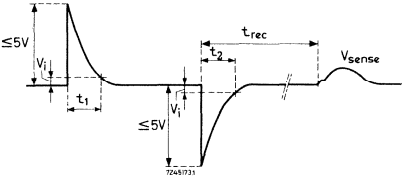

## GENERAL REQUIREMENTS

### Inhibit Current

1) The rise time $t_r$ and fall time $t_f$ of the current $I_Z$ through the inhibit wire should have such a slope, that the induced voltage on the sense wire meets the condition:
$t_1 = t_2$ = max. 1.5 µs at $V_i$ = 27 mV ± 1 mV

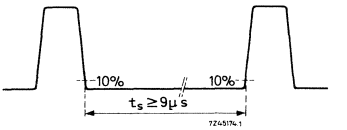



2) The minimum recovery time $t_{rec}$ between the inhibit pulse and the read pulse has to be min. 5 µs for $t_1 = t_2$ = max. 1.5 µs at $V_i$ = 27 mV ± 1 mV. (recovery time RA 2 A)



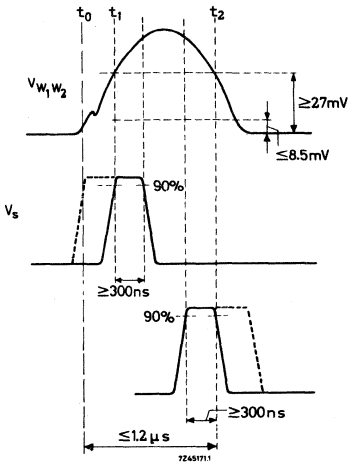

### Strobe Pulse

1) The minimum time between two successive strobe pulses has to be min. 9 µs.
(recovery time RA 2 B)



2) When $V_{W1W2}$ = min 27 mV and $-V_S$ = max 0.85 V a negative going output pulse is generated on the output terminal of the RA 2B. The coincidence of the input voltage $V_{W1W2}$, measured between the times $t_1$ and $t_2$, and the strobe pulse $V_S$, measured at the 90% level, has to be min 300 ns.
The two extreme situations are elucidated in the figure beside.

3) When however the sense wire is also carrying interference or disturbing signals, the strobe pulse $V_S$ has to be situated very precisely with respect to the input voltage $V_{W1W2}$.



# Circuit blocks

# 10-Series

# INTRODUCTION

The "10-series" presents a range of circuit blocks, developed to meet the requirements of the industry for machine-control, process control, data handling, measuring- and signalling systems. With this "10-series", systems are designed and built quickly, economically and with the utmost reliability.

The "10-series" offers a complete range, consisting of various logic elements together with all necessary auxiliary units including timers, pulse shapers, input and output devices. Moreover, all accessories for a quick and easy construction of equipment are available e.g. power supplies, printed-wiring boards, etc., see section "ACCESSORIES FOR CIRCUIT BLOCKS 10-SERIES".

Types of circuit blocks

In this series the following units and assembled panels are available:

| description | abbreviation | catalog number | page |
|---|---|---|---|
| Dual positive gate inverter amplifier | 2.GI 10 | 2722 004 08001 | D17 |
| Dual positive gate inverter amplifier | 2.GI 11 | 2722 004 08011 | D21 |
| Dual positive gate inverter amplifier | 2.GI 12 | 2722 004 08021 | D25 |
| Flip-flop | FF 10 | 2722 004 00001 | D29 |
| Flip-flop | FF 11 | 2722 004 00011 | D33 |
| Flip-flop | FF 12 | 2722 004 00021 | D39 |
| Dual trigger gate | 2.TG 13 | 2722 004 15001 | D45 |
| Dual trigger gate | 2.TG 14 | 2722 004 15011 | D49 |
| Quadruple trigger gate | 4.TG 15 | 2722 004 15021 | D53 |
| Timer unit | TU 10 | 2722 004 18001 | D57 |
| Gate amplifier | GA 11 | 2722 004 17001 | D63 |
| One-shot multivibrator | OS 11 | 2722 004 10011 | D69 |
| Pulse driver | PD 11 | 2722 004 13011 | D75 |
| Pulse shaper | PS 10 | 2722 004 11001 | D81 |
| Relay driver | RD 10 | 2722 004 16001 | D85 |
| Relay driver | RD 11 | 2722 004 16011 | D89 |
| Power amplifier | PA 10 | 2722 032 00021 | D93 |
| Printed-wiring board for PA 10 | PAA 10 | 4322 026 38680 | D219 |
| Numerical indicator tube driver | ID 10 | 2722 004 20001 | D97 |
| Decade counter/numerical indicator tube driver assembly | DCA 10 | 2722 009 020.. | D103 |
| Dual decade counter/numerical indicator tube driver assembly | 2.DCA 11 | 2722 009 020.. | D123 |
| Dual decade counter assembly | 2.DCA 12 | 2722 009 020.. | D141 |

| description | abbreviation | catalog number | page |
|---|---|---|---|
| Reversible decade counter/numerical indicator tube driver assembly | BCA 10 | 2722 009 021.. | D161 |
| Dual shift register assembly | 2.SRA 10 | 2722 009 03001 | D189 |
| Reversible shift register assembly | RSR 10 | 2722 009 03011 | D201 |

A number of static input and output devices can be used in conjunction with 10-series circuit blocks, see chapter INPUT/OUTPUT DEVICES.

Economic equipment design and construction are inherent to the following features:

- all circuits are compatable with little circuit diversity permitting simple and direct interconnections of the blocks within the range
- high "fan-out" figures and built-in logic facilities reduce the total number of blocks in a system considerably. They also facilitate later additions and modifications
- easy to use loading table enables the system design to be completed quickly
- the possibility of extending gate-, trigger-, and set-inputs makes the circuit blocks particularly valuable, where flexibility in equipment design is required
- input and output currents of the blocks are designed in a way that external components are unnecessary. Only for extension of the number of inputs, diodes have to be mounted externally
- the uniformity of terminal configuration reduces the time for interwiring the blocks and facilitates the design of printed-wiring boards

Outstanding reliability has been secured by:

- "worst-case" design of all circuits, where calculations have been performed with end-of-life data of all components
- use of professional semi-conductors
- careful testing and inspection of individual components and assemblies before, during and after manufacture
- quality control on running factory production, which ensures a product of equal and high quality
- built-in threshold against interference, which render the "10-series" particularly attractive for use in industrial environments
- printed-wiring circuits with plated through holes; the encapsulation and sealing techniques give the circuit block virtual immunity from the effects of humidity, vibration and shock

→ For detailed design and application information the publication "Practical circuits with 10-series Circuit blocks" (order no. 9399 263 00401) should be consulted.

# CONSTRUCTION

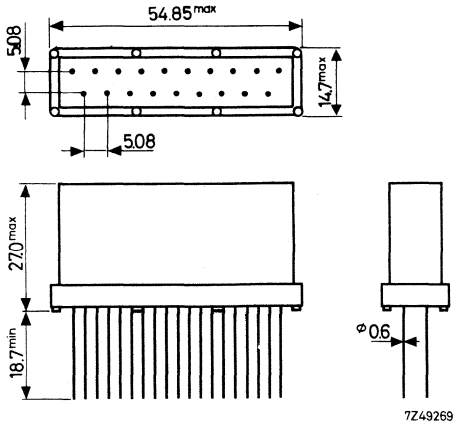
A circuit block is a small encapsulated unit containing a basic electronic circuit, designed to accept and operate upon a specific type of input signal and to produce a specific type of electrical output. A number of different blocks can be combined to form larger parts of electronic systems.

The blocks are housed in standard cases of two different heights.
The maximum overall dimensions are:

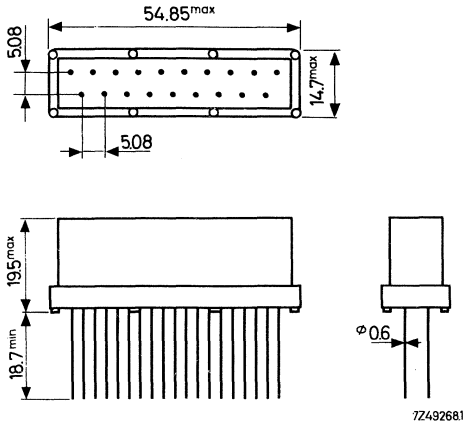
High standard case 54.85 mm x 14.70 mm x 27.00 mm
Low standard case 54.85 mm x 14.70 mm x 19.50 mm

Both cases have 19 terminals, protruding the bottom side of the cases in two rows.
The distance between the two rows is 5.08 mm ± 0.1 (0.2") and the distance between the wires in one row is 5.08 mm ± 0.1 (0.2"), in accordance with the IEC standard hole grid for printed-wiring boards.

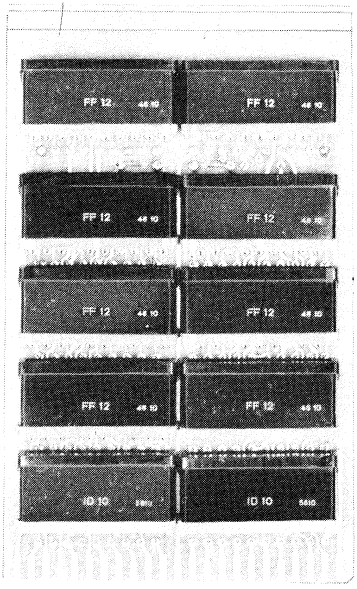
The unit can be mounted in any position.
To insulate the metal can electrically from the printed-wiring conductors for vertical and horizontal mounting on a printed-wiring board the terminal side of the unit is equipped with a plastic sleeve; for horizontal mounting the top side of the unit can be mechanically secured to the board with the aid of a special locking cap.




High standard case




Low standard case




RZ 22603-9

Assembled printed-wiring board

# CHARACTERISTICS

## Temperature range

Operating temperature: -25 °C to +55 °C.
For temperatures below 0 °C, derated output data are issued in the individual data sheets.
Storage temperature: -55 °C to +75 °C.

## Count rate

For a.c. logic applications: approx. 30 kHz
For d.c. logic applications: approx. 65 kHz

## Power supply

| terminals | | operating |
|---|---|---|
| 9 | $V_N$ | -12 V ± 5% |
| 10 | $V_E$ | 0 V common |
| 19 | $V_P$ | +12 V ± 5% |

The average power dissipation of the logic blocks is 50 to 100 mW.

## Logic levels

| | operating | | limiting values | |
|---|---|---|---|---|
| | maximum | minimum | diode inputs | outputs |
| State "1" | $V_P$ | 2/3 $V_P$ | 13V | 15V |
| State "0" | +0.3 V | 0 V | -2V | 0V |

# TEST SPECIFICATIONS

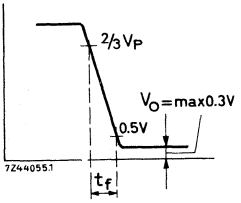
Before and during manufacture samples of circuit blocks are regularly subjected to the following tests:

1. Vibration test according to method 201A of MIL-STD-202.
   Frequency 10-55 Hz, with amplitude of 0.76 mm.
2. Shock test according to method 202A of MIL-STD-202.
   Acceleration 50 g in 3 perpendicular directions.
3. Temperature-cycling test according to method 102A of MIL-STD-202.
   Condition D, 5 cycles from - 55 °C to + 85 °C.
4. Accelerated humidity test according to method 106A of MIL-STD-202.
   10 cycles as indicated in Fig. 1 page 2 of method 106A.
5. Long-term humidity test according to MIL-STD-202, method 1034. Units not operating. Duration 56 days at 40 °C and relative humidity 95%.
   Measurements after 7, 14, 28 and 56 days.
6. As item 5, but units operating under the most unfavourable electrical conditions regarding supply voltages, output load and input characteristics.
7. Long-term test at maximum temperature according to method 108 of MIL-STD-202.
   Test condition E, 55 °C during 1500 hours.
   Units operating under the most unfavourable electrical conditions.
   Measurements after 250, 500, 1000 and 1500 hours.
8. Terminals tested on strength, tests on mounting, soldering, lacquer and coding.

# TIME DEFINITIONS

1 Fall time : $t_f$

The time in which the input- respectively output voltage changes from 2/3 Vp to 0.5 V.

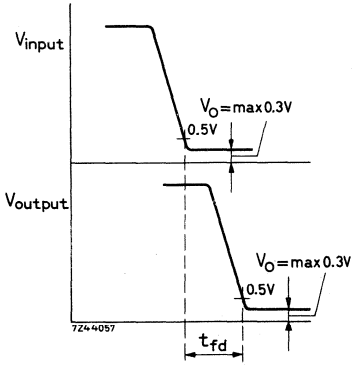



2 Fall delay : $t_{fd}$

The time, between the 0.5V-points of the negative-going transients of the input- and output voltages.
This fall delay $t_{fd}$ is related to:

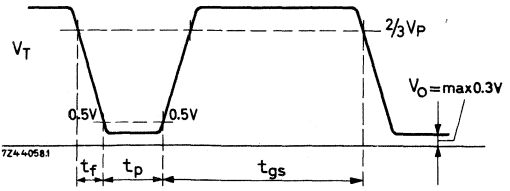
a) Gate invertors (GI's) — the input- and output voltage, the latter measured over 2 stages.

b) Flip-flops (FF's) — the input voltage and the negative-going output voltage.



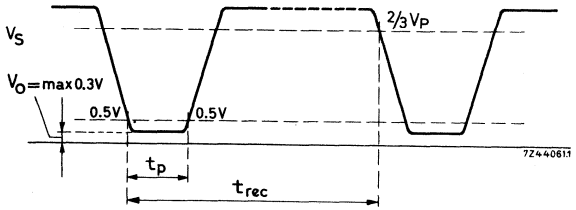

3 Trigger input data FF's and TG's

$t_f$ = fall time
$t_p$ = pulse duration
$t_{gs}$ = trigger gate setting time



4 Set/reset input data FF's

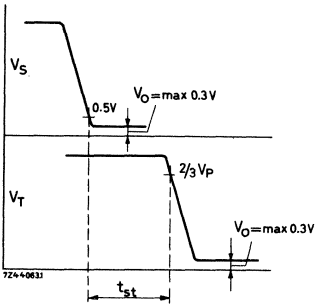
$t_p$ = the duration of the set/reset (S)-pulse
$t_{rec}$ = the recovery time, which is the time between the successive pulses on the different S-terminals of a flip-flop.

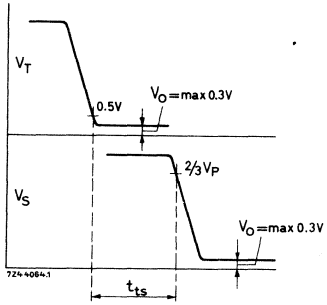



5 Inhibiting time between S- and T-signals of FF's

a) $t_{st}$ = the inhibiting time between a set(S)-signal and a successive trigger(T)-signal of a flip-flop.

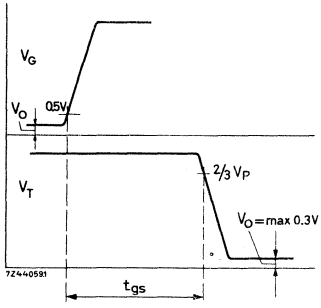
b) $t_{ts}$ = the inhibiting time between a trigger(T)-signal and a successive set(S)-signal of a flip-flop.



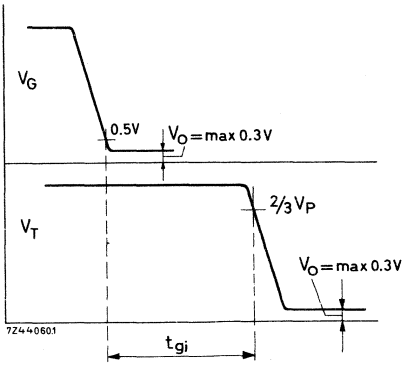

6 Trigger gate setting-time : $t_{gs}$

The time the gate(G)-signal shall be present in advance to open the gate for the trigger(T)-signal.



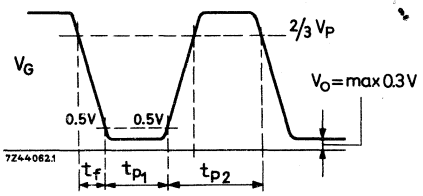
7 Trigger gate inhibiting time : $t_{gi}$

The time the gate(G)-signal shall be present in advance to close the gate for the trigger(T)-signal.




8 Input data GI's

$t_{p1}$ = the duration of "positive low" input signals
$t_{p2}$ = the duration of "positive high" input signals



# INPUT AND OUTPUT DATA

INPUT DATA

| unit | terminal | note | direct current | transient charge |
|---|---|---|---|---|
| FF11, FF12 | G | | 1.1 mA | 1.2 nC |
| 2.TG13, 2.TG14, 4.TG15 | T | gate open | 1.1 mA | 3.4 nC |
| FF10, FF11, FF12 | S | | 1.95 mA | 2.8 nC |
| 2.GI 10, 2.GI 11, 2.GI 12 | G | | 1.1 mA | 2.1 nC |
| GA11 | G | | 1.1 mA | 1.2 nC |
| OS11 | G | | 1.1 mA | 1.2 nC |
| | T | gate open | 1.1 mA | 2.3 nC |
| TU10, PD11 | G | | 1.1 mA | 1.2 nC |
| | T | gate open | 1.1 mA | 3.2 nC |
| RD10, RD11 | G | | 4.7 mA | 3.4 nC |
| PA10 | G | | 5.3 mA | 5.2 nC |

OUTPUT DATA

| unit | terminal | note | direct current | transient charge |
|---|---|---|---|---|
| FF10, FF11, FF12 | $Q_1$, $Q_2$ | | 8.2 mA | 27 nC |
| 2.GI 10, 2.GI 11, 2.GI 12 | Q | | 8.2 mA | 9 nC |
| GA11 | Q | | 62 mA | 75 nC |
| OS11 | $Q_1$ | | 8.6 mA | 24 nC |
| | $Q_2$ | | 12.8 mA | 29 nC |
| TU10 | Q | | 32 mA | 30 nC |
| PD11 | Q | | 100 mA | 185 nC |
| PS10 | Q | | 10 mA | 39 nC |
| RD10, RD11 | Q | | 200 mA | |
| PA10 | Q | | 2 A | |

## LOADING RULES

1 Verify that the sum of the required d.c. input currents of the driven units does not exceed the available d.c. output current of the driving unit.

2 When however T-inputs are incorporated in the driven units, the transient charges must also be verified.

3 Only driven units, of which all inputs are high, do load the driving stage during the negative going transient.

4 The wiring capacitance consumes an extra charge of 0.007 nC/pF.

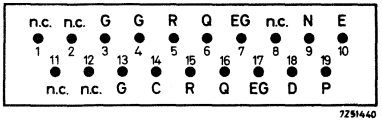
5 T-inputs of closed gates do not require any current or charge.

6 The verifications mentioned above hold for operations at the worst combination of supply voltage tolerance (12V $\pm$ 5%) and ambient temperature between 0 and +55 °C. For temperatures below 0 °C, derating figures are issued in the individual data sheets.

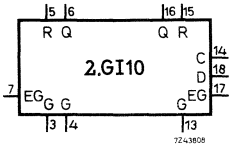
# DUAL POSITIVE GATE INVERTER AMPLIFIER

The unit comprises a single input-and a double input positive diode gate-inverter combination, together with one separate diode which can be used to extend the number of gate (G) inputs on any of the two circuits at the extension gate inputs EG.
The collectors Q of the two transistors are not connected with their corresponding collector resistors R. Therefore with the two transistors a logical operation can be performed by interconnecting the two collectors Q with one collector resistor R. The second collector resistor R must be left disconnected.
The circuit is mounted inside a sealed metal can with 19 wire terminals.

| | | |
|---|---|---|
| Ambient temperature range: | | |
| | operating | -25 to +55 °C<br>below 0 °C: derated output data |
| | storage | -55 °C to +75 °C |
| Weight | | approx. 30 g |
| Case | | low standard case |




terminal location

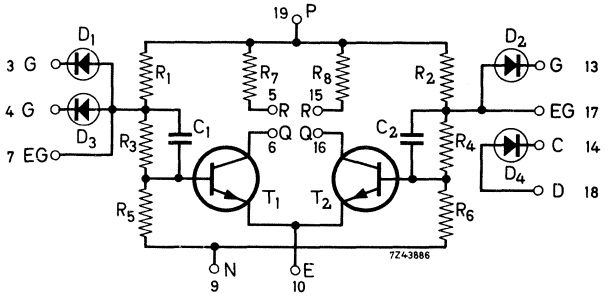



drawing symbol

## CIRCUIT DATA

Terminal

1 = not connected
2 = not connected
3 = G = gate input
4 = G = gate input
5 = R = connection collector resistor
6 = Q = output
7 = EG = extension gate input
8 = not connected
9 = N = supply −12 V
10 = E = common supply 0 V
11 = not connected
12 = not connected
13 = G = gate input
14 = C = cathode separate diode
15 = R = connection collector resistor
16 = Q = output
17 = EG = extension gate input
18 = D = anode separate diode
19 = P = supply +12 V




Power supply

Terminal 9 : $V_N$ = −12 V ±5%, $-I_N$ = 0.6 mA
10 : $V_E$ = 0 V common
19 : $V_P$ = +12 V ±5%,
$I_P$ = 2.8 mA (both transistors non-conducting)
= 3.9 mA (one transistor conducting)
= 5.1 mA (both transistors conducting)

The current values are nominal

INPUT REQUIREMENTS (at $V_P$ = 11.4 V and $V_N$ = −12.6 V unless specified differently).

Transistor conducting (output level "positive low")

Voltage at all gate inputs $V_G$ = min. 2/3 $V_P$
= max. $V_P$

Type of diodes and maximum number connected in parallel at terminal EG:
12 x AAY21/AAY32

Transistor non-conducting (output level "positive high")

Voltage at one or more gate inputs $V_G$ = min. 0 V
= max. 0.3 V

Total required direct current $-I_{GD}$ = max. 1.1 mA

Total required transient charge when $V_G$ changes from 2/3 $V_p$ to 0.5 V in 1.5 µs $-Q_{GT}$ = max. 2.1 nC

Time data

Pulse duration $t_{p1}$ = min. 6 µs, $t_{p2}$ = min. 6 µs } See point 8*

OUTPUT DATA (at $V_P$ = 11.4 V and $V_N$ = -12.6 V unless specified differently).

Voltages, direct currents and transient charges

Transistor conducting (output level "positive low")

Voltage $V_Q$ = min. 0 V
= max. 0.3 V

Available direct current $I_{QD}$ = min. 8.2 mA
min. 7.0 mA ($T_{amb}$ = min. - 25 °C)**

Available transient charge when $V_Q$ changes from 2/3 Vp to 0.5 V in 1.5 µs $Q_{QT}$ = min. 9 nC
min. 7 nC ($T_{amb}$ = min. - 25 °C)**

If 2 or 3 collectors Q are paralleled, all but one collector resistor R must be left disconnected. If 4 to 16 collectors Q are paralleled, all but two collector resistors R must be left disconnected. In the latter case the available direct current respectively available transient charge must be reduced to: $I_{QD}$ = min. 6.7 mA
$Q_{QT}$ = min. 7.4 nC
$I_{QD}$ = min. 5.5 mA
$Q_{QT}$ = min. 5.4 nC } ($T_{amb}$ = min -25 °C)**

Transistor non-conducting (output level "positive high")

Voltage $V_Q$ = min. 2/3 Vp
= max. Vp

*Of section "Time definitions 10-series circuit blocks".
** Between 0 and - 25 °C to be derived by linear interpolation.

Time data

| | | | |
|---|---|---|---|
| Fall time | $t_f$ | = max. 1.5 µs | See point 1* |
| Fall delay | $t_{fd}$ | = max. 3 µs | See point 2* |

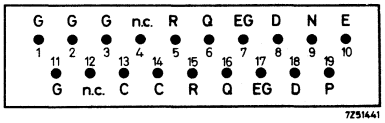
Maximum wiring capacitance 200 pF.

*) Of section "Time definitions 10-series circuit blocks".

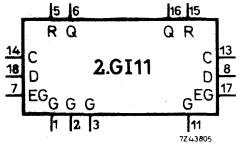
# DUAL POSITIVE GATE INVERTER AMPLIFIER

The unit comprises a single input-and a triple input positive diode gate-inverter combination, together with two separate diodes which can be used to extend the number of gate (G) inputs on any of the two circuits at the extension gate inputs EG.
The collectors Q of the two transistors are not connected with their corresponding collector resistor R. Therefore with the two transistors a logical operation can be performed by interconnecting the two collectors Q with one collector resistor R. The second collector resistor R must be left disconnected.
The circuit is mounted inside a sealed metal can with 19 wire terminals.

| | | |
|---|---|---|
| Ambient temperature range: | | |
| | operating | -25 to +55 °C<br>below 0 °C: derated output data |
| | storage | -55 °C to +75 °C |
| Weight | | approx. 40 g |
| Case | | high standard case |




terminal location

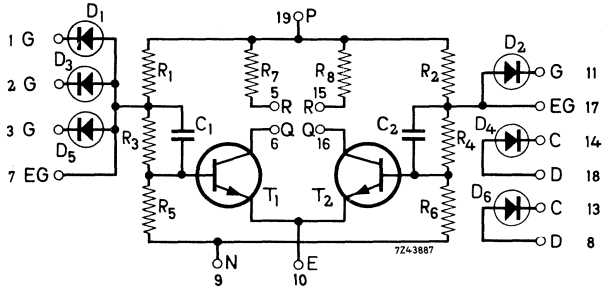



drawing symbol

CIRCUIT DATA

Terminal

1 = G = gate input
2 = G = gate input
3 = G = gate input
4 = not connected
5 = R = connection collector resistor
6 = Q = output
7 = EG = extension gate input
8 = D = anode separate diode
9 = N = supply −12V
10 = E = common supply 0 V
11 = G = gate input
12 = not connected
13 = C = cathode separate diode
14 = C = cathode separate diode
15 = R = connection collector resistor
16 = Q = output
17 = EG = extension gate input
18 = D = anode separate diode
19 = P = supply +12V




Power supply

Terminal 9 : $V_N$ = −12 V ±5%, $-I_N$ = 0.6 mA
10 : $V_E$ = 0 V common
19 : $V_P$ = +12 V ±5%,
$I_P$ = 2.8 mA (both transistors non-conducting)
= 3.9 mA (one transistor conducting)
= 5.1 mA (both transistors conducting)

The current values are nominal

INPUT REQUIREMENTS (at $V_P$ = 11.4 V and $V_N$ = −12.6 V unless specified differently).

Transistor conducting (output level "positive low").

Voltage at all gate inputs $V_G$ = min. $2/3V_P$
max. $V_P$

Type of diodes and maximum number connected in parallel at terminal EG:
12xAAY21/AAY32

Transistor non-conducting (output level "positive high").

Voltage at one or more gate inputs $V_G$ = min. 0 V = max. 0.3 V

Total required direct current $-I_{GD}$ = max. 1.1 mA

Total required transient charge when $V_G$ changes from 2/3 Vp to 0.5 V in 1.5 µs $-Q_{GT}$ = max. 2.1 nC

Time data

Pulse duration $t_{p1}$ = min. 6 µs; $t_{p2}$ = min. 6 µs } See point 8*

OUTPUT DATA (at $V_P$ = 11.4 and $V_N$ = -12.6 V unless specified differently).

Voltages, direct currents and transient charges

Transistor conducting (output level "positive low")

Voltage $V_Q$ = min. 0 V = max. 0.3 V

Available direct current $I_{QD}$ = min. 8.2 mA = min. 7.0 mA ($T_{amb}$ = min. -25 °C)**

Available transient charge when $V_Q$ changes from 2/3 Vp to 0 V in 1.5 µs $Q_{QT}$ = min. 9 nC = min. 7 nC ($T_{amb}$ = min. -25 °C)**

If 2 or 3 collectors Q are paralleled all but one collector resistor R must be left disconnected. If 4 to 16 collectors Q are paralleled, all but two collector resistors R must be left disconnected. In the latter case the available direct current respectively available transient charge must be reduced to: $I_{QD}$ = min. 6.7 mA, $Q_{QT}$ = min. 7.4 nC; $I_{QD}$ = min. 5.5 mA, $Q_{QT}$ = min. 5.4 nC } ($T_{amb}$ = min -25°C)**

Transistor non-conducting (output level "positive high")

Voltage $V_Q$ = min. 2/3 Vp = max. $V_P$

* Of section "Time definitions 10-series circuit blocks".

** Between 0 and -25 °C to be derived by linear interpolation.

Time data

| | | | |
|---|---|---|---|
| Fall time | $t_f$ | = max. 1.5 µs | See point 1* |
| Fall delay | $t_{fd}$ | = max. 3 µs | See point 2* |

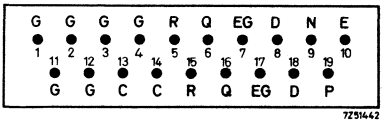
Maximum wiring capacitance 200 pF.

* Of section "Time definitions 10-series circuit blocks".

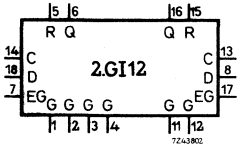
# DUAL POSITIVE GATE INVERTER AMPLIFIER

The unit comprises a double input- and a quadruple input positive diode gate-inverter combination, together with two separate diodes which can be used to extend the number of gate (G) inputs on any of the two circuits at the extension gate inputs EG.
The collectors Q of the two transistors are not connected with their corresponding collector resistors R. Therefore with the two transistors a logical operation can be performed by interconnecting the two collectors Q with one collector resistor R. The second collector resistor R must be left disconnected.
The circuit is mounted inside a sealed metal can with 19 wire terminals.

| | | |
|---|---|---|
| Ambient temperature range: | | |
| | operating | -25 to +55 °C<br>below 0 °C: derated output data |
| | storage | -55 °C to +75 °C |
| Weight | | approx. 40 g |
| Case | | high standard case |



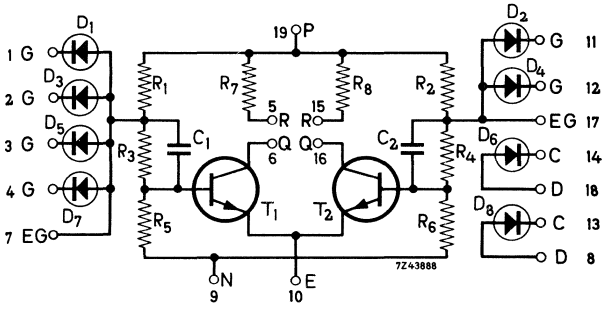

terminal location




drawing symbol

CIRCUIT DATA

Terminal
1 = G = gate input
2 = G = gate input
3 = G = gate input
4 = G = gate input
5 = R = connection collector resistor
6 = Q = output
7 = EG = extension gate input
8 = D = anode separate diode
9 = N = supply −12 V
10 = E = common supply 0 V
11 = G = gate input
12 = G = gate input
13 = C = cathode separate diode
14 = C = cathode separate diode
15 = R = connection collector resistor
16 = Q = output
17 = EG = extension gate input
18 = D = anode separate diode
19 = P = supply +12 V




Power supply

Terminal 9 : $V_N$ = −12 V ± 5%, $-I_N$ = 0.6 mA
10 : $V_E$ = 0 V common
19 : $V_P$ = +12 V ± 5%,
$I_P$ = 2.8 mA (both transistors non-conducting)
= 3.9 mA (one transistor conducting)
= 5.1 mA (with transistors conducting)

} Current values are nominal

INPUT REQUIREMENTS (at $V_P$ = 11.4 V and $V_N$ = -12.6 V unless specified differently).

Transistor conducting (output level "positive low").

Voltage at all gate inputs $V_G$ = min. 2/3 $V_P$, max. $V_P$

Type of diodes and maximum number connected in parallel at terminal EG: 12 x AAY21/AAY32

Transistor non-conducting (output level "positive high").

Voltage at one or more gate inputs $V_G$ = min. 0 V, = max. 0.3 V

Total required direct current $-I_{GD}$ = max. 1.1 mA

Total required transient charge, when $V_G$ changes from 2/3 $V_P$ to 0.5 V in 1.5 µs $-Q_{GT}$ = max. 2.1 nC

Time data

Pulse duration $t_{p1}$ = min. 6 µs, $t_{p2}$ = min. 6 µs } See point 8*

OUTPUT DATA (at $V_P$ = 11.4 V and $V_N$ = -12.6 V, unless specified differently).

Voltages, direct currents and transient charges

Transistor conducting (output level "positive low")

Voltage $V_Q$ = min. 0 V, = max. 0.3 V

Available direct current $I_{QD}$ = min. 8.2 mA, = min. 7.0 mA ($T_{amb}$ = min. - 25 °C)**

Available transient charge when $V_Q$ changes from 2/3 $V_P$ to 0.5 V in 1.5 µs $Q_{QT}$ = min. 9 nC, = min. 7 nC ($T_{amb}$ = min - 25 °C)**

If 2 or 3 collectors Q are paralleled all but one collector resistor R must be left disconnected. If 4 to 16 collectors Q are paralleled,

* Of section "Time definitions 10-series circuit blocks".

** Between 0 and - 25 °C to be derived by linear interpolation.

all but two collector resistors R must be left disconnected. In the latter case the available direct current respectively available transient charge must be reduced to: $I_{QD}$ = min. 6.7 mA
$Q_{QT}$ = min. 7.4 nC
$I_{QD}$ = min. 5.5 mA
$Q_{QT}$ = min. 5.4 nC

($T_{amb}$ = min. -25 °C)**

| | | | |
|---|---|---|---|
| Transistor non-conducting | (output level "positive high") | | |
| Voltage | $V_Q$ | = min. 2/3 $V_P$<br>= max. $V_P$ | |
| Time data | | | |
| Fall time | $t_f$ | = max. 1.5 µs | See point 1* |
| Fall delay | $t_{fd}$ | = max. 3 µs | See point 2* |

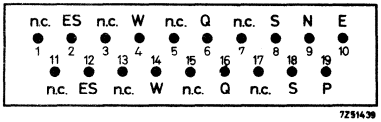
Maximum wiring capacitance 200 pF.

* Of section "Time definitions 10-series circuit blocks".
** Between 0 and - 25 °C to be derived by linear interpolation.

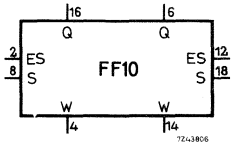
# FLIP-FLOP

The unit comprises a set/reset bi-stable multivibrator circuit. The number of set/reset (S) inputs can be extended with the aid of external diodes at the extension inputs ES.
The circuit constitutes a memory function, driven by means of a d.c. level at the S-inputs. In conjunction with the dual trigger gates 2TG 13 or 2TG 14 an a.c. -driven (triggered) flip-flop can be formed, normally used in binary counters and shift registers; in conjunction with the quadruple trigger gate 4TG 15 one stage of a bi-directional counter or bi-directional shift register is formed. Up to 10 trigger gates can be paralleled at W-inputs of the flip-flop. In these applications the Q-output terminals of the trigger gates are connected to the W-input terminals of the flip-flop FF 10.
The circuit is mounted inside a sealed metal can with 19 wire terminals.

| | | |
|---|---|---|
| Ambient temperature range: | | |
| | operating | -25 to +55 °C |
| | | below 0 °C: derated output data |
| | storage | -55 °C to +75 °C |
| Weight | | approx. 30 g |
| Case | | low standard case |



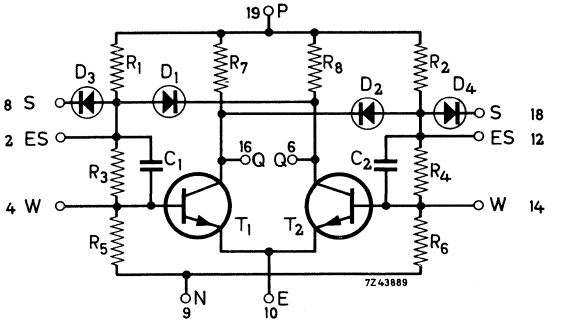

terminal location




drawing symbol

CIRCUIT DIAGRAM

Terminal 1 = not connected
2 = ES = extension set/reset input
3 = not connected
4 = W = extension trigger gate
5 = not connected
6 = Q = output
7 = not connected
8 = S = set/reset input
9 = N = supply - 12 V
10 = E = common supply 0 V
11 = not connected
12 = ES = extension set/reset input
13 = not connected
14 = W = extension trigger gate
15 = not connected
16 = Q = output
17 = not connected
18 = S = set/reset input
19 = P = supply + 12 V




Power supply

Terminal 9 : $V_N$ = -12V ±5%, $-I_N$ = 0.6 mA
10 : $V_E$ = 0 V common
19 : $V_P$ = +12V ±5%, $I_P$ = 4.8 mA
} nominal value of the current

INPUT REQUIREMENTS (at $V_P$ = 11.4V and $V_N$ = -12.6V unless specified differently).

Set/reset input (S-terminals)

A d.c. voltage level is applied to terminal S. A "positive low" voltage (between 0 V and 0.3 V) drives the corresponding transistor into the non-conducting state.

Transistor conducting (output level "positive low")

| | | |
|---|---|---|
| Voltage | $V_S$ = min. 2/3 $V_P$<br>= max. + $V_P$ | |
| | Type of diodes and maximum number connected in parallel at terminal ES: 12 x OA 85/OA 95 | |

Transistor non-conducting (output level "positive high")

| | | |
|---|---|---|
| Voltage | $V_S$ = min. 0 V<br>= max. 0.3 V | |
| Required direct current | $-I_{SD}$ = max. 1.95 mA | |
| Required transient charge when $V_S$ changes from 2/3 $V_P$ to 0.5 V in 1.5 µs | $-Q_{ST}$ = max. 2.8 nC | |
| Time data | | |
| Pulse duration | $t_p$ = min. 2 µs | See point 4 * |
| Recovery time | $t_{rec}$ = min. 15 µs | |

Base-input (W-terminal)

| | | |
|---|---|---|
| Capacitance (wiring + output TG13/ TG14/TG15) | $C_W$ = max. 100 pF | |

OUTPUT DATA (at $V_P$ = 11.4 V and $V_N$ = −12.6 V, unless specified differently).

Voltages, direct currents and transient charges

Transistor conducting (output level "positive low")

| | | |
|---|---|---|
| Voltage | $V_Q$ = min. 0 V<br>= max. 0.3 V | |
| Available direct current | $I_{QD}$ = min. 8.2 mA<br>= min. 6.6 mA ($T_{amb}$ = min. −25 °C)** | |
| Available transient charge, when $V_Q$ changes from 2/3 $V_P$ to 0.5 V in 1.5 µs | $Q_{QT}$ = min. 27 nC<br>min. 22 nC ($T_{amb}$ = min. −25 °C)** | |

Transistor non-conducting (output level "positive high")

| | | |
|---|---|---|
| Voltage | $V_Q$ = min. 2/3 $V_P$<br>= max. $V_P$ | |
| Time data | | |
| Fall time | $t_f$ = max. 1.5 µs | See point 1* |
| Fall delay | $t_{fd}$ = max. 2 µs | See point 2* |

Maximum wiring capacitance 200 pF

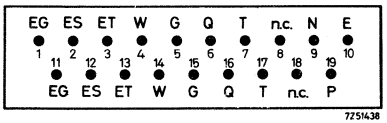
* Of section "Time definitions 10-series circuit blocks".

** Between 0 and −25 °C to be derived by linear interpolation.

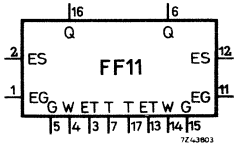
# FLIP-FLOP

The unit comprises a set/reset bi-stable multivibrator circuit with built-in trigger gates. The number of set/reset inputs, gate (G) inputs as well as the trigger (T) inputs can be extended by the aid of external diodes at the extension inputs ES, EG or ET respectively.
The circuit constitutes a memory function when driven by means of a d.c. level at the ES-inputs via an external diode or a negative-going trigger signal at the T-inputs.
In the case of trigger drive, the switching of the flip-flop can be controlled by a d.c. level applied to the built-in G-inputs (e.g. in shift registers), whilst the T-inputs are interconnected.
It can also be used as a binary divider, when the G-inputs are connected to the appropriate Q-outputs. With the aid of trigger gates 2TG 13 and 2TG 14 extra triggering facilities can be made by connecting their Q-outputs to the W-inputs of the flip-flop (e.g. in bi-directional shift registers and counters).
With the aid of the quadruple trigger gate 4TG 15, of which the Q-output terminals are connected to the appropriate W-input terminals of two units FF 11, two stages of a bi-directional counter or bi-directional shift register are formed.
Up to 9 extra trigger gates can be paralleled to one flip-flop.
The circuit is mounted inside a sealed metal can with 19 wire terminals.

| | | |
|---|---|---|
| Ambient temperature range: | | |
| | operating | -25 to +55 °C<br>below 0 °C: derated output data |
| | storage | -55 °C to +75 °C |
| Weight | | approx. 40g |
| Case | | high standard case |



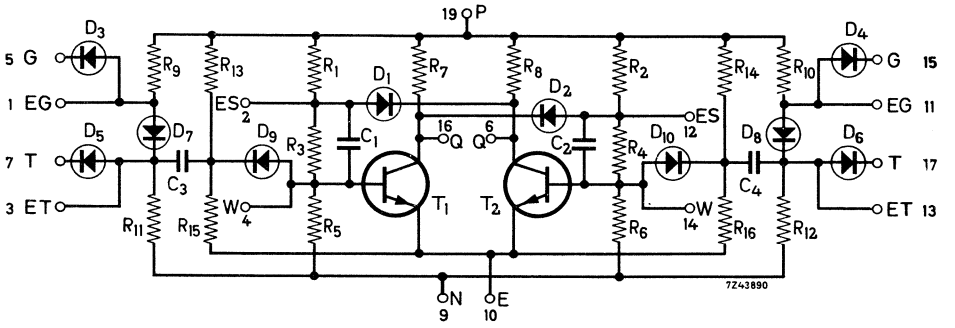

terminal location




drawing symbol

CIRCUIT DATA

Terminal
1 = EG = extension gate input
2 = ES = extension set/reset input
3 = ET = extension trigger input
4 = W = extension trigger gate
5 = G = gate input
6 = Q = output
7 = T = trigger input
8 = not connected
9 = N = supply -12 V
10 = E = common supply 0 V
11 = EG = extension gate input
12 = ES = extension set/reset input
13 = ET = extension trigger input
14 = W = extension trigger gate
15 = G = gate input
16 = Q = output
17 = T = trigger input
18 = not connected
19 = P = supply +12 V




Power supply

Terminal 9 : $V_N$ = -12 V ±5%, $-I_N$ = 1.1 mA
10 : $V_E$ = 0 V common
19 : $V_P$ = +12 V ±5%, $I_P$ = 7.0 mA
} nominal value of the current

INPUT REQUIREMENTS (at $V_P$ = 11.4V and $V_N$ = -12.6V unless specified differently).

Set/reset input (ES-terminals)

A d.c. voltage level $V_S$ is applied to the terminal ES via a diode (e.g. type OA 85/OA 95), the anode connected to terminal ES. A "positive low" voltage between 0V and 0.3V drives the corresponding transistor into the non-conducting state.

Transistor conducting (output level "positive low").

Voltage $V_S$ = min. $2/3V_P$,
= max. $+V_P$

Type of diodes and maximum number connected in parallel at terminal ES:
3 x OA 85/OA 95

Transistor non-conducting (output level "positive high").

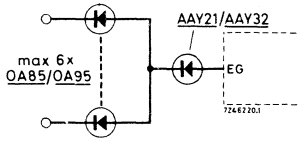
| | | |
|---|---|---|
| Voltage | $V_S$ = min. 0V<br>= max. 0.3V | |
| Required direct current | $-I_{SD}$ = max. 1.95 mA | |
| Required transient charge when $V_S$ changes from 2/3 Vp to 0.5 V in 1.5 µs | $-Q_{ST}$ = max. 2.8 nC | |
| Time data | | |
| pulse duration | $t_p$ = min. 2 µs | See point 4* |
| recovery time | $t_{rec}$ = min. 15 µs | |
| Time delay between S- and T-signals | $t_{ts}$ = min. 15 µs | See point 5* |

Gate-input (G-terminals)

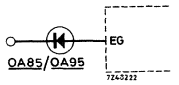
A d.c. voltage level is applied to terminal G. A "positive low" voltage closes the gate, whilst a "positive high" voltage (between 2/3 Vp and Vp) opens the gate.

Gate open

Voltage $V_G$ = min. 2/3 Vp
= max. Vp




Gate extension input EG: max number of parallel input diodes: 6 x OA85/OA95




Gate extension input EG: with only one input diode at EG

Gate closed

Voltage $V_G$ = min. 0V
= max. 0.3V

Required direct current $-I_{GD}$ = max. 1.1 mA

* Of section "Time definitions 10-series circuit blocks".

| | | |
|---|---|---|
| Required transient charge, when $V_G$ changes from 2/3 $V_P$ to 0.5 V in 1.5 µs | $-Q_{GT}$ = max. 1.2 nC | |
| Time data | | |
| Trigger gate setting time | $t_{gs}$ = min. 29 µs | See point 6* |
| Trigger gate inhibiting time | $t_{gi}$ = min. 29 µs | See point 7* |

Trigger input (T-terminals).

A negative-going voltage step is applied to the terminals T separately or to both terminals interconnected in the case of binary divider applications. This voltage step on terminal T drives the transistor into the non-conducting state if the corresponding gate has been opened by the appropriate input signal on terminal G.

| | Gate open | Gate closed |
|---|---|---|
| $V_G$ | = min. 2/3 $V_P$<br>= max. $V_P$ | = min. 0 V<br>= max. 0.3 V |
| Required direct current when $V_T$ = max. 0.3 V | $-I_{TD}$ = max. 1.1 mA | 0 mA |
| Required transient charge when $V_T$ changes from 2/3 $V_P$ to 0.5 V in 1.5 µs | $-Q_{TT}$ = max. 3.4 nC | 0 nC |
| Input noise level | $V_n$ = max. 1.2 V peak to peak | |
| | Recommended type of diode and maximum number connected in parallel at terminal ET: 6 x BAY 38 | |
| Time data | | |
| Fall time | $t_f$ = max. 1.5 µs | |
| Pulse duration | $t_p$ = min. 2 µs | See point 3* |
| Trigger gate setting time | $t_{gs}$ = min. 29 µs | |
| Time delay between T- and S-signals | $t_{ts}$ = min. 15 µs | See point 5* |

Base input (W-terminal)

Capacitance (wiring + output TG13/TG14/TG15): $C_W$ = max. 95 pF

* Of section "Time definitions 10-series circuit blocks".

OUTPUT DATA (At $V_P$ = 11.4V and $V_N$ = -12.6V, unless specified differently).

Voltages, direct currents and transient charges

| | | | |
|---|---|---|---|
| Transistor conducting | (output level "positive low") | | |
| Voltage | $V_Q$ | = min. 0V<br>= max. 0.3V | |
| Available direct current | $I_{QD}$ | = min. 8.2 mA<br>= min. 6.6 mA ($T_{amb}$ = min. -25 °C) ** | |
| Available transient charge, when $V_Q$ changes from 2/3Vp to 0.5V in 1.5 µs | $Q_{QT}$ | = min. 27 nC<br>= min. 22 nC ($T_{amb}$ = min. -25 °C)** | |
| Transistor non-conducting | (output level "positive high") | | |
| Voltage | $V_Q$ | = min. 2/3Vp<br>= max. $V_P$ | |
| Time data | | | |
| Fall time | $t_f$ | = max. 1.5 µs | See point 1* |
| Fall delay | $t_{fd}$ | = max. 2 µs | See point 2* |

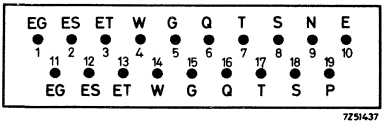
Maximum wiring capacitance 200 pF

* Of section "Time definitions 10-series circuit blocks".
** Between 0 and -25 °C to be derived by linear interpolation.

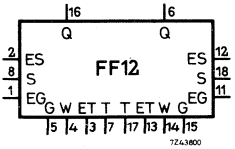
# FLIP-FLOP

The unit comprises a set/reset bi-stable multivibrator circuit with built-in trigger gates. The number of set/reset (S) inputs, the gate (G) inputs as well as the trigger (T) inputs can be extended with the aid of external diodes at the extension inputs ES, EG or ET respectively.
The circuit constitutes a memory function when driven by means of a d.c. level at the S-inputs or a negative-going trigger signal at the T-inputs. In the case of trigger drive, the switching of the flip-flop can be controlled by a d.c. level applied to the built-in G-inputs (e.g. in shift registers), whilst the T-inputs are interconnected. It can also be used as a binary divider, when the G-inputs are connected to the appropriate Q-outputs.
With the aid of trigger gates 2TG 13 and 2TG 14 extra triggering facilities can be made by connecting their Q-outputs to the corresponding W-inputs of the flip-flop (e.g. in bi-directional shift registers and counters).
With the aid of the quadruple trigger gate 4TG 15, of which the Q-output terminals are connected to the appropriate W-input terminals of two units FF 12, two stages of a bi-directional counter or bi-directional shift register are formed.
Up to 9 extra trigger gates can be paralleled to one flip-flop.
The circuit is mounted inside a sealed metal can with 19 wire terminals.

| | | |
|---|---|---|
| Ambient temperature range: | | |
| | operating | -25 to +55 °C<br>below 0 °C: derated output data |
| | storage | -55 °C to +75 °C |
| Weight | | approx. 40 g |
| Case | | high standard case |



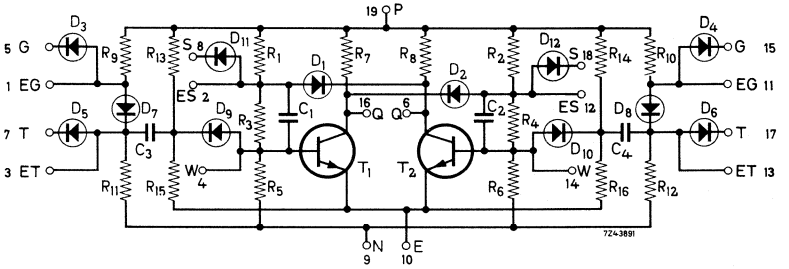

terminal location




drawing symbol

## CIRCUIT DATA

Terminal
1 = EG = extension gate input
2 = ES = extension set/reset input
3 = ET = extension trigger input
4 = W = extension trigger gate
5 = G = gate input
6 = Q = output
7 = T = trigger-input
8 = S = set/reset input
9 = N = supply - 12 V
10 = E = common supply 0 V
11 = EG = extension gate input
12 = ES = extension set/reset input
13 = ET = extension trigger input
14 = W = extension trigger gate
15 = G = gate input
16 = Q = output
17 = T = trigger input
18 = S = set/reset input
19 = P = supply + 12 V




Power supply

Terminal 9 : $V_N$ = -12 V ±5 %, $-I_N$ = 1.1 mA
10 : $V_E$ = 0 V common
19 : $V_P$ = +12 V ±5 %, $I_P$ = 7.0 mA
} nominal value of the current

INPUT REQUIREMENTS (at $V_P$ = 11.4 V and $V_N$ = -12.6 V unless specified differently).

Set/reset input (S-terminals)

A d.c. voltage level is applied to terminal S . A "positive low" voltage (between 0 V and 0.3 V) drives the corresponding transistor into the non-conducting state.

Transistor conducting (output level "positive low").

Voltage $V_S$ = min. 2/3 $V_P$
= max. $V_P$

Type of diodes and maximum number connected in parallel at terminal ES:
3 x OA 85/OA 95

Transistor non-conducting (output level "positive high")

| | | |
|---|---|---|
| Voltage | $V_S$ = min. 0 V<br>= max. 0.3 V | |
| Required direct current | $-I_{SD}$ = max. 1.95 mA | |
| Required transient charge, when $V_S$ changes from 2/3 Vp to 0.5 V in 1.5 µs | $-Q_{ST}$ = max. 2.8 nC | |

Time data

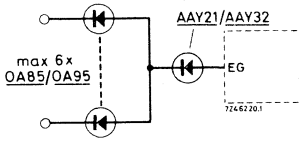
| | | |
|---|---|---|
| pulse duration<br>recovery time | $t_p$ = min. 2 µs<br>$t_{rec}$ = min. 15 µs | See point 4* |
| Time delay between S- and T-signal | $t_{st}$ = min. 15 µs | See point 5* |

Gate-input (G-terminals)

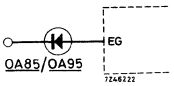
A d.c. voltage level is applied to terminal G. A "positive low" voltage closes the gate, whilst a "positive high" voltage (between 2/3 Vp and Vp) opens the gate.

Gate open

| | |
|---|---|
| Voltage | $V_G$ = min. 2/3 Vp<br>= max. $V_P$ |




Gate extension input EG: max number of parallel input diodes: 6 x OA85/OA95




Gate extension input EG: with only one input diode at EG

Gate closed

| | |
|---|---|
| Voltage | $V_G$ = min. 0 V<br>= max. 0.3 V |
| Required direct current | $-I_{GD}$ = max. 1.1 mA |

*Of section "Time definitions 10-series circuit blocks".

| | | | |
|---|---|---|---|
| Required transient charge, when $V_G$ changes from 2/3 $V_P$ to 0.5 V in 1.5 µs | $-Q_{GT}$ | = max. 1.2 nC | |
| Time data | | | |
| Trigger gate setting time | $t_{gs}$ | = min. 29 µs | See point 6* |
| Trigger gate inhibiting time | $t_{gi}$ | = min. 29 µs | See point 7* |

Trigger input (T-terminals).

A negative-going voltage step is applied to the terminals T separately or to both terminals interconnected in the case of binary divider applications. This voltage step on terminal T drives the transistor into the non-conducting state if the corresponding gate has been opened by the appropriate input signal on terminal G.

| | | Gate open | Gate closed |
|---|---|---|---|
| | $V_G$ | = min. 2/3 $V_P$<br>= max. $V_P$ | = min. 0 V<br>= max. 0.3 V |
| Required direct current when $V_T$ = max. 0.3 V | $-I_{TD}$ | = max. 1.1 mA | 0 mA |
| Required transient charge when $V_T$ changes from 2/3 $V_P$ to 0.5 V in 1.5 µs | | Gate open | Gate closed |
| | $-Q_{TT}$ | = max. 3.4 nC | 0 nC |
| Input noise level | $V_n$ | = max. 1.2 V peak to peak | |

Recommended type of diodes and maximum number connected in parallel at terminal ET: 6 x BAY 38

| Time data | | | |
|---|---|---|---|
| Fall time | $t_f$ | = max. 1.5 µs | |
| Pulse duration | $t_p$ | = min. 2 µs | See point 3* |
| Trigger gate setting time | $t_{gs}$ | = min. 29 µs | |
| Time delay between T- and S-signals | $t_{ts}$ | = min. 15 µs | See point 5* |

Base input (W-terminal)

Capacitance (wiring + output TG13/TG14/TG15): $C_W$ = max. 95 pF

* Of section "Time definitions 10-series circuit blocks".

OUTPUT DATA (At $V_P$ = 11.4 V and $V_N$ = -12.6 V, unless specified differently).

Voltages, direct currents and transient charges

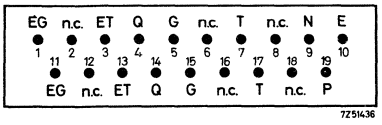
| | | | |
|---|---|---|---|
| Transistor conducting | (output level "positive low") | | |
| Voltage | $V_Q$ | = min. 0 V<br>= max. 0.3 V | |
| Available direct current | $I_{QD}$ | = min. 8.2 mA<br>= min. 6.6 mA ($T_{amb}$ = min. - 25 °C) ** | |
| Available transient charge, when $V_Q$ changes from 2/3 $V_P$ to 0.5 V in 1.5 µs | $Q_{TT}$ | = min. 27 nC<br>= min. 22 nC ($T_{amb}$ = min. - 25 °C) ** | |
| Time data | | | |
| Fall time | $t_f$ | = max. 1.5 µs | See point 1* |
| Fall delay | $t_{fd}$ | = max. 2 µs | See point 2* |
| Transistor non-conducting | (output level "positive high") | | |
| Voltage | $V_Q$ | = min. 2/3 $V_P$<br>= max. $V_P$ | |
| Maximum wiring capacitance | 200 pF | | |

* Of section "Time definitions 10-series circuit blocks".
** Between 0 and - 25 °C to be derived by linear interpolation.

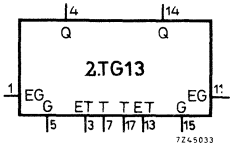
# DUAL TRIGGER GATE

The unit comprises two identical trigger gate circuits, which are normally used in conjunction with flip-flop units FF 10, FF 11 and FF 12.
With the dual trigger gate a second-pair of trigger inputs are formed for the flip-flops FF 11 and FF 12, to make one stage of a bi-directional counter or shift register.
In these applications the 2TG13 output Q-terminals are to be connected directly to the flip-flop W-terminals.
The trigger gates are controlled by a d.c. voltage level, applied to the G-terminals.
The number of gate (G) inputs or trigger (T) inputs can be extended with the aid of external diodes at the extension inputs EG or ET.
The circuit is mounted inside a sealed metal can with 19 wire terminals.

| | | |
|---|---|---|
| Ambient temperature range: | | |
| | operating | -25 to +55 °C |
| | storage | -55 to +75 °C |
| Weight | | approx. 30 g |
| Case | | low standard case |



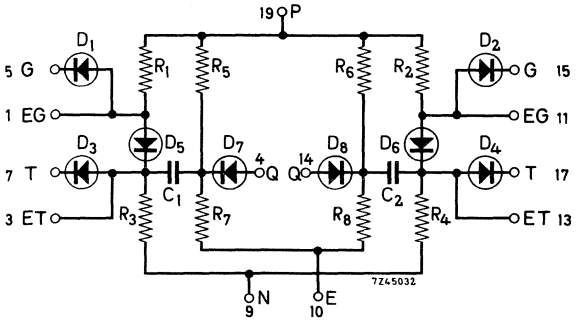

terminal location




drawing symbol

CIRCUIT DATA

Terminal
1 = EG = extension gate input
2 = not connected
3 = ET = extension trigger input
4 = Q = output
5 = G = gate input
6 = not connected
7 = T = trigger input
8 = not connected
9 = N = supply −12 V
10 = E = common supply 0 V
11 = EG = extension gate input
12 = not connected
13 = ET = extension trigger input
14 = Q = output
15 = G = gate input
16 = not connected
17 = T = trigger input
18 = not connected
19 = P = supply +12 V




Power supply

Terminal 9 : $V_N$ = −12 V ±5%, $-I_N$ = 0.5 mA
10 : $V_E$ = 0 V common
19 : $V_P$ = +12 V ±5%, $I_P$ = 2.2 mA
} nominal value of the current

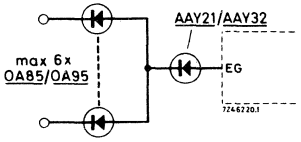
INPUT REQUIREMENTS (at $V_P$ = 11.4 V and $V_N$ = −12.6 V unless specified differently).

Gate input (G-terminals)

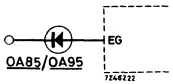
A d.c. voltage level is applied to terminal G. A "positive low" voltage closes the gate, whilst a "positive high" voltage opens the gate.

Gate open

Voltage $V_G$ = min. 2/3 $V_P$
= max. $V_P$




Gate extension input EG: max number of parallel input diodes: 6 x OA85/OA95




Gate extension input EG: with only one input diode at EG

Gate closed

| | | |
|---|---|---|
| Voltage | $V_G$ | = min. 0 V<br>= max. 0.3 V |
| Required direct current | $-I_{GD}$ | = max. 1.1 mA |
| Required transient charge when $V_G$ changes from 2/3 $V_P$ to 0.5 V in 1.5 µs | $-Q_{GT}$ | = max. 1.2 nC |

Time data

| | | | |
|---|---|---|---|
| Trigger gate setting time | $t_{gs}$ | = min. 29 µs | See point 6 * |
| Trigger gate inhibiting time | $t_{gi}$ | = min. 29 µs | See point 7 * |

Trigger input (T-terminals)

A negative-going voltage step is applied to the terminals T separately or to both terminals interconnected.
This voltage step on terminal T passes the trigger gate if it has been opened by an appropriate input signal on terminal G.

| | | Gate open | Gate closed |
|---|---|---|---|
| | $V_G$ | = min. 2/3 $V_P$<br>= max. $V_P$ | = min. 0V<br>= max. 0.3V |
| Required direct current when $V_T$ = max. 0.3V | $-I_{TD}$ | = max. 1.1 mA | 0 mA |
| Required transient charge when $V_T$ changes from 2/3 $V_P$ to 0.5 V in 1.5 µs | $-Q_{TT}$ | = max. 3.4 nC | 0 nC |

*) Of section "Time definitions 10-series circuit blocks".

| | | |
|---|---|---|
| Input noise level | $V_n$ = max. 1.2 V peak to peak | |
| | Recommended type of diodes and maximum number connected in parallel at terminal ET: 6 x BAY 38 | |

Time data

| | | |
|---|---|---|
| Fall time | $t_f$ = max. 1.5 µs | * |
| Pulse duration | $t_p$ = min. 2 µs | See point 3 |
| Trigger gate setting time | $t_{gs}$ = min. 29 µs | |

OUTPUT DATA

When the 2TG13 is used in conjunction with flip-flops FF 10, FF 11 and FF 12, the Q-output terminals are directly connected to the W-terminals of the flip-flop.

Output capacitance: $C_o$ max. 5 pF

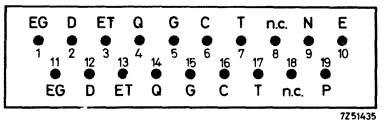
* Of section "Time definitions 10-series circuit blocks".

# DUAL TRIGGER GATE

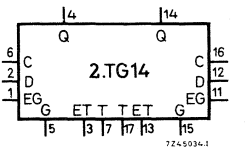
The unit comprises two identical trigger gate circuits, which are normally used in conjunction with flip-flop units FF 10, FF 11 and FF 12.
With the dual trigger gate a second pair of trigger inputs are formed for the flip-flops FF 11 and FF 12, to make one stage of a bi-directional counter or shift register. In these applications the 2TG 14 output Q-terminals are to be connected directly to the flip-flop W-terminals.
The trigger gates are controlled by a d.c. voltage level applied to the G-terminals.
Two separate built-in diodes can be used to extend the number of gate (G) inputs on any of the extension inputs EG.

The circuit is mounted inside a sealed metal can with 19 wire terminals.

| | | |
|---|---|---|
| Ambient temperature range: | | |
| | operating | - 25 to + 55 °C |
| | storage | - 55 to + 75 °C |
| Weight | | approx. 30 g |
| Case | | low standard case |




terminal location

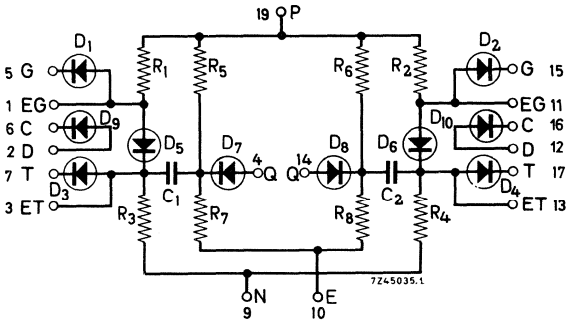



drawing symbol

## CIRCUIT DATA

Terminal

1 = EG = extension gate input
2 = D = anode separate diode
3 = ET = extension trigger input
4 = Q = output
5 = G = gate input
6 = C = cathode separate diode
7 = T = trigger input
8 = not connected
9 = N = supply −12 V
10 = E = common supply 0 V
11 = EG = extension gate input
12 = D = anode separate diode
13 = ET = extension trigger input
14 = Q = output
15 = G = gate input
16 = C = cathode separate diode
17 = T = trigger input
18 = not connected
19 = P = supply +12 V




Power supply

Terminal 9 : $V_N$ = −12 V ±5%, $-I_N$ = 0.5 mA
10 : $V_E$ = 0 V common
19 : $V_P$ = +12 V ±5%, $I_P$ = 2.2 mA
} nominal value of the current

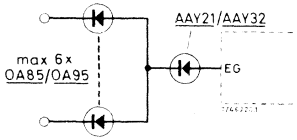
INPUT REQUIREMENTS (at $V_P$ = 11.4 V and $V_N$ = −12.6 V unless specified differently).

Gate input (G-terminals)

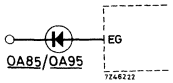
A d.c. voltage level is applied to terminal G. A "positive low" voltage closes the gate, whilst a "positive high" voltage opens the gate.

Gate open

Voltage $V_G$ = min. 2/3 $V_P$
= max. $V_P$




Gate extension input EG: max number of parallel input diodes: 6 x OA85/OA95




Gate extension input EG: with only one input diode at EG

Gate closed

| | | |
|---|---|---|
| Voltage | $V_G$ | = min. 0 V<br>= max. 0.3 V |
| Total required direct current | $-I_{GD}$ | = max. 1.1 mA |
| Total required transient charge, when $V_G$ changes from 2/3Vp to 0.5V in 1.5 µs | $-Q_{GT}$ | = max. 1.2 nC |

Time data

| | | | |
|---|---|---|---|
| Trigger gate setting time | $t_{gs}$ | = min 29 µs | See point 6* |
| Trigger gate inhibiting time | $t_{gi}$ | = min 29 µs | See point 7* |

Trigger-input (T-terminals)

A negative-going voltage step is applied to the terminals T separately or to both terminals interconnected. This voltage step on terminal T passes the trigger gate if it has been opened by an appropriate input signal on terminal G.

| | | Gate open | Gate closed |
|---|---|---|---|
| | $V_G$ | = min 2/3Vp<br>= max Vp | = min. 0 V<br>= max. 0.3V |
| Required direct current when $V_T$ = max. 0.3V | $-I_{TD}$ | = max 1.1mA | 0 mA |
| Required transient charge when $V_T$ changes from 2/3Vp to 0.5V in 1.5 µs | $-Q_{TT}$ | = max 3.4nC | 0 nC |

* Of section "Time definitions 10-series circuit blocks".

| | | | |
|---|---|---|---|
| Input noise level | $V_n$ | = max 1.2 V peak to peak | |
| | Recommended type of diodes and maximum number connected in parallel at terminal ET: 6 x BAY 38 | | |

Time data

| | | | |
|---|---|---|---|
| Fall time | $t_f$ | = max 1.5 µs | See point 3* |
| Pulse duration | $t_p$ | = min 2 µs | |
| Trigger gate setting time | $t_{gs}$ | = min 29 µs | |

OUTPUT DATA

When the 2TG14 is used in conjunction with flip-flops FF 10, FF 11 and FF12, the Q-output terminals are directly connected to the W-terminals of the flip-flop.

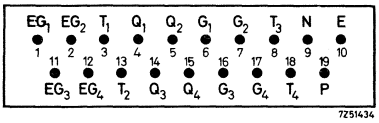
Output capacitance: $C_o$ = max. 5 pF

* Of section "Time definitions 10-series circuit blocks".

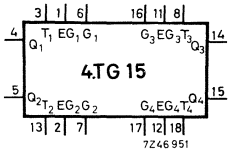
# QUADRUPLE TRIGGER GATE

The unit comprises four separate identical trigger gate circuits, which are normally used in conjunction with flip-flop units FF 10, FF 11 and FF 12.
By connecting the output Q-terminals of the 4TG 15 directly to the appropriate W-terminals of a flip-flop FF 10 one stage of a bi-directional counter or bi-directional shift register is formed.
When, however, the Q-terminals of one 4TG 15 are connected to the appropriate W-terminals of two units FF 11 or FF 12, two stages of a bi-directional counter or bi-directional shift register are formed.
The trigger gates are controlled by a d.c. voltage level, applied to the G-terminals.
The number of gate (G) inputs can be extended with the aid of external diodes at the extension inputs EG.
The circuit is mounted inside a sealed metal can with 19 wire terminals.

| | | |
|---|---|---|
| Ambient temperature range: | | |
| | operating | - 25 to + 55 °C |
| | storage | - 55 to + 75 °C |
| Weight | | approx. 40 g |
| Case | | high standard case |




terminal location

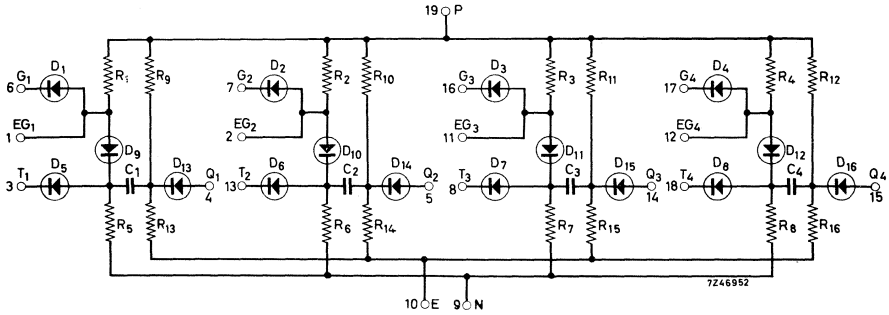



drawing symbol

## CIRCUIT DATA

Terminal

1 = $EG_1$ = extension gate input
2 = $EG_2$ = extension gate input
3 = $T_1$ = trigger input
4 = $Q_1$ = output
5 = $Q_2$ = output
6 = $G_1$ = gate input
7 = $G_2$ = gate input
8 = $T_3$ = trigger input
9 = N = supply - 12V
10 = E = common supply 0V
11 = $EG_3$ = extension gate input
12 = $EG_4$ = extension gate input
13 = $T_2$ = trigger input
14 = $Q_3$ = output
15 = $Q_4$ = output
16 = $G_3$ = gate input
17 = $G_4$ = gate input
18 = $T_4$ = trigger input
19 = P = supply + 12V




Power supply

Terminal 9: $V_N = -12V \pm 5\%$, $-I_N = 1.0mA$ } nominal value
10: $V_E = 0V$ common } of the current
19: $V_P = +12V \pm 5\%$, $I_P = 4.4mA$ }

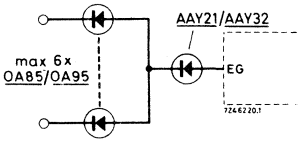
## INPUT REQUIREMENTS (at $V_P = 11.4V$ and $V_N = -12.6V$ unless specified differently)

Gate inputs (G-terminals)

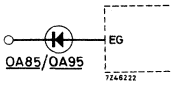
A d.c. voltage level is applied to terminal G. A "positive low" voltage closes the gate, whilst a "positive high" voltage opens the gate.

Gate open

Voltage $V_G$ = min. 2/3 $V_P$
= max. $V_P$




Gate extension input EG: max. number of parallel input diodes: 6 x OA85/OA95




Gate extension input EG: with only one input diode at EG.

Gate closed

Voltage $V_G$ = min. 0 V
= max. 0.3 V

Required direct current $-I_{GD}$ = max. 1.1 mA.

Required transient charge when $V_G$ changes from 2/3 Vp to 0.5 V in 1.5 µs $-Q_{GT}$ = max. 1.2 nC

Time data

Trigger gate setting time $t_{gs}$ = min. 29 µs See point 6 *
Trigger gate inhibiting time $t_{gi}$ = min. 29 µs See point 7 *

Trigger input (T-terminals)

A negative-going voltage step is applied to the terminals T separately or to both terminals interconnected.
This voltage step on terminal T passes the trigger gate if it has been opened by an appropriate input signal on terminal G.

| | Gate open | Gate closed |
|---|---|---|
| | $V_G$ = min. 2/3 $V_p$ | = min. 0 V |
| | = max. $V_p$ | = max. 0.3 V |
| Required direct current when $V_T$ = max. 0.3 V | $-I_{TD}$ = max. 1.1 mA | 0 mA |
| Required transient charge when $V_T$ changes from 2/3 Vp to 0.5 V in 1.5 µs | $-Q_{TT}$ = max. 3.4 nC | 0 nC |
| Input noise level | $V_n$ = max. 1.2 V peak to peak | |

* Of section "Time definitions 10-series circuit blocks".

Time data

| | | | |
|---|---|---|---|
| Fall time | $t_f$ | = max. 1.5 µs | See point 3 * |
| Pulse duration | $t_p$ | = min. 2.0 µs | |
| Trigger gate setting time | $t_{gs}$ | = min. 29 µs | |

OUTPUT DATA

When the 4TG 15 is used in conjunction with flip-flops FF 10, FF 11 and FF 12, the Q-output terminals are directly connected to the W-terminals of the flip-flop.

Output capacitance: $C_o$ = max. 5 pF

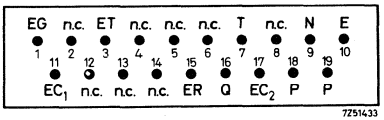
* Of section "Time definitions 10-series circuit blocks".

# TIMER UNIT

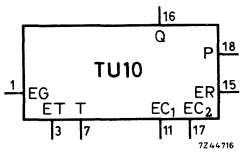
The unit TU10 contains a timing circuit followed by a Schmitt trigger circuit and an inverting amplifier. This unit comprises a built-in trigger gate as well. The trigger gate can be controlled by a d.c. voltage level applied via an external diode to terminal EG.
The number of the trigger (T) inputs can be extended with the aid of external diodes at the extension input ET.
When a negative-going voltage step is applied to terminal T, the circuit generates a positive-going pulse at the output Q -terminal, provided the gate is open. The duration of the output pulse is determined by the values of the external capacitor to be connected between the terminals $EC_1$ and $EC_2$ and the external resistor between the terminals ER and P.

The terminals ER and P must be interconnected when no external resistor is used.
The circuit is mounted inside a sealed metal can with 19 wire terminals.

| | | |
|---|---|---|
| Ambient temperature range: | | |
| | operating | -25 to +55 °C<br>below 0 °C: derated output data. |
| | storage | -55 °C to +75 °C |
| Weight | | approx. 40g |
| Case | | high standard case |

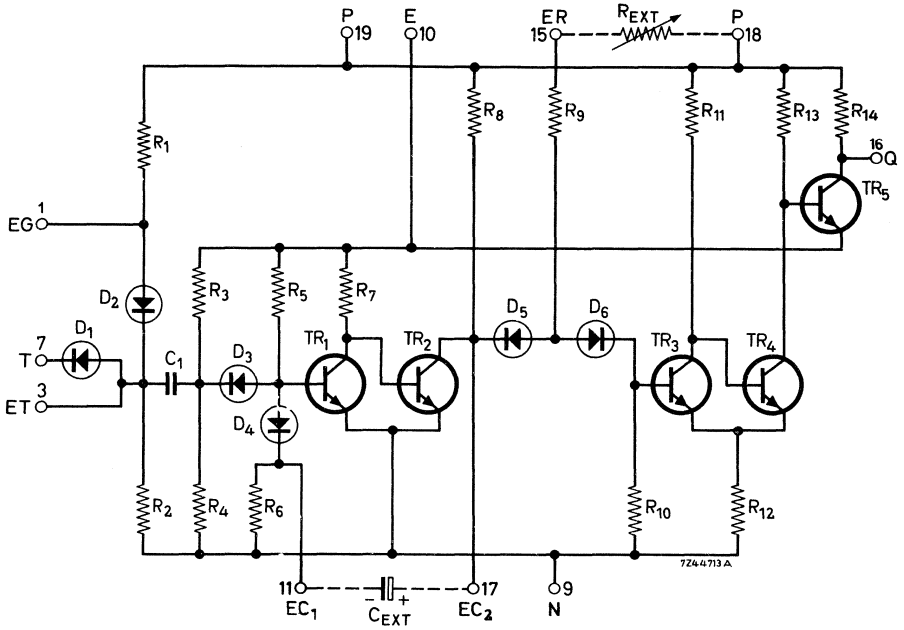



terminal location




drawing symbol

## CIRCUIT DATA




Terminal

1 = EG = extension gate input
2 = not connected
3 = ET = extension trigger input
4 = not connected
5 = not connected
6 = not connected
7 = T = trigger input
8 = not connected
9 = N = supply - 12 V
10 = E = common supply 0 V
11 = $EC_1$ = for external capacitor(-side)
12 = not connected
13 = not connected
14 = not connected
15 = ER = for external resistor
16 = Q = output
17 = $EC_2$ = for external capacitor (+side)
18 = P = supply + 12V (internally connected to terminal 19)
19 = P = supply + 12V

Power supply

Terminal 9: $V_N$ = - 12V ± 5%, - $I_N$ = 9.5mA
10: $V_E$ = 0V common
19: $V_P$ = + 12V ± 5%, $I_P$ = 5.0 mA
} nominal value of the current

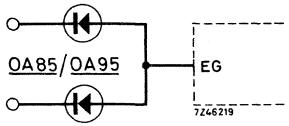
INPUT REQUIREMENTS (at $V_P$ = 11.4V and $V_N$ = - 12.6V unless specified differently).

Gate input (EG-terminal)

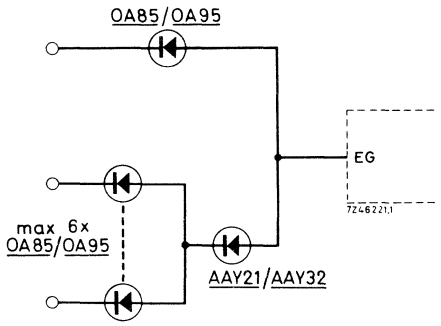
A d.c. voltage level is applied to terminal EG via an external diode. A "positive low" voltage closes the gate, whilst a "positive high" voltage opens the gate.

Gate open

Voltage $V_G$ = min. 2/3 $V_P$
= max. $V_P$




Gate extension input EG: with two input diodes




Gate extension input EG: max number of parallel input diodes:
7 x OA85/OA95/AAY21/AAY32

Gate closed

Voltage $V_G$ = min. 0V
= max. 0.3V

Required direct current $-I_{GD}$ = max. 1.1 mA

Required transient charge when $V_G$ changes from 2/3 $V_P$ to 0.5V in 1.5 µs $-Q_{GT}$ = max. 1.2 nC

Time data

Trigger gate setting time $t_{gs}$ = min. 26 µs see point 6*

Trigger gate inhibiting time $t_{gi}$ = min. 26 µs see point 7*

Trigger input (T-terminal)

A negative-going voltage step is applied to terminal T. This voltage step on terminal T passes the gate, when it has been opened by the appropriate voltage level on terminal EG and transistor TR5 is driven in the non-conducting state.

* Of section "Time definitions 10-series circuit blocks".

| | Gate open | Gate closed |
|---|---|---|
| Voltage | $V_G$ = min. 2/3 $V_P$ = max. $V_P$ | = min. 0 V = max. 0.3V |
| Required direct current | $-I_{TD}$ = max. 1.1 mA | = 0 mA |
| Required transient charge when $V_T$ changes from 2/3$V_P$ to 0.5V in 1.5 µs | $-Q_{TT}$ = max. 3.2 nC | 0 nC |

Recommended type of diodes and maximum number connected in parallel at terminal ET: 6 x BAY 38/BAX 13

Time data : see par. "Delay and swiching times" below

Input noise level $V_n$ = max. 1.2 V peak to peak

OUTPUT DATA (at $V_P$ = 11.4V and $V_N$ = - 12.6V unless specified differently).

Transistor TR5 conducting

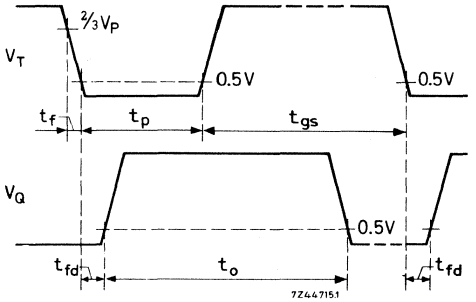
Voltage $V_Q$ = min . 0V = max. 0.3V

Available direct current $I_{QD}$ = min. 32 mA = min. 29 mA ($T_{amb}$ = min. - 25 °C)**

Available transient charge when $V_Q$ changes from 2/3$V_P$ to 0.5V in 1.5 µs $Q_{QT}$ = min. 30 nC = min. 27 nC ($T_{amb}$ = min. - 25 °C)**

Maximum wiring capacitance 200 pF

Delays and switching times




** Between 0 and - 25 °C to be derived by linear interpolation.

fall time $t_f$ = max. 1.5 µs
fall delay $t_{fd}$ = max. 2 µs
input pulse duration $t_p$ = min. 2 µs
output pulse duration $t_o$ = depends on the values of the external capacitor $C_{ext}$ and the external resistor $R_{ext}$.

- The minimum time between two successive input pulses is only determined by the trigger gate setting time ($t_{gs}$).
- Besides the above mentioned restriction no recovery time of the unit has to be taken into account.
- When during the delay the input is triggered for a second time, the delay action will start all over again.

Duration of the output pulse : dependent on the values of $R_{ext}$ and $C_{ext}$

| | Increase of the duration with external capacitor $C_{ext}$ *) |
|---|---|
| $R_{ext}$ = 47 kΩ ± 10% | 44 - 79 ms/µF |
| terminals ER and P interconnected | 23 - 35 ms/µF |

The absolute max.values: $R_{ext}$ = 52 kΩ and $C_{ext}$ = 1800 µF.
By means of this resistor the output pulse duration can be varied by a factor 2. The terminals ER and P must be interconnected, if no external resistor is used.

Stability of the output pulse duration (for orientation only)

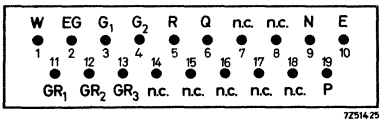
A variation of the supply voltages $V_N$ and $V_P$ of ± 5% varies the pulse duration by less than ± 1.5% with $R_{ext.}$ = 52 kΩ and ± 0.6% with $R_{ext.}$ = 0
A variation in ambient temperature of 1 °C varies the pulse duration by less than 0.1%.
A variation of the leakage current of the external capacitor ($C_{ext}$) with 1µA varies the pulse duration by less than 0.8%.

* The maximum leakage current of the external capacitor must be less than 20 µA. The working voltage of the external capacitor must be > 25 V.

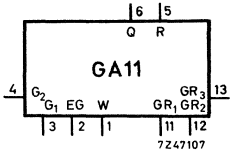
# GATE AMPLIFIER

The unit contains a gate circuit and a non-inverting amplifier. The two amplifier stages give an appreciable power amplification between input and output.
The amplifier of the unit GA 11 can be preceded by one-level as well as two level logic circuits, performing an AND respectively an AND-AND or AND-OR operation for "positive high" signals.
Three resistors of 10 kΩ have been mounted inside the block, possibly needed for the AND-OR operation.
The collector resistor R of the output stage can be left floating for driving e.g. inductive loads. In this case the available output current is increased, and less $I_p$ is drawn from the stabilised $V_p$.
The circuit is mounted inside a sealed metal can with 19 wire terminals.

| | | |
|---|---|---|
| Ambient temperature range: | | |
| | operating | - 25 to + 55 °C |
| | storage | - 55 to + 75 °C |
| Weight | | approx. 30 g |
| Case | | low standard case |




terminal location

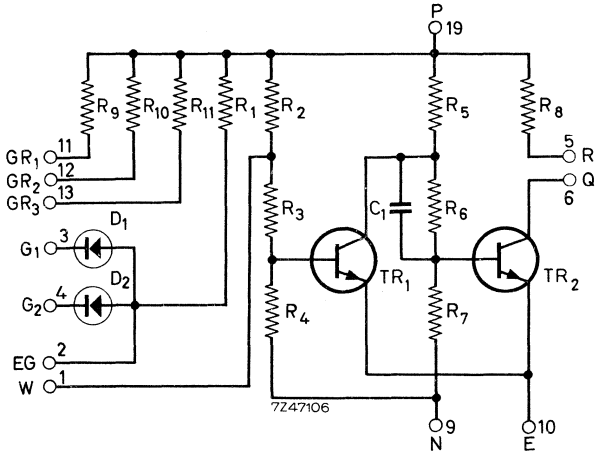



drawing symbol

## CIRCUIT DATA

Terminal

1 = W = input amplifier
2 = EG = extension gate input
3 = $G_1$ = gate input
4 = $G_2$ = gate input
5 = R = connection collector resistor
6 = Q = output
7 = not connected
8 = not connected
9 = N = supply - 12V
10 = E = common supply 0V
11 = $GR_1$ = connection gate resistor
12 = $GR_2$ = connection gate resistor
13 = $GR_3$ = connection gate resistor
14 = not connected
15 = not connected
16 = not connected
17 = not connected
18 = not connected
19 = P = supply +12V




Power supply

Terminal 9: $V_N$ = - 12V ± 5% $-I_N$ = 1.5mA
10: $V_E$ = 0V common
19: $V_P$ = +12V ± 5% $I_P$ = 15mA (Q and R interconnected)
$I_P$ = 6mA (Q and R not interconnected)
nominal value of the current

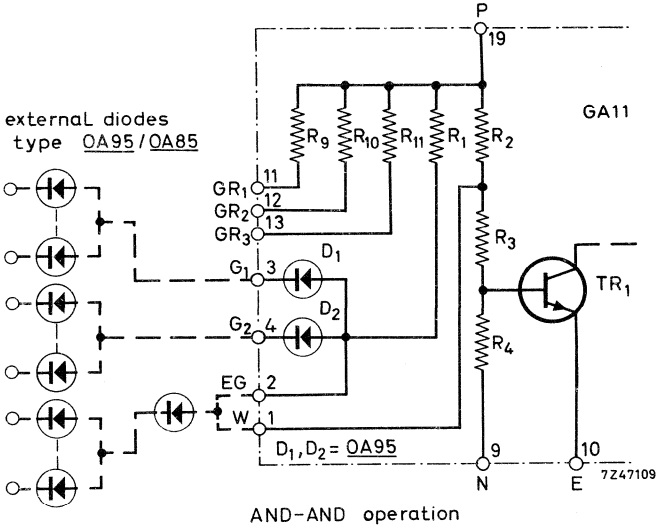
INPUT REQUIREMENTS (at $V_P$ = 11.4V and $V_N$ = - 12.6V unless specified differently)

Input (G, EG and W-terminals)

The three logic circuit configurations, which can be performed and connected to the input terminals are:

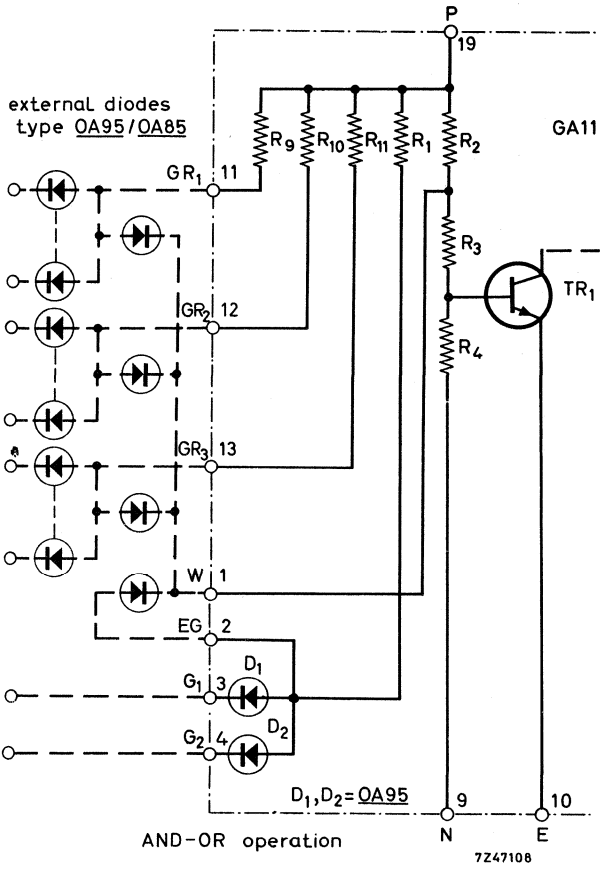
1 A one-level logic circuit, performing an AND operation for "positive high" signals and preceding the amplifier circuit, can be obtained by interconnecting the EG and W terminals.

2 A two-level logic circuit, performing an AND-AND operation and preceding the amplifier circuit, can be obtained by connecting the external diodes as shown in the diagram below.
When all inputs of all gate circuits are at a "positive high" level, transistor $TR_1$ is conducting and consequently transistor $TR_2$ is non-conducting. So the output level is at "positive high" voltage as well.




AND-AND operation

3 A two-level logic circuit, performing an AND-OR operation and preceding the amplifier can be obtained by connecting the external diodes as shown in the diagram below.
When all inputs of only one gate circuit are at "positive high" level, transistor $TR_1$ is conducting and consequently transistor $TR_2$ is non-conducting. So the output level is at "positive high" voltage as well.




In the above mentioned three cases the voltages and currents are as follows:

Transistor TR2 conducting (output level "positive low")

| | |
|---|---|
| Voltage | $V_W$ = max. 1.5 V |
| Required direct current | $-I_{GD}$ = max. 1.1 mA |
| Required transient charge when $V_Q$ changes from 2/3 $V_P$ to 0.5 V in 1.5 µs | $-Q_{GT}$ = max. 1.2 nC |

Transistor TR2 non-conducting (output level "positive high")

| | |
|---|---|
| Voltage | $V_W$ = min. 3.25 V |

OUTPUT DATA (at $V_P$ = 11.4 V and $V_N$ = - 12.6 V unless specified differently)

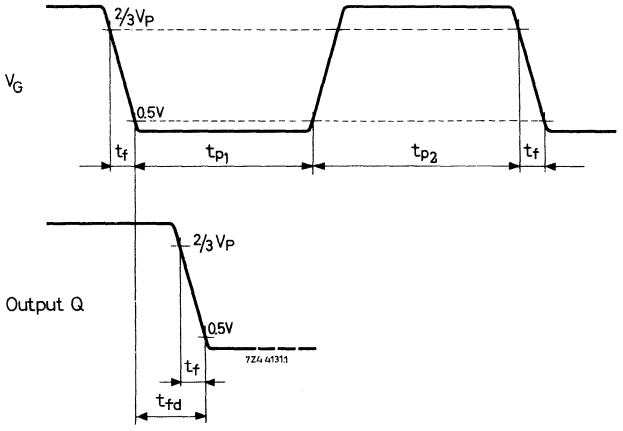
Transistor TR2 conducting (output level "positive low")

| | | |
|---|---|---|
| Voltage | $V_Q$ | = min. 0 V<br>= max. 0.3 V |
| Available direct current | $I_{QD}$ | = min. 62 mA (Q and R interconnected)<br>= min. 71 mA (Q and R not interconnected) * |
| Available transient charge when $V_Q$ changes from 2/3 $V_P$ to 0.5 V in 1.5 µs | $Q_{QT}$ | = min. 75 nC (Q and R interconnected)<br>= min. 80 nC (Q and R not interconnected) |

Transistor TR2 non-conducting

| | | |
|---|---|---|
| Voltage | $V_Q$ | = absolute max. 15 V |
| Maximum wiring capacitance | | 1000 pF |

Delays and switching times




Pulse duration: $t_{p1}$ = min. 6 µs
$t_{p2}$ = min. 6 µs

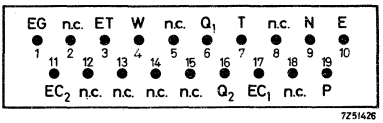
Fall delay : $t_{fd}$ = max. 3 µs (at $t_f$ = max. 1.5 µs)

* When inductive loads are switched, the output transistor must be protected against voltage transients by means of a diode, mounted across the load, the anode connected to the Q-output terminal. Recommended type of diode: BY100.

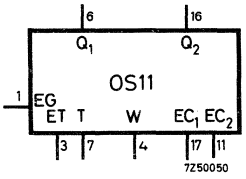
# ONE-SHOT MULTIVIBRATOR

The unit OS 11 contains a monostable multivibrator circuit and a trigger gate. The trigger gate can be controlled by a d.c. voltage level, applied via an external diode, to terminal EG. The number of the trigger (T)-inputs can be extended with the aid of external diodes at the extension input ET.
With the aid of the trigger gates 2. TG 13, 2. TG 14 and 4. TG 15 extra triggering facilities can be made by connecting their Q-outputs to the W-input of the one-shot multivibrator.
When a negative-going voltage step is applied to terminal T, the circuit generates a pulse at the output(Q)-terminals, provided the gate is open. The duration of the output pulse can be increased by an external capacitor to be connected between the terminals $EC_1$ and $EC_2$.
The circuit is mounted inside a sealed metal can with 19 wire terminals.

| | | |
|---|---|---|
| Ambient temperature range: | | |
| | operating | - 25 to + 55 °C<br>below 0 °C: derated output data |
| | storage | - 55 °C to + 75 °C |
| Weight | | approx. 40g |
| Case | | high standard case |




terminal location

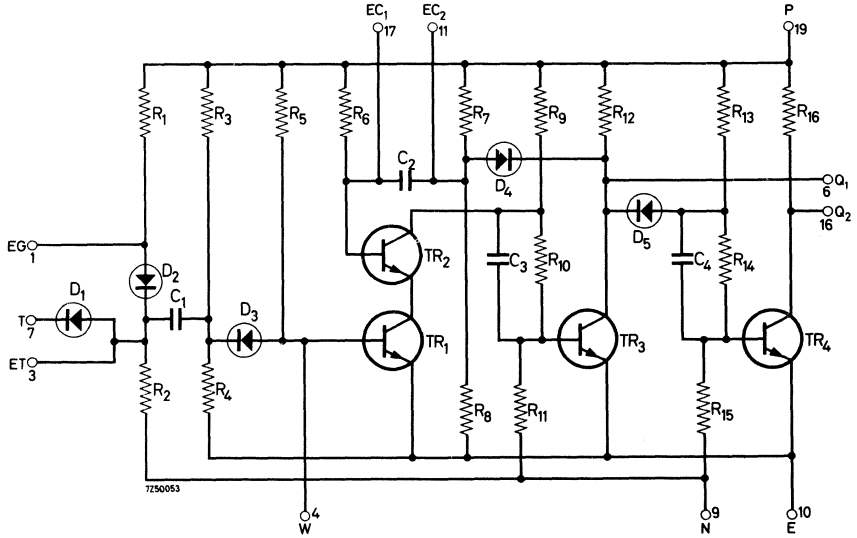



drawing symbol

CIRCUIT DATA

Terminal

1 = EG = extension gate input
2 = not connected
3 = ET = extension trigger input
4 = W = extension trigger gate
5 = not connected
6 = $Q_1$ = output 1
7 = T = trigger input
8 = not connected
9 = N = supply −12 V
10 = E = common supply 0 V
11 = $EC_2$ = for external capacitor
12 = not connected
13 = not connected
14 = not connected
15 = not connected
16 = $Q_2$ = output 2
17 = $EC_1$ = for external capacitor
18 = not connected
19 = P = supply +12 V




Power supply

Terminal 9 : $V_N$ = −12 V ±5 %, $-I_N$ = 1 mA
10 : $V_E$ = 0 V common
19 : $V_P$ = +12 V ±5 %, $I_P$ = 6 mA

} nominal value of the current

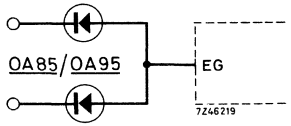
INPUT REQUIREMENTS (at $V_P$ = 11.4 V and $V_N$ = -12.6 V unless specified differently).

Gate input (EG-terminals)

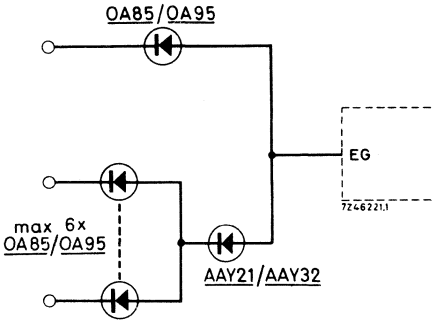
A d.c. voltage level is applied to terminal EG via an external diode.
A "positive low" voltage closes the gate, whilst a "positive high" voltage opens the gate.

Gate open

Voltage $V_G$ = min. 2/3 $V_P$
= max. $V_P$




Gate extension input EG: with two input diodes




Gate extension input EG: max. number of parallel input diodes: 7xOA85/OA95

Gate closed

| | | |
|---|---|---|
| Voltage | $V_G$ | = min. 0 V<br>= max. 0.3 V |
| Required direct current | $-I_{GD}$ | = max. 1.1 mA |
| Required transient charge when $V_G$ changes from 2/3 $V_P$ to 0.5 V in 1.5 µs | $-Q_{GT}$ | = max. 1.2 nC |

Time data

| | | | | |
|---|---|---|---|---|
| Trigger gate setting time | $t_{gs}$ | = min | 20 µs | See point 6* |
| Trigger gate inhibiting time | $t_{gi}$ | = min | 20 µs | See point 7* |

Trigger input (T-terminal)

A negative-going voltage step is applied to terminal T. This voltage step on terminal T passes the gate, when it has been opened by the appropriate voltage level on terminal EG, and drives transistor $TR_3$ in the conducting state and transistor $TR_4$ in the non-conducting state.

*Section "Time definitions" of "Circuit blocks 10-Series".

| | Gate open | Gate closed |
|---|---|---|
| Voltage | $V_G$ = min. 2/3 $V_p$<br>= max. $V_P$ | = min 0V<br>= max 0.3V |
| Required direct current | $-I_{TD}$ = max. 1.1 mA | 0 mA |
| Required transient charge when $V_T$ changes from 2/3 $V_P$ to 0.5 V in 1.5 µs | $-Q_{TT}$ = max. 2.3 nC | 0 nC |

Recommended type of diodes and maximum number connected in parallel at terminal ET: 6 x BAY 38/BAX13

Time data: see par. "Delays and switching times", below.
Input noise level $V_n$ = max. 1.2 V peak to peak

Base-input (W-terminal)

Input capacitance max. 60 pF

Additional triggering facilities can be obtained by connecting the output of the trigger gates to terminal W of the one-shot multivibrator, e.g. 6 trigger gates may be connected in parallel to terminal W provided the total wiring capacitance $C_W$ = max. 30 pF

OUTPUT DATA (at $V_P$ = 11.4 V and $V_N$ = - 12.6 V unless specified differently)

Transistor TR3 respectively TR4 conducting

| | | |
|---|---|---|
| Voltage | $V_{Q\,1,2}$ = min. 0 V<br>= max. 0.3 V | |
| | $T_{amb}$ = min. 0 °C | $T_{amb}$ = min. - 25 °C* |
| Available direct current | | |
| output $Q_1$ | $I_{QD}$ = min. 8.6 mA | min. 5.5 mA |
| output $Q_2$ | = min. 12.8 mA | min. 9.5 mA |
| Available transient charge when $V_Q$ changes from 2/3 $V_P$ to 0.5 V in 1.5 µs | | |
| output $Q_1$ | $Q_{QT}$ = min. 24 nC | min. 17.2 nC |
| output $Q_2$ | $Q_{QT}$ = min. 29 nC | min. 22 nC |

* Between 0 and - 25 °C to be derived by linear interpolation

Maximum wiring capacitance: 200 pF

Duration of the output pulse·

| | |
|---|---|
| Intrinsic value | $t_f + t_o$ = max. 4 µs |
| Increase with external capacitor | 1 µs per 58 pF |
| Tolerance | ± 15% |

Stability of output pulse duration

An increase in ambient temperature by 1 °C gives a reduction of the pulse duration of less than 0.1 % and vice versa.

There is practically no difference in duration between different output pulses at any combination of permitted supply voltages.

An increase of the leakage current of the external capacitor ($C_{ext}$) with 1 µA decreases the pulse duration by less than 0.4 % and vice versa.

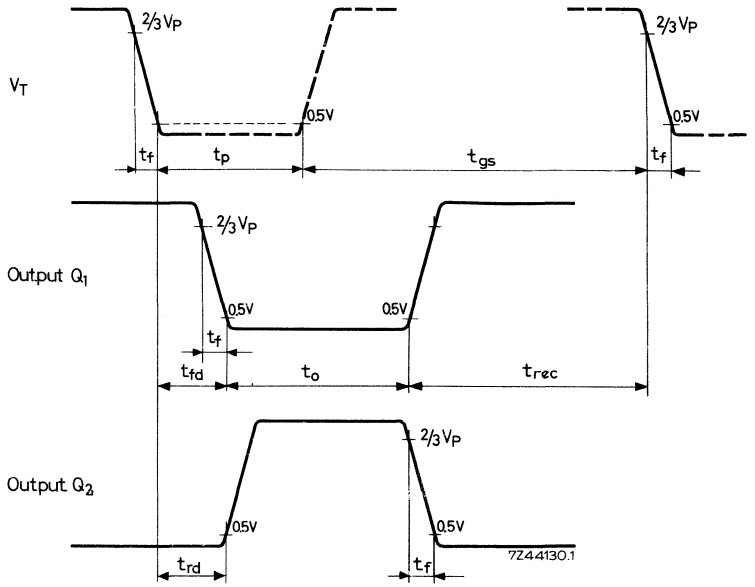
Delays and switching times

| | | |
|---|---|---|
| fall time | : $t_f$ | = max. 1.5 µs |
| fall delay | : $t_{fd}$ | = max. 2 µs |
| rise delay | : $t_{rd}$ | = max. 2 µs |
| input pulse duration | : $t_p$ | = min. 2 µs |
| output pulse duration | : $t_o$ | = depends on value of external bipolar capacitor between terminals 11 and 17. |
| recovery time | : $t_{rec}$ | = min. $t_o$ |

The minimum time between two successive input pulses is determined by two factors (see also the figure on the next page):

1) $2 \times t_o \geq t_p + t_{gs}$ : the next input pulse may start a time = $t_o$ after the trailing edge of the output pulse.

2) $2 \times t_o < t_p + t_{gs}$ : the next input pulse may start a time = $t_{gs}$ (20 µsec) after the trailing edge of the preceding input pulse.


$V_T$
2/3 $V_P$
0.5V
$t_f$
$t_p$
$t_{gs}$
Output $Q_1$
$t_{fd}$
$t_o$
$t_{rec}$
Output $Q_2$
$t_{rd}$
7Z44130.1

# PULSE DRIVER

The unit PD 11 contains a monostable multivibrator circuit and a trigger gate. The trigger gate can be controlled by a d.c. voltage level applied via an external diode to terminal EG. The number of the trigger(T) inputs can be extended with the aid of external diodes at the extension input ET.

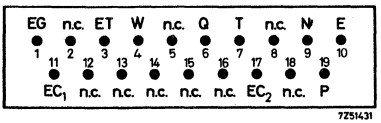
With the aid of the trigger gates 2. TG 13, 2. TG 14 and 4. TG 15 extra triggering facilities can be made by connecting their Q-outputs to the W-input of the pulse driver.

When a negative-going voltage step is applied to terminal T, the circuit generates a pulse at the output Q -terminal, provided the gate is open.

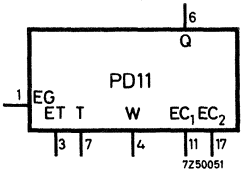
The duration of the output pulse can be increased by an external capacitance to be connected between the terminals $EC_1$ and $EC_2$.

The circuit is mounted inside a sealed metal can with 19 wire terminals.

| | | |
|---|---|---|
| Ambient temperature range: | | |
| | operating | - 25 to + 55 °C |
| | storage | - 55 to + 75 °C |
| Weight | | approx. 40 g |
| Case | | high standard case |




terminal location

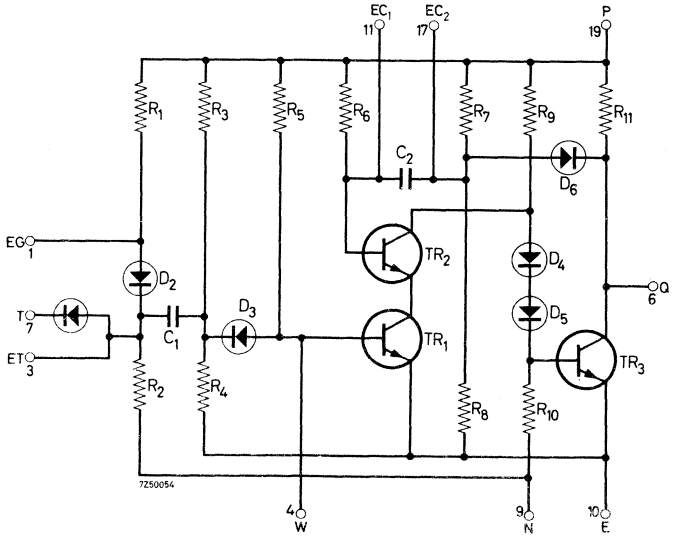



drawing symbol

## CIRCUIT DATA

Terminal

1 = EG = extension gate input
2 = not connected
3 = ET = extension trigger input
4 = W = extension trigger gate
5 = not connected
6 = Q = output
7 = T = trigger input
8 = not connected
9 = N = supply -12 V
10 = E = common supply 0 V
11 = $EC_1$ = for external capacitor
12 = not connected
13 = not connected
14 = not connected
15 = not connected
16 = not connected
17 = $EC_2$ = for external capacitor
18 = not connected
19 = P = supply +12 V




Power supply

Terminal 9 : $V_N$ = -12 V ±5 %, $-I_N$ = 1.5 mA
(transistor TR3 non-conducting)
= 1.7 mA
(transistor TR3 conducting)
10 : $V_E$ = 0 V common
19 : $V_P$ = +12 V ±5 %, $I_P$ = 19 mA
(transistor TR3 non-conducting)
= 28 mA
(transistor TR3 conducting)

The current values are nominal

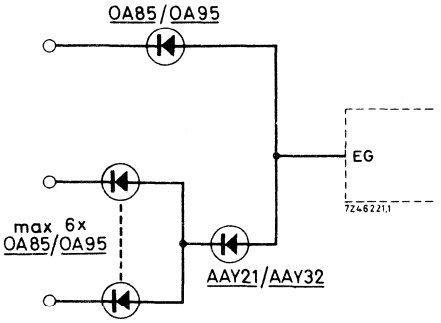
INPUT REQUIREMENTS (at $V_P$ = 11.4 V and $V_N$ = -12.6 V unless specified differently).

Gate input (EG-terminal)

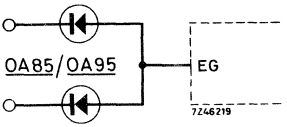
A d.c. voltage level is applied to terminal EG via an external diode.
A "positive low" voltage closes the gate, whilst a "positive high" voltage opens the gate.

Gate open

Voltage $V_G$ = min. 2/3Vp
= max. $V_P$




Gate extension input EG: max number of parallel input diodes: 7xOA85/OA95




Gate extension input EG: with two input diodes

Gate closed

Voltage $V_G$ = min. 0 V
= max. 0.3 V

Required direct current $-I_{GD}$ = max. 1.1 mA

Required transient charge when VG changes from 2/3 Vp to 0.5 V in 1.5 µs $-Q_{GT}$ = max. 1.2 nC

Time data

| | | | |
|---|---|---|---|
| Trigger gate setting time | $t_{gs}$ | = min. 26 µs | See point 6* |
| Trigger gate inhibiting time | $t_{gi}$ | = min. 26 µs | See point 7* |

*Section "Time definitions" of "Circuit blocks 10-Series".

Trigger input (T-terminal)

A negative-going voltage step is applied to terminal T. This voltage step on terminal T passes the gate, when it has been opened by the appropriate voltage level on terminal EG, and drives transistor $TR_3$ in the conducting state.

| | Gate open | Gate closed |
|---|---|---|
| Voltage | $V_G$ = min. 2/3 $V_p$<br>= max. $V_p$ | = min. 0 V<br>= max. 0.3 V |
| Required direct current | $-I_{TD}$ = max. 1.1 mA | 0 mA |
| | Gate open | Gate closed |
| Required transient charge when $V_T$ changes from 2/3 Vp to 0.5 V in 1.5 µs | $-Q_{TT}$ = max. 3.2 nC | 0 nC |

Recommended type of diodes and maximum number connected in parallel at terminal ET: 6 x BAY38/BAX13

Time data : see par. "Delays and switching times".

Input noise level $V_n$ = max. 1.2 V peak to peak

Base-input (W-terminal)

Input capacitance max. 60 pF

Additional triggering facilities can be obtained by connecting the output of the trigger gates to terminal W of the pulse driver, e.g. 6 trigger gates may be connected in parallel to terminal W provided the total wiring capacitance $C_W$ = max. 30 pF

OUTPUT DATA (at $V_p$ = 11.4 V and $V_N$ = -12.6 V unless specified differently).

Transistor $TR_3$ conducting

| | |
|---|---|
| Voltage | $V_Q$ = min. 0 V<br>= max. 0.3 V |
| Available direct current | $I_{QD}$ = min. 100 mA |
| Available transient charge when $V_Q$ changes from 2/3 Vp to 0.5 V in 1.5 µs | $Q_{QT}$ = min. 185 nC |

Maximum wiring capacitance 1500 pF

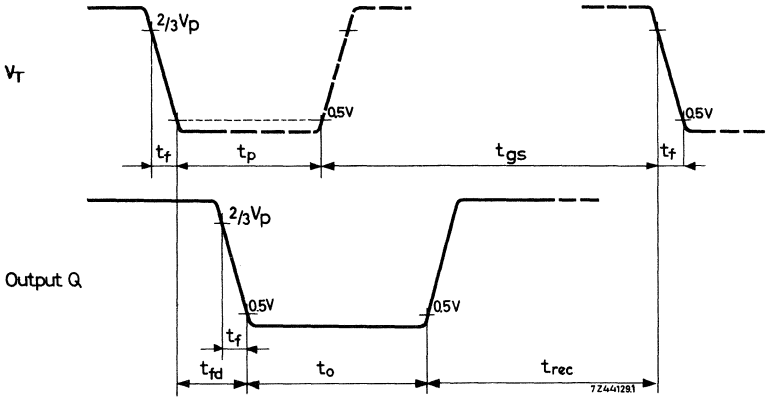
Delays and switching times

| | | |
|---|---|---|
| fall time | : $t_f$ | = max. 1.5 µs |
| fall delay | : $t_{fd}$ | = max. 2 µs |
| input pulse duration | : $t_p$ | = min. 2 µs |
| output pulse duration | : $t_o$ | = depends on value of external capacitor between terminals 11 and 17. |
| | | = max. 5 ms |
| recovery time | : $t_{rec}$ | = min. 2 $t_o$ |

The minimum time between two successive input pulses is determined by two factors:

1) $3 \times t_o \geq t_p + t_{gs}$ : the next input pulse may start a time = 2 $t_o$ after the trailing edge of the output pulse.

2) $3 \times t_o < t_p + t_{gs}$ : the next input pulse may start a time = $t_{gs}$ (26 µsec) after the trailing edge of the preceding input pulse.




Duration of the output pulse

| | |
|---|---|
| Intrinsic value | $t_f + t_o$ = max. 4 µs |
| Increase with external capacitor | 1 µs per 280 pF |
| Tolerance | ± 15 % |

Stability of output-pulse duration

An increase in ambient temperature by 1 °C gives a reduction of the pulse duration of less than 0.1 % and vise versa.
There is practically no difference in duration between different output pulses at any combination of permitted supply voltages.
An increase of the leakage current of the external capacitor ($C_{ext}$) with 1 µA decreases the pulse duration by less than 0.15 % and vice versa.

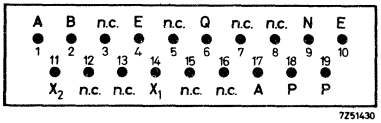
# PULSE SHAPER

The unit PS 10 contains a Schmitt trigger (squaring) circuit followed by an inverting amplifier.
An input signal of a magnitude exceeding the tripping level of the unit, is re-shaped and inverted into the standard d.c. level at the output. The output voltage transients are short and suitable for driving the various circuits at their trigger(T) inputs.
The terminals A and B are provided in order to be able to use the PS 10 for the following purposes:

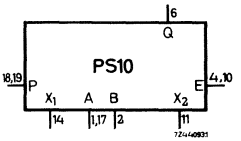
1 as a pulse shaper, driven by an external source
2 as a relaxation oscillator circuit
3 as a pulse shaper, driven by circuit blocks of the 10-series.

The circuit is mounted inside a sealed metal can with 19 wire terminals.

| | | |
|---|---|---|
| Ambient temperature range: | | |
| | operating | -25 to +55 °C |
| | | below 0 °C: derated data |
| | storage | -55 °C to +75 °C |
| Weight | | approx. 30 g |
| Case | | low standard case |



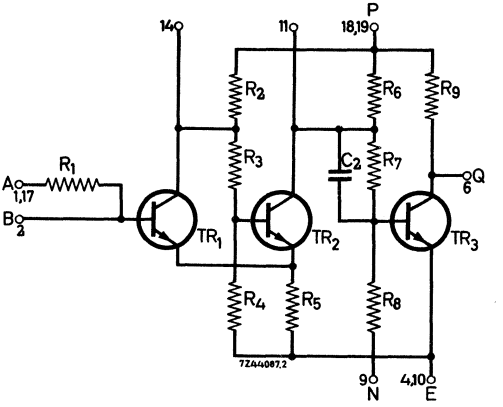

terminal location




drawing symbol

## CIRCUIT DATA

Terminal 1 = A = resistor input (interconnected to terminal 17)
2 = B = direct base input
3 = not connected
4 = E = common supply 0 V (interconnected to terminal 10)
5 = not connected
6 = Q = output
7 = not connected
8 = not connected
9 = N = supply - 12 V
10 = E = common supply 0 V (interconnected to terminal 4)
11 = $X_2$ = internally connected
12 = not connected
13 = not connected
14 = $X_1$ = internally connected
15 = not connected
16 = not connected
17 = A = resistor input (interconnected to terminal 1)
18 = P = supply + 12 V } terminals 18 and 19 interconnected
19 = P = supply + 12 V }




Power supply

Terminal 9 : $V_N$ = - 12 V ±5%, $-I_N$ = 1 mA } nominal value of the current
10 : $V_E$ = 0 V common
19 : $V_P$ = + 12 V ±5%, $I_P$ = 6 mA }

INPUT REQUIREMENTS (at $V_P$ = 11.4 V and $V_N$ = -12.6 V unless specified differently).

Application 1

Unit driven by an external source with $R_i$ = max. 24 kΩ
= max. 16 kΩ ($T_{amb}$ = min. -25 °C)*

Input voltage to be applied to terminal B

Transistor TR3 conducting (output level "positive low")

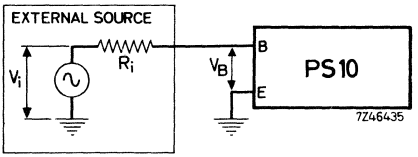
| | | |
|---|---|---|
| Voltage | $V_B$ | = max. 0.36 $V_P$ |
| limiting value | | = max. 10 V |
| Current | $I_B$ | = min. 0.1 mA |
| limiting value | | = max. 12 mA |

Transistor TR3 non-conducting (output level "positive high")

| | | |
|---|---|---|
| Voltage | $V_B$ | = min. 0.13 $V_P$ |
| limiting value | $-V_B$ | = max. 1.2 V |
| Current | $-I_B$ | = max. 0.01 mA |

Hysteresis (difference between on and off tripping level)

Voltage $\Delta V_B$ = min. 0.12 $V_P$




The hysteresis is affected by the $R_i$ of the external source.
The relation is given by the following formula:

| $T_{amb}$ = min. 0 °C | $T_{amb}$ = min. - 25 °C |
|---|---|
| $\Delta V_i$ = min. (0.12 $V_P$ - 0.057 $R_i$) | = min. (0.12 $V_P$ - 0.085 $R_i$) |
| $\Delta V_B = \frac{\Delta V_i}{1 + 0.07\ R_i}$ | $= \frac{\Delta V_i}{1 + 0.084\ R_i}$ |

$R_i$ in kΩ and Vin volt

Application 2 : Unit used in a relaxation oscillator circuit

Application information will be issued separately.

Application 3 : Unit driven by circuit blocks of the 10-series

For this operation terminal A has to be connected to $V_P$ (terminal 18) and the input voltage $V_G$ has to be applied to terminal B via a diode, e.g. type OA 85/OA 95.

* Between 0 and - 25 °C to be derived by linear interpolation.

Transistor TR3 non-conducting (output level "positive high")

| | |
|---|---|
| Voltage | $V_G$ = min. 0 V<br>= max. 0.3 V |
| Required direct current | $-I_{GD}$ = max. 0.9 mA |
| Required transient charge when $V_B$ changes from 2/3 $V_P$ to 0.5 V in 1.5 µs | $-Q_{GT}$ = max. 0.8 nC |

Transistor TR3 conducting (output level "positive low")

| | |
|---|---|
| Voltage | $V_G$ = min. 2/3 $V_P$<br>Type of diodes and number to be connected in parallel to terminal B:<br>30 x OA 85/OA 95/AAY 21/AAY32 |

OUTPUT DATA (at $V_P$ = 11.4 V and $V_N$ = - 12.6 V unless specified differently)

Transistor TR3 conducting (output level "positive low")

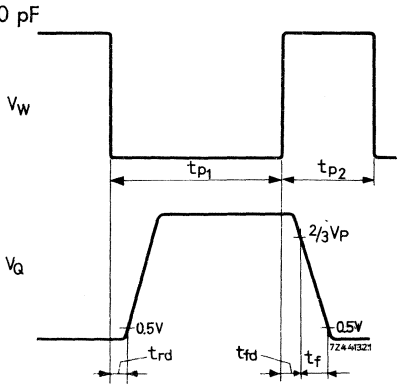
| | |
|---|---|
| Voltage | $V_Q$ = min. 0 V<br>= max. 0.3 V |
| Available direct current | $I_{QD}$ = min. 10 mA<br>= min. 7.7 mA ($T_{amb}$ = min. - 25 °C)* |
| Available transient charge when $V_Q$ changes from 2/3 $V_P$ to 0.5 V in 1.5 µs | $Q_{QT}$ = min. 39 nC<br>min. 21 nC ($T_{amb}$ = min. - 25 °C)* |

Maximum wiring capacitance 200 pF

Delays and switching times

pulse duration : $t_{p1}$ = min. 6 µs
$t_{p2}$ = min. 3 µs
fall delay : $t_{fd}$ = max. 0.1 µs
rise delay : $t_{rd}$ = max. 0.1 µs
fall time : $t_f$ = max. 1.5 µs

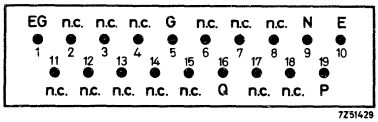
* Between 0 and - 25 °C to be derived by linear interpolation.



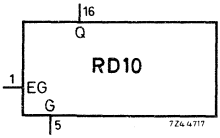
# RELAY DRIVER

The unit comprises a single input positive diode gate followed by a non-inverting amplifier, intended for driving relays. The number of gate (G) inputs can be extended by means of external diodes to be connected to the extension gate input EG.
The circuit is mounted inside a sealed metal can with 19 wire terminals.

| | | |
|---|---|---|
| Maximum pulse repetition frequency | | 100 Hz |
| Ambient temperature range: | | |
| | operating | -25 to +55 °C<br>below 0 °C: derated output data |
| | storage | -55 °C to +75 °C |
| Weight | | approx. 30 g |
| Case | | low standard case |




terminal location

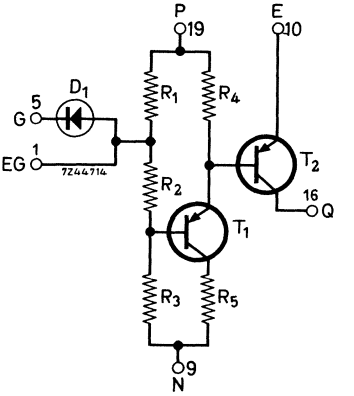



drawing symbol

## CIRCUIT DATA

Terminal

| | | | |
|---|---|---|---|
| 1 = EG | = extension gate input | 11 = | not connected |
| 2 = | not connected | 12 = | not connected |
| 3 = | not connected | 13 = | not connected |
| 4 = | not connected | 14 = | not connected |
| 5 = G | = gate input | 15 = | not connected |
| 6 = | not connected | 16 = Q | = output |
| 7 = | not connected | 17 = | not connected |
| 8 = | not connected | 18 = | not connected |
| 9 = N | = supply - 12V | 19 = P | = supply + 12V |
| 10 = E | = common supply 0V | | |




Power supply

Terminal 9 : $V_N$ = - 12V ± 5%; $-I_N$ = 4.2 mA (output transistor non-conducting) } nominal values of the current

$-I_N$ = 16.8 mA (output transistor conducting) } nominal values of the current

10 : $V_E$ = 0V common

19 : $V_P$ = + 12V ± 5% $I_P$ = 4.6 mA (output transistor non-conducting) } nominal values of the current

$I_P$ = 8 mA (output transistor conducting) } nominal values of the current

INPUT REQUIREMENTS (at $V_P$ = 11.4V and $V_N$ = - 12.6V unless specified differently).

Output transistor conducting

Voltage $V_G$ = max. 0.3V
= min. 0V

Total required direct current $-I_{GD}$ = max. 4.7 mA

Total required transient charge, when $V_G$ changes from $2/3\,V_P$ to 0.5V in 1.5 µs $-Q_{GT}$ = max. 3.4 nC

Output transistor non-conducting

Voltage $V_G$ = min. $2/3 V_P$
= max. $V_P$
Type of diodes and maximum number connected in parallel at terminal EG:
12 x AAY21/AAY32

OUTPUT DATA

Output transistor conducting

Voltage $-V_Q$ = max. 0.5V

Available load current $-I_Q$ = min. 200 mA
= min. 132 mA ($T_{amb}$ = min. - 25 °C)*

Output transistor non-conducting

Voltage $-V_Q$ = absolute max. 55V (resistive load)
= absolute max. 30V (inductive load)

Leakage current $-I_Q$ = max. 2.5 mA

Notes: 1) Protection diode

When inductive loads are switched, the output transistor $T_2$ must be protected against voltage transients by means of a diode, mounted across the load, the cathode connected to the Q - output terminal. Recommended type of diode: BY100.

2) Mounting rules

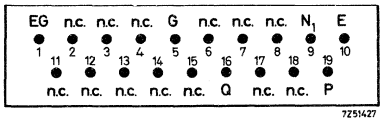
Due to heat dissipation it is not allowed to mount more than 8 units RD10 on e.g. a printed-wiring board of the standard dimensions (121.8 mm x 207.0 mm x 1.6 mm).
This holds for vertical mounting as well as for horizontal mounting. Moreover the units must be spread over the board as much as possible. Mounting of 3 printed-wiring boards equipped with RD 10's adjacent to each other in the mounting chassis 4322 026 38240 is prohibited without forced cooling.

* Between 0 and - 25 °C to be derived by linear interpolation.

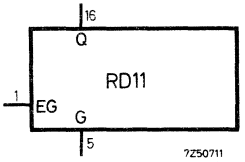
# RELAY DRIVER

The unit comprises a single input positive diode gate followed by a non-inverting amplifier, intended for driving inductive and resistive loads. The number of gate (G) inputs can be extended by means of external diodes to be connected to the extension gate input EG.
The output transistor $TR_3$ is cut off, only when all inputs are at a positive high level (min. 2/3 $V_p$).
The terminal location is exactly similar to that of the RD 10.
The circuit is mounted inside a sealed metal can with 19 wire terminals.

| | | |
|---|---|---|
| Maximum pulse repetition frequency | | 100 Hz |
| Ambient temperature range: | | |
| | operating | −25 to +55 °C |
| | storage | −55 to +75 °C |
| Weight | | approx. 30 g |
| Case | | low standard case |




terminal location

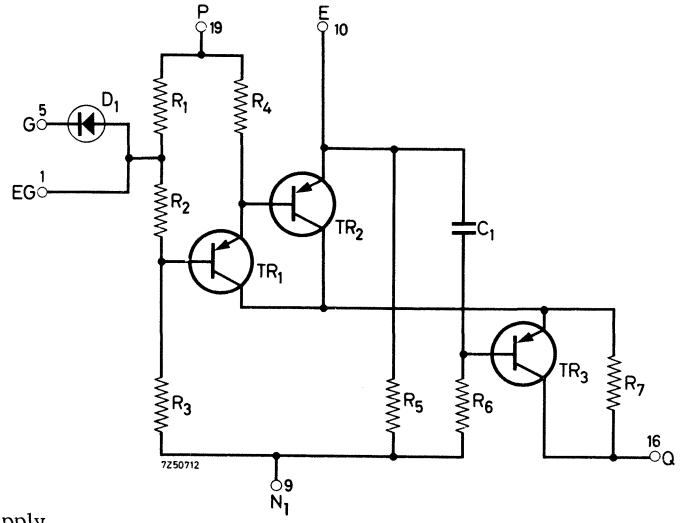



drawing symbol

CIRCUIT DATA

Terminal

| | | | |
|---|---|---|---|
| 1 = EG | = extension gate input | 11 = | not connected |
| 2 = | not connected | 12 = | not connected |
| 3 = | not connected | 13 = | not connected |
| 4 = | not connected | 14 = | not connected |
| 5 = G | = gate input | 15 = | not connected |
| 6 = | not connected | 16 = Q | = output |
| 7 = | not connected | 17 = | not connected |
| 8 = | not connected | 18 = | not connected |
| 9 = $N_1$ | = supply - 12 V | 19 = P | = supply + 12 V |
| 10 = E | = common supply 0 V | | |




Power supply

Terminal 9 : $V_{N_1}$ = −12 V ± 5% ; $-I_{N_1}$ = 17 mA (output transistor conducting)
10 : $V_E$ = 0 V common
19 : $V_p$ = +12 V ± 5% ; $I_p$ = 8 mA (output transistor conducting)

} nominal values of the current

Output voltage: $-V_{N_2}$ = 12 V up to max. 55 V;
$-I_{N_2}$ = max. 200 mA

INPUT REQUIREMENTS (at $V_p$ = 11.4 V and $V_{N_1}$ = −12.6 V unless specified differently)

Output transistor conducting

Voltage $V_G$ = max. 0.3 V, min. 0 V

| | |
|---|---|
| Total required direct current | $-I_{GD}$ = max. 4.7 mA |
| Total required transient charge, when $V_G$ changes from 2/3 $V_p$ to 0.5 V in 1.5 $\mu$s | $-Q_{GT}$ = max. 3.4 nC |

Output transistor non-conducting

| | |
|---|---|
| Voltage | $V_G$ = min. 2/3 $V_p$ / max. $V_p$ |

Type of diodes and maximum number connected in parallel at terminal EG: 12 x OA95/OA85

OUTPUT DATA

Output transistor conducting

| | |
|---|---|
| Voltage | $-V_Q$ = max. 0.8 V |
| Available load current | $-I_Q$ = min. 200 mA |

Output transistor non-conducting

| | |
|---|---|
| Voltage | $-V_Q$ = absolute max. 55 V |
| Leakage current | $-I_Q$ = max. 5 mA |

Notes:

1. Protection diode

When inductive loads are switched, the output transistor $TR_3$ must be protected against voltage transients by means of a diode, mounted across the load, the cathode connected to the Q - output terminal. Recommended types of diode: BAY39/1N921/1N922/BAX78.

2. Mounting rules

Due to heat dissipation it is not allowed to mount more than 8 units RD 11 on e.g. a printed-wiring board of the standard dimensions (121.8 mm x 207.0 mm x 1.6 mm).
This holds for vertical mounting as well as for horizontal mounting. Moreover the units must be spread over the board as much as possible. Mounting of 3 printed-wiring boards equipped with RD 11's adjacent to each other in the mounting chassis 4322 026 38240 is prohibited without forced cooling.

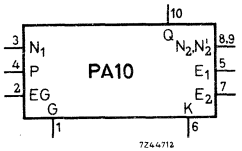
3. Power supply

When the power supplies are switched on or switched off, care must be taken that the output voltage $V_{N2}$ may only be applied without the presence of the other supply voltages $V_{N1}$ and $V_p$ for a time of max. 60 s.

# POWER AMPLIFIER

The PA10 consists of a npn/pnp/pnp transistor amplifier circuit, designed to be used as a power amplifier in the "10-series" of circuit blocks.
The amplifier can be driven directly by the circuit blocks FF 10, FF 11, FF 12, 2GI10, 2GI11, 2GI12, OS11, PD11, PS10, GA 11 and TU10.
The output loadability is 2A, 55 V (abs. max. values). The built-in diode across the output terminals protects the output transistor against voltage transients which occur when the unit is driving an inductive load.
The circuit is mounted on a glass epoxy printed-wiring board, the output transistor is provided with an aluminium heat sink.

| | | |
|---|---|---|
| Ambient temperature range: | | |
| | operating | - 25 to + 55 °C |
| | storage | - 55 to + 75 °C |
| Weight | | approx. 90 g |

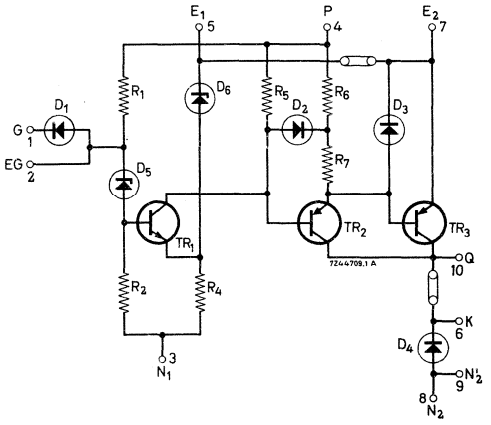



drawing symbol

## CIRCUIT DATA

Terminal

1 = G = gate input
2 = EG = extention gate input
3 = $N_1$ = supply - 12 V
4 = P = supply + 12V
5 = $E_1$ = common supply 0 V
6 = K = cathode of diode D 4
7 = $E_2$ = common supply 0 V
8 = $N_2$ = supply abs. max. 55 V
9 = $N_2'$ = supply abs. max. 55 V
10 = Q = output



Power supply

Terminal 3 : $V_{N_1}$ = - 12 V ± 5%, - $I_{N1}$ = max. 30 mA ($TR_3$ conducting)
= max. 18 mA ($TR_3$ non-conducting)

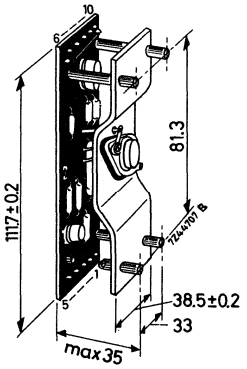
4: $V_P$ = + 12 V ± 5%, $I_P$ = max. 41 mA ($TR_3$ conducting)
= max. 39.5 mA ($TR_3$ non-conducting)

5: $V_{E1}$ = 0 V common

7: $V_{E2}$ = 0 V common

8: $-V_{N2}$ = 12 V up to max. 55 V, - $I_{N2}$ = max. 2A

## MECHANICAL CONSTRUCTION




The dimensions (max 111.9 mm x 38.7 mm x 35 mm) and terminal location can be seen from the drawing given above.
Since the aluminium heat-sink is insulated from the circuit, no special measures need be taken regarding the mounting of the unit. The mechanical design of the PA 10 is based on its use in the standardized mounting chassis 4322 026 38240. For this purpose the PA 10 is to be mounted directly on a printed-wiring board. On such a standard printed-wiring board (4322 026 38680), up to four PA 10's can be mounted; it takes two positions in the chassis 4322 026 38240. To ensure proper cooling of the unit, the PA 10 has to be mounted in such a way that a free flow of air through it is guaranteed.

## INPUT REQUIREMENTS

A d.c. voltage level is applied to terminal G.

Output transistor $TR_3$ non-conducting

| | |
|---|---|
| voltage | $V_G$ = max. 0.3 V<br>= min. 0 V |
| required direct current | $-I_{GD}$ = max. 5.3 mA |
| required transient charge when $V_G$ changes from 2/3 $V_P$ to 0.5 V in 1.5 µs | $-Q_{GT}$ = max. 5.2 nC |

Output transistor $TR_3$ conducting

| | |
|---|---|
| voltage | $V_G$ = min. 2/3 $V_P$<br>= max. $V_P$ |

Type of diodes and maximum number connected in parallel at terminal EG:
12 x OA85/OA95

## OUTPUT DATA

Output transistor $TR_3$ non-conducting

| | |
|---|---|
| voltage | $-V_Q$ = absolute max. 55 V |
| leakage current | $-I_Q$ = max. 30 mA |

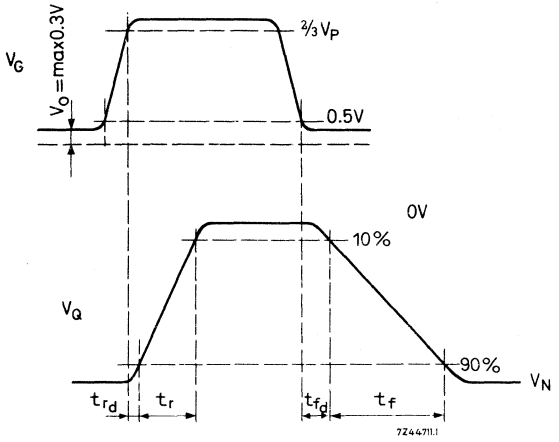
Output transistor $TR_3$ conducting

| | |
|---|---|
| voltage | $-V_Q$ = max. 1.2 V |
| available load current | $-I_Q$ = min. 2A (switching rate = max. 40 Hz)<br>For load currents less than 2A the maximum switching rate has to be determined with the formula below:<br>$f_{max} = 360 - 160\,\lvert I_Q \rvert$ |

Delays and switching times (for orientation only)

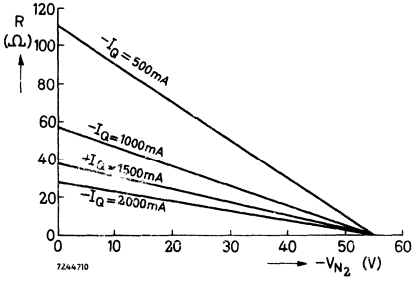
Unit loaded with a resistor of 30 Ω

Rise delay : $t_{rd}$ = max. 10 µs
Rise time : $t_r$ = max. 50 µs
Fall delay : $t_{fd}$ = max. 25 µs
Fall time : $t_f$ = max. 100 µs




Unit loaded with an inductive load

The unit is provided with a built-in diode to protect the output transistor against voltage transients which occur when an inductive load is switched. This protection is realized at the expense of a very long fall delay time of the current in this load.
At supply voltages below 55 V , however, a wire jumper in series with this diode can be interchanged with a resistor to decrease this delay time.
The max. permissible value of this resistor is given in the figure below with the current, flowing through the load at the moment of switching-off, as parameter.



# NUMERICAL INDICATOR TUBE DRIVER

The unit ID 10 can drive the numerical indicator tube ZM1000, ZM1020 or ZM1080. It has to be driven by a decade counter operating in the 1-2-4-8 or 1-2-4-2 (jump at 8) code.

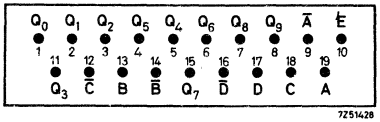
The unit comprises the decoding circuits for both codes as well as the driver stages for the ZM1000, ZM1020 or ZM1080.

When the decade counter is set on digit number 0, the inputs A, B, C and D of the ID 10 are to be connected to the outputs of the flip-flops in the decade, which are at low level. Consequently the inputs $\overline{A}$, $\overline{B}$, $\overline{C}$ and $\overline{D}$ are to be connected to the flip-flop outputs which are at high level.

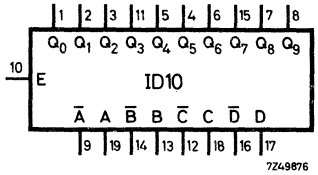
Primarily the ID 10 forms a load for outputs of flip-flops, which are at high level. For flip-flop outputs at low level the ID 10 forms a relative low load.
So any additional load in excess of the ID 10 is restricted by the specified minimum value of the high level for the flip-flop outputs.
The last flip-flop of the decade counter is still capable to drive the next decade.

The circuit is mounted inside a sealed metal can with 19 wire terminals.

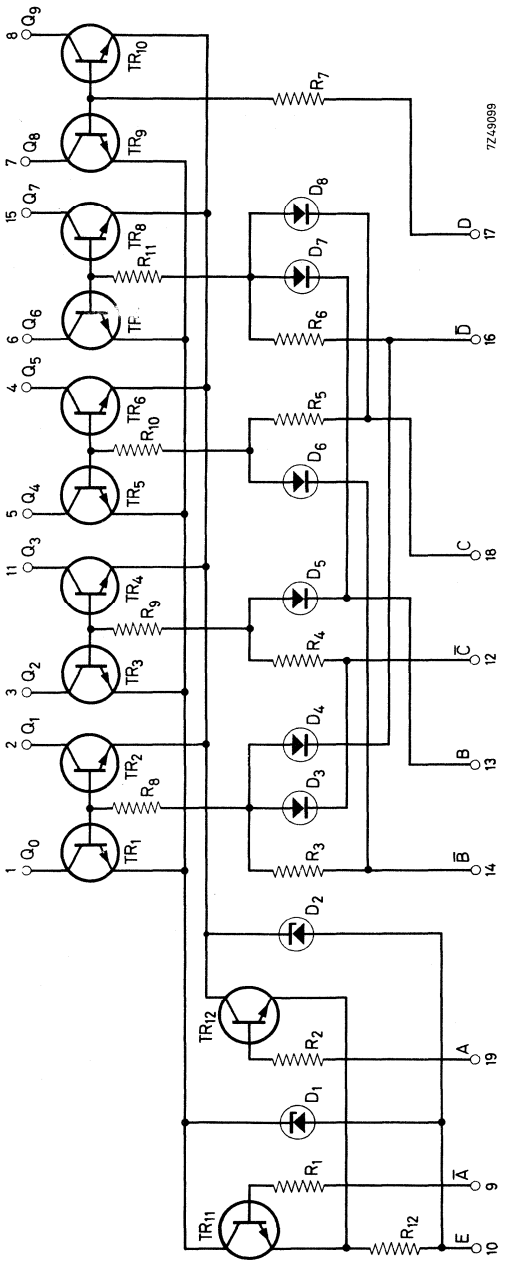
| | | |
|---|---|---|
| Ambient-temperature range: | | |
| | operating | −55 to +55 °C |
| | storage | −55 to +85 °C |
| Weight | | approx. 40 g |
| Case | | high standard case |




terminal location




drawing symbol




CIRCUIT DATA

Terminals

1 = $Q_0$ = output to be connected to pin $k_0$ of indicator tube
2 = $Q_1$ = output to be connected to pin $k_1$ of indicator tube
3 = $Q_2$ = output to be connected to pin $k_2$ of indicator tube
4 = $Q_5$ = output to be connected to pin $k_5$ of indicator tube
5 = $Q_4$ = output to be connected to pin $k_4$ of indicator tube
6 = $Q_6$ = output to be connected to pin $k_6$ of indicator tube
7 = $Q_8$ = output to be connected to pin $k_8$ of indicator tube
8 = $Q_9$ = output to be connected to pin $k_9$ of indicator tube
9 = $\overline{A}$ = input to be connected to $\overline{Q}$ of driving flip-flop A
10 = E = common supply 0V
11 = $Q_3$ = output to be connected to pin $k_3$ of indicator tube
12 = $\overline{C}$ = input to be connected to $\overline{Q}$ of driving flip-flop C
13 = B = input to be connected to Q of driving flip-flop B
14 = $\overline{B}$ = input to be connected to $\overline{Q}$ of driving flip-flop B
15 = $Q_7$ = output to be connected to pin $k_7$ of indicator tube
16 = $\overline{D}$ = input to be connected to $\overline{Q}$ of driving flip-flop D
17 = D = input to be connected to Q of driving flip-flop D
18 = C = input to be connected to Q of driving flip-flop C
19 = A = input to be connected to Q of driving flip-flop A

Power supply

Terminal 10 : 0V common, connected to the metal case

$V_b$ = 250V ± 10%, $R_a$ = 68kΩ ± 2% } power supply for the ZM1000,
$V_b$ = 250V ± 15%, $R_a$ = 62kΩ ± 2% } ZM1020 or ZM1080

INPUT REQUIREMENTS

Input at low level

Voltage $V_I$ = min. 0V
= max. 0.3V

| | A, $\overline{A}$, D | $\overline{B}$, C, $\overline{C}$, $\overline{D}$ | B |
|---|---|---|---|
| Required direct current | 0mA | 0.3mA | 0.6mA |

Input at high level

Voltage $V_I$ = min. 7.6V
= max. 15V

| | A, $\overline{A}$, D | $\overline{B}$, C, $\overline{C}$, $\overline{D}$ | B |
|---|---|---|---|
| Required direct current | 0.2mA | 0.28mA | 0mA |

When the ID 10 is driven by flip-flops with only the Q-outputs connected to the inputs of the ID 10, the Q-outputs of these flip-flops may furthermore be loaded with a number of 10-series diode-inputs, provided each driven input represents a load of $-I_D$ = max. 1.1mA and $-Q_T$ = max. 3.4nC, as stated on the next page.

| input ID 10 | number of diode-inputs | |
|---|---|---|
| | min. 0 °C | min. -25 °C |
| A, $\overline{A}$, D | 6 | 6 |
| B | 7 | 5 |
| $\overline{B}$, C, $\overline{C}$, $\overline{D}$ | 4 | 4 |

The loadability of the flip-flop outputs can be increased by connecting an external resistor of 51 kΩ ± 5% in parallel for each additional diode-input with the built-in collector resistor of the corresponding output. This resistor has to be connected between the output terminal and the positive voltage supply $V_p$.
This resistor however represents a load at low level for the driving unit.

Required direct current : $I_R$ = max. 0.2 mA
Required transient charge: $Q_R$ = max. 0.2 nC

Note - When a current is flowing towards the unit the positive sign is used.

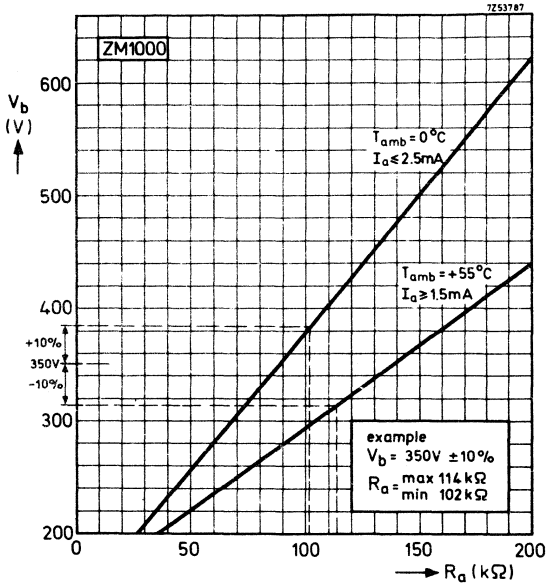
OUTPUT DATA

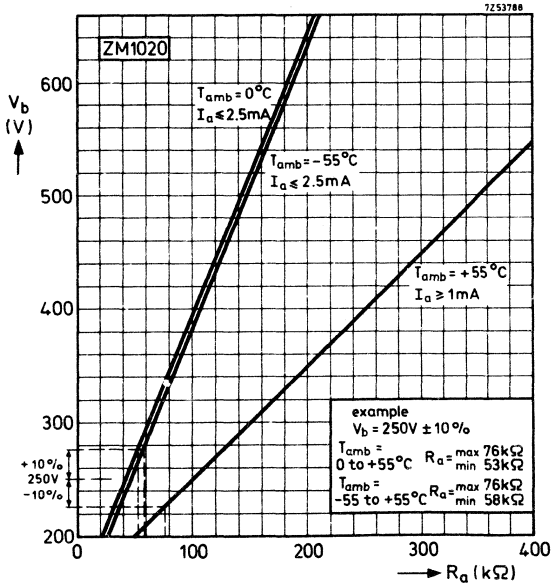
The outputs $Q_0$ up to and including $Q_9$ of the ID 10 have to be connected to the pins → $k_0$ up to and including $k_9$ of the numerical indicator tube ZM1000, ZM1020 or ZM1080.
The anode of these tubes has to be connected via a resistor $R_a$ to the high voltage power supply $V_b$.

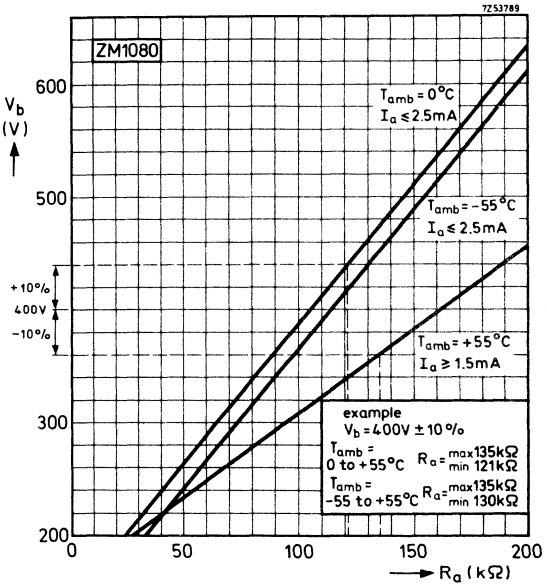
The current available at these 10 numerical outputs of the ID 10 can cope with the → required cathode current $I_k$ of the indicator tube ZM1000, ZM1020 or ZM1080, when the following conditions are observed:

a. operation temperature range
b. power supply $V_b$ for ZM1000, ZM1020 or ZM1080
c. anode series resistor $R_a$

In the following graphs these data are specified.

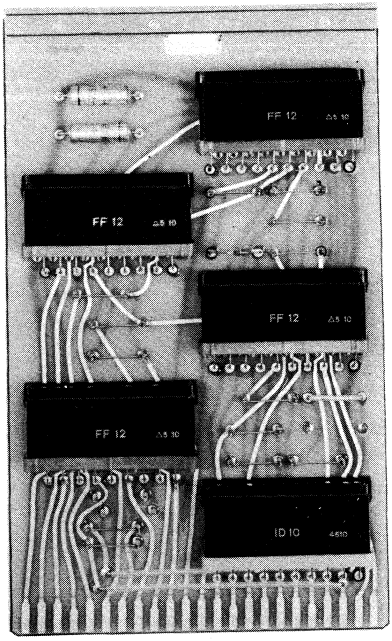

7Z53787
ZM1000
$V_b$ (V)
600
500
400
300
200
+10%
350V
-10%
$T_{amb}$ = 0°C
$I_a \leq 2.5$mA
$T_{amb}$ = +55°C
$I_a \geq 1.5$mA
example
$V_b$ = 350V ±10%
$R_a$ = max 114kΩ
min 102kΩ
0
50
100
150
200
$R_a$ (kΩ)


7Z53788
ZM1020
$V_b$ (V)
600
500
400
300
200
+10%
250V
-10%
$T_{amb}$ = 0°C
$I_a \leq 2.5$mA
$T_{amb}$ = −55°C
$I_a \leq 2.5$mA
$T_{amb}$ = +55°C
$I_a \geq 1$mA
example
$V_b$ = 250V ±10%
$T_{amb}$ = 0 to +55°C $R_a$ = max 76kΩ min 53kΩ
$T_{amb}$ = −55 to +55°C $R_a$ = max 76kΩ min 58kΩ
0
100
200
300
400
$R_a$ (kΩ)




Wiring capacitance at each output Q-terminal of the ID10: max. 500 pF

# DECADE COUNTER AND NUMERICAL INDICATOR TUBE DRIVER ASSEMBLY




RZ 22603-11

The assembly consists of four circuit blocks FF 12, with or without a circuit block ID 10, mounted on a printed-wiring board. It is available in five versions.

- DCA 10 A catalog number 2722 009 02001.

  This assembly contains four flip-flops FF 12, intended to be used as a single decade counter, operating in the 1-2-4-8 code, and a numerical indicator tube driver ID 10, providing the BCD - to decimal decoding- and driving circuits for the numerical indicator tube ZM1000, ZM1020 or ZM1080.
  The required interconnections are shown in Figs. 1 and 2.

- DCA 10 B catalog number 2722 009 02011.

  This assembly is identical to the DCA 10 A but without the circuit block ID 10 mounted on the board. The lay-out of the printed-wiring board allows the mounting of the ID 10 separately (see Figs. 7 and 8).

- DCA 10 C catalog number 2722 009 02021.

  This assembly contains four flip-flops FF 12, intended to be used as a buffer memory. When the trigger inputs of the four flip-flops are interconnected externally, with one trigger pulse applied to this common trigger line, the contents of a decade counter can be shifted in parallel into the buffer memory. To this end the Q-outputs of the decade counter have to be connected to the corresponding gate inputs (G) of the buffer memory flip-flops.

  Furthermore the assembly contains the numerical indicator tube driver ID 10, providing the BCD - to decimal decoding and driving circuits for the numerical indicator tube ZM1000, ZM1020 or ZM1080.
  The required interconnections are shown in Figs. 9 and 10.

- DCA 10 D catalog number 2722 009 02031.

  This assembly is identical to the DCA 10 C but without the circuit block ID 10 mounted on the board. The lay-out of the printed-wiring board allows the mounting of the ID 10 separately (see Figs. 11 and 12).

- DCA 10 E catalog number 2722 009 02041.

  This assembly contains four flip-flops FF 12, intended to be used as a binary counter, scaler of 16.
  The required interconnections are shown in Figs. 13 and 14.

All these versions are provided with the capacitors $C_1$ and $C_2$, which filter the supply voltages from noise. These capacitors are mounted on the printed-wiring board.

The bare printed-wiring board (catalog number 4322 026 38700), provided with plated-through holes and double-sided goldplated contacts, is made of glass-epoxy material. Moreover, the printed-wiring board is delivered with an extractor and a locking device. With the mating connector (catalog number 2422 020 52591), not supplied with the assembly, the printed-wiring board of standard dimensions (121.8 mm x 207.0 mm x 1.6 mm) can be used directly in the standard mounting chassis (catalog number 4322 026 38240). The circuit blocks are secured to the printed-wiring board by means of locking caps (catalog number 4322 026 32150).

| | | |
|---|---|---|
| Counting rate | | max. 30 kHz |
| Ambient temperature range | | |
| | operating | −25 to +55 °C |
| | | below 0 °C: derated output data |
| | storage | −55 to +75 °C |
| Weight | | approx. 300 g |

The date specified below apply to the DCA 10 A in particular.
For the sake of simplicity for the other versions only data are specified separately, which differ from those of the DCA 10 A.

# DECADE COUNTER AND NUMERICAL INDICATOR TUBE DRIVER DCA 10 A

## CIRCUIT DATA

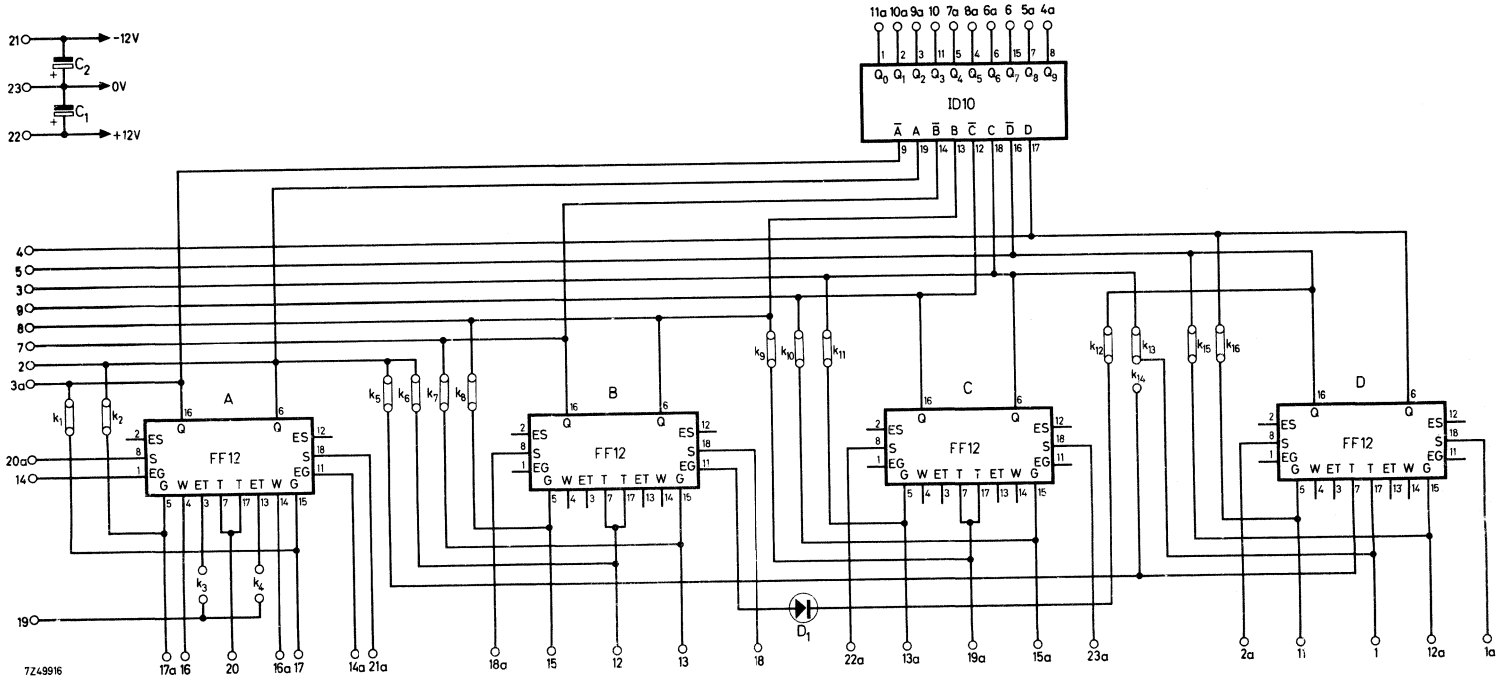



Fig. 1

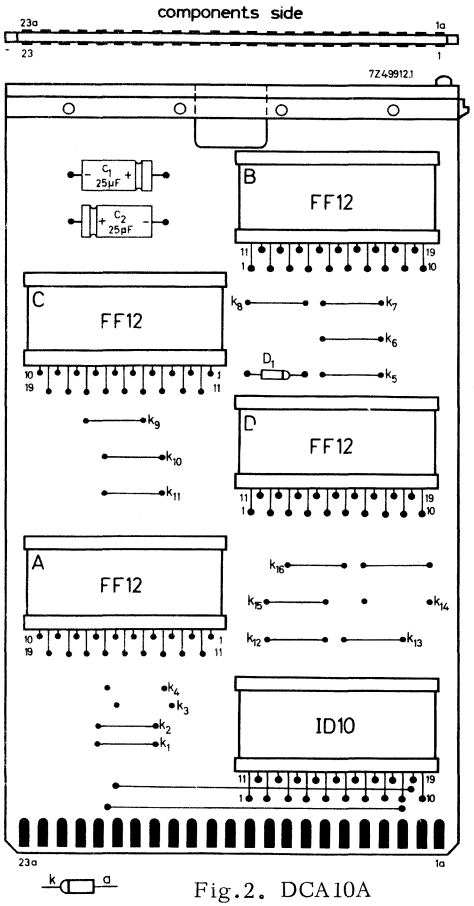



Fig.2. DCA10A

Terminals

1 = trigger input T of flip-flop D
2 = output Q of flip-flop A
3 = output Q of flip-flop C
4 = output Q of flip-flop D
5 = output $\overline{Q}$ of flip-flop D
6 = numerical output 7 of ID 10
7 = output $\overline{Q}$ of flip-flop B
8 = output Q of flip-flop B
9 = output $\overline{Q}$ of flip-flop C
10 = numerical output 3 of ID 10
11 = gate input G of flip-flop D
12 = trigger input T of flip-flop B
13 = gate input G of flip-flop B
14 = extension gate input EG of flip-flop A
15 = gate input G of flip-flop B
16 = base input W of flip-flop A
17 = gate input G of flip-flop A
18 = set input S of flip-flop B
19 = additional trigger input T of flip-flop A
20 = trigger input T of flip-flop A
21 = common negative supply −12 V
22 = common positive supply +12 V
23 = common supply 0 V

1a = set input S of flip-flop D
2a = set input S of flip-flop D
3a = output $\overline{Q}$ of flip-flop A
4a = numerical output 9 of ID 10
5a = numerical output 8 of ID 10
6a = numerical output 6 of ID 10
7a = numerical output 4 of ID 10
8a = numerical output 5 of ID 10
9a = numerical output 2 of ID 10
10a = numerical output 1 of ID 10
11a = numerical output 0 of ID 10
12a = gate input G of flip-flop D
13a = gate input G of flip-flop C
14a = extension gate input EG of flip-flop A
15a = gate input G of flip-flop C
16a = base input W of flip-flop A
17a = gate input G of flip-flop A
18a = set input S of flip-flop B
19a = trigger input T of flip-flop C
20a = set input S of flip-flop A
21a = set input S of flip-flop A
22a = set input S of flip-flop C
23a = set input S of flip-flop C

Power supply

Terminal 21 : $V_N = -12\ V \pm 5\%$, $-I_N = 4.1$ mA
22 : $V_P = +12\ V \pm 5\%$, $I_P = 30$ mA
23 : $V_E = 0$ V common

} The current values are nominal

INPUT REQUIREMENTS (at $V_P = 11.4$ V and $V_N = -12.6$ V unless specified differently)

Set/reset input (S-terminals)

Each S-input of the four flip-flops is brought out separately. A "positive low" voltage (between 0 V and 0.3 V) drives the corresponding transistor into the non-conducting state.

| | | |
|---|---|---|
| Transistor-conducting | | |
| Voltage | $V_S$ | = min. 2/3 $V_P$<br>= max. $V_P$ |
| Transistor non-conducting | | |
| Voltage | $V_S$ | = min. 0 V<br>= max. 0.3 V |
| Required direct current | $-I_{SD}$ | = max. 1.95 mA |
| Required transient charge when $V_S$ changes from 2/3 $V_P$ to 0.5 V in 1.5 $\mu$s | $-Q_{ST}$ | = max. 2.8 nC |

When the four flip-flops are reset simultaneously

| | | | | | | |
|---|---|---|---|---|---|---|
| Required direct current | $-I_{SD}$ | = | min. | 7.8 | mA | |
| Required transient charge when $V_S$ changes from 2/3 $V_P$ to 0.5 V in 1.5 $\mu$s | $-Q_{ST}$ | = | max. | 11.2 | nC | |

Time data

| | | | | | | |
|---|---|---|---|---|---|---|
| Pulse duration | $t_p$ | = | min. | 8 | $\mu$s | See point 4 x) |
| Recovery time | $t_{rec}$ | = | min. | 15 | $\mu$s | |
| Time delay between S- and T-signal | $t_{st}$ | = | min. | 15 | $\mu$s | See point 5 x) |

Gate input (G-terminals)

A d.c. voltage level is applied to terminal G.
A "positive low" voltage closes the gate, whilst a "positive high" voltage (between 2/3 $V_P$ and $V_P$) opens the gate.

Gate open

| | | | | | | |
|---|---|---|---|---|---|---|
| Voltage | $V_G$ | = | min. | 2/3 | $V_P$ | |
| | | = | max. | | $V_P$ | |

Gate closed

| | | | | | | |
|---|---|---|---|---|---|---|
| Voltage | $V_G$ | = | min. | 0 | V | |
| | | = | max. | 0.3 | V | |
| Required direct current | $-I_{GD}$ | = | max. | 1.1 | mA | |
| Required transient charge when $V_G$ changes from 2/3 $V_P$ to 0.5 V in 1.5 $\mu$s | $-Q_{GT}$ | = | max. | 1.2 | nC | |

Time data

| | | | | | | |
|---|---|---|---|---|---|---|
| Trigger gate setting time | $t_{gs}$ | = | min. | 29 | $\mu$s | See point 6 x) |
| Trigger gate inhibiting time | $t_{gi}$ | = | min. | 29 | $\mu$s | See point 7 x) |

Trigger input (T-terminals)

A negative-going voltage step or trigger pulse is applied to the trigger inputs T of flip-flop A (terminal 20).
Each trigger pulse applied to this terminal switches the flip-flop, provided that the corresponding G- and EG inputs are left floating or min. 2/3 $V_P$ (gate open).

x) Section "Time definitions" of "Circuit blocks 10-Series".

| | | Gate open | Gate closed |
|---|---|---|---|
| | $V_G$ | = min. 2/3 $V_P$ | = min. 0 V |
| | | = max. $V_P$ | = max. 0.3 V |
| Required direct current when $V_T$ = max. 0.3 V | $-I_{TD}$ | = max. 1.1 mA | = 0 mA |
| Required transient charge when $V_T$ changes from 2/3 $V_P$ to 0.5 V in 1.5 $\mu$s | $-Q_{TT}$ | = max. 3.4 nC | = 0 nC |
| Time data | | | |
| Fall time | $t_f$ | = max. 1.5 $\mu$s | See point 3 x) |
| Pulse duration | $t_p$ | = min. 2 $\mu$s | |
| Trigger gate setting time | $t_{gs}$ | = min. 29 $\mu$s | |

Base input (W-terminals)

Capacitance (wiring plus output of TG 13, TG 14 or TG 15) max. 95 pF

Note - The output capacitance of the trigger gates TG 13, TG 14 and TG 15 is max. 5 pF

OUTPUT DATA (at $V_P$ = 11.4 V and $V_N$ = −12.6 V, unless specified differently)

Decade counter section

In excess of the internal load, represented by the circuit blocks mounted on the printed-wiring board, including the numerical indicator tube driver ID 10, the Q-outputs of each flip-flop in the decade counter may furthermore be loaded as specified in the following table.

The loadability of the flip-flop outputs can be increased by connecting an external resistor in parallel with the built-in collector resistor of the corresponding output. This resistor has to be connected between the output terminal and $V_P$.
For each additional driven input, a parallel resistor of 51 k$\Omega \pm 5\%$ is required.
The total number of driven inputs is also specified in the following table.

x) Section "Time definitions" of "Circuit blocks 10-Series".

| flip-flop | | FF 12-A | | FF 12-B | | FF 12-C | | FF 12-D | |
|---|---|---|---|---|---|---|---|---|---|
| output terminal | | $\overline{Q}$ | Q | $\overline{Q}$ | Q | $\overline{Q}$ | Q | $\overline{Q}$ | Q |
| | | 3a | 2 | 7 | 8 | 9 | 3 | 5 | 4 |
| max. number of 10-series circuit blocks, that may be driven, provided each driven input represents a load: $-I_D$ = max. 1.1 mA and $-Q_T$ = max. 3.4 nC | $T_{amb}$ = min. 0 °C | 5 | 2 | 3 | 5 | 3 | 3 | 2 | 5 |
| | $T_{amb}$ = min. −25 °C | 5 | 2 | 3 | 3 | 3 | 3 | 2 | 5 |
| max. number of driven 10-series circuit blocks with external parallel collector resistor(s) | $T_{amb}$ = min. 0 °C | 6 | 5 | 5 | 5 | 5 | 4 | 4 | 6 |
| | $T_{amb}$ = min. −25 °C | 5 | 3 | 4 | 3 | 4 | 3 | 3 | 5 |

Wiring capacitance at each Q-output max. 175 pF

Output levels during counting

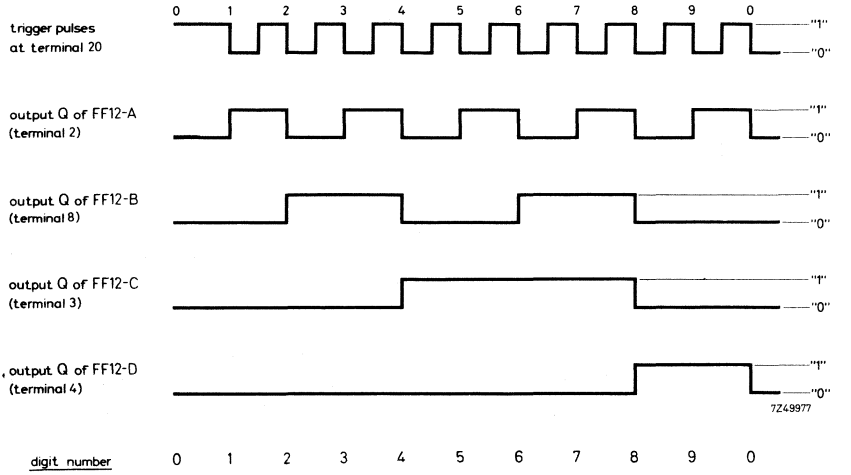



Fig.3

The output levels at the Q-outputs of each flip-flop are shown in Fig.3.
Note that when a Q-output is at "positive low" ("0") level the corresponding $\overline{Q}$-output is at "positive high" ("1") level and vice versa.
After 10 negative-going pulses at the trigger input terminal 20, the output Q of flip-flop D delivers the negative-going carry pulse for the next decade, while the decade counter has resumed its initial position, namely all Q-output terminals being at "positive low" level.
The relation between a digit number (output ID 10) and the corresponding state of each flip-flop is shown in the figure as well.

Numerical indicator tube driver section

The outputs $Q_0$ (terminal 11a) up to and including $Q_9$ (terminal 4a) of the ID 10 have to be connected to the pins $k_0$ up to and including $k_9$ of the numerical indicator tube ZM1000, ZM1020 or ZM1080. The anode of these tubes has to be connected via a resistor ($R_a$) to the high voltage power supply ($V_b$).

The current available at these 10 numerical outputs of the ID 10 can cope with the required cathode current $I_k$ of the indicator tubes ZM1000, ZM1020 and ZM1080, when the following conditions are observed:

- operating-temperature range
- power supply $V_b$ for ZM1000, ZM1020 and ZM1080
- anode series resistor $R_a$.

In the following graphs these data are specified.

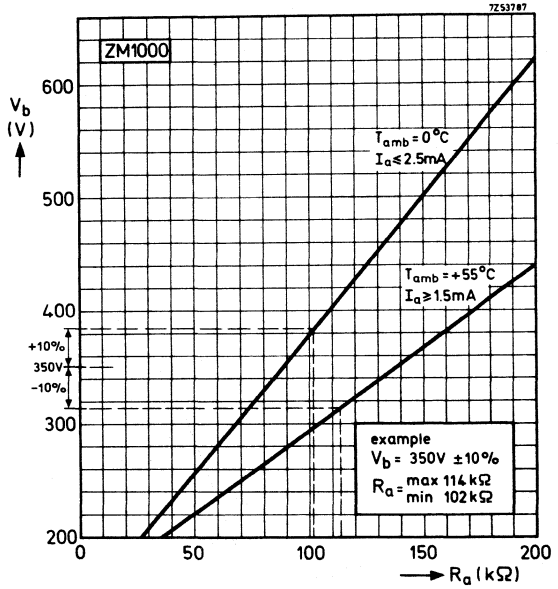



Fig.4

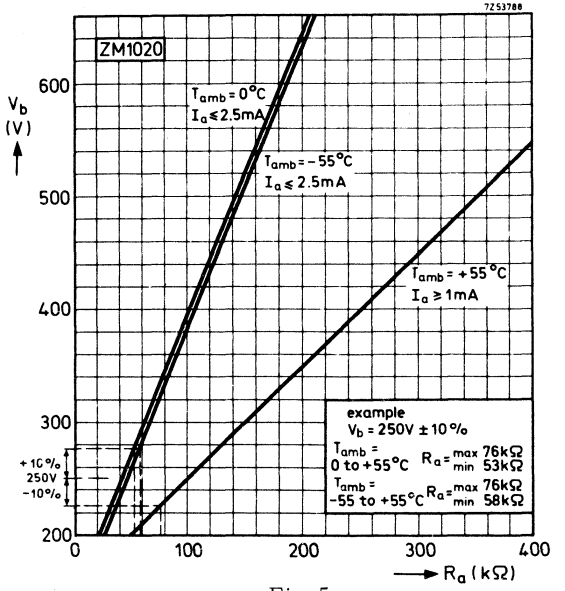



Fig. 5

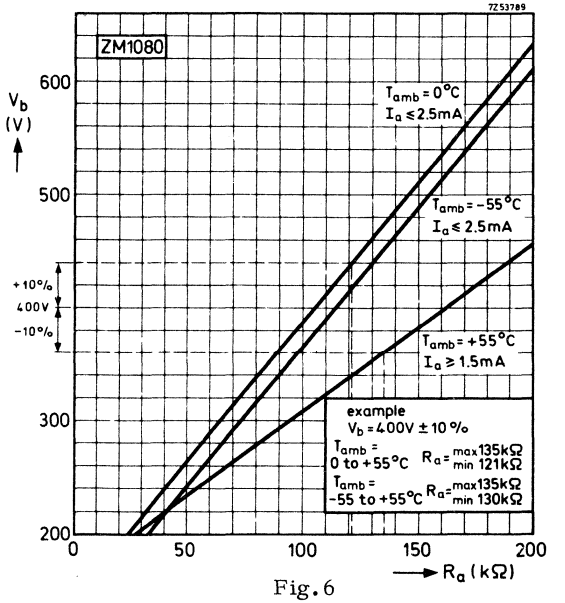



Fig. 6

Wiring capacitance at each Q-output of the ID10 max. 500 pF

# DECADE COUNTER DCA 10 B

## CIRCUIT DATA

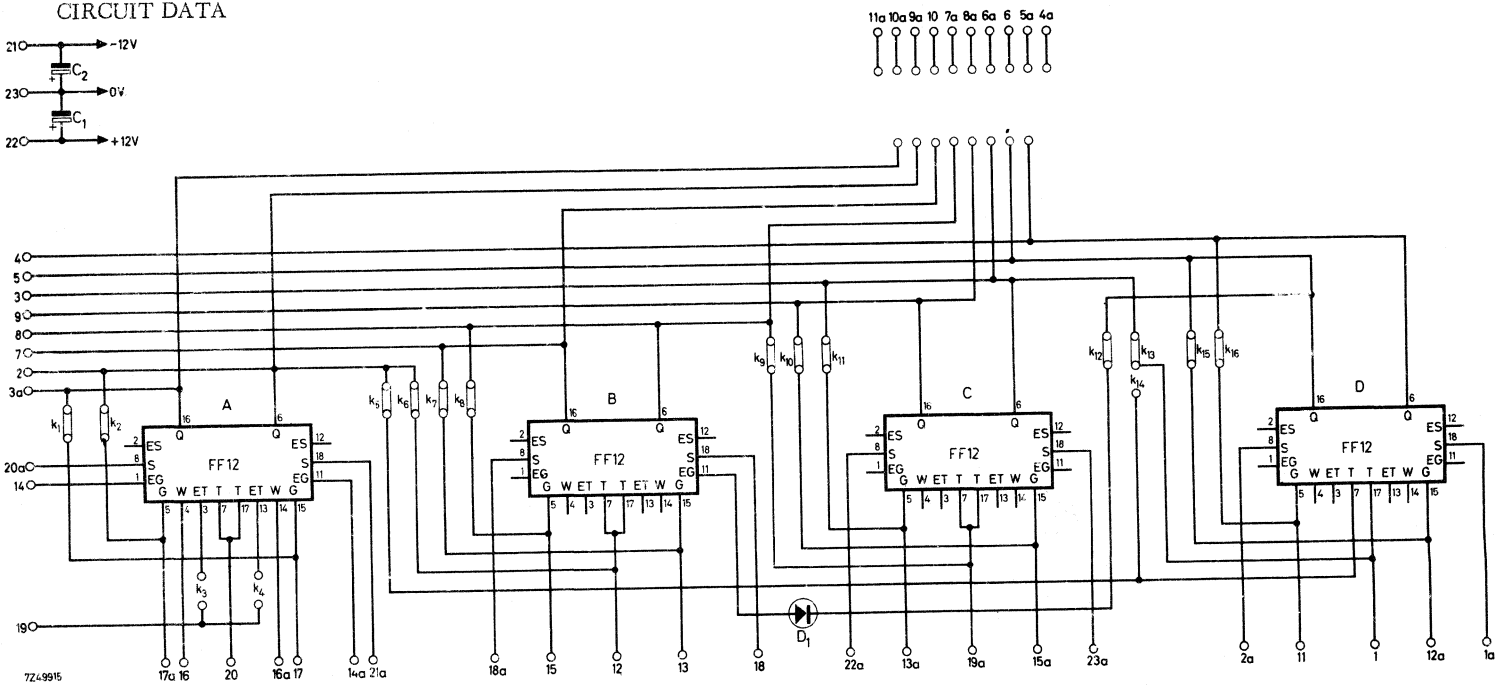



Fig. 7

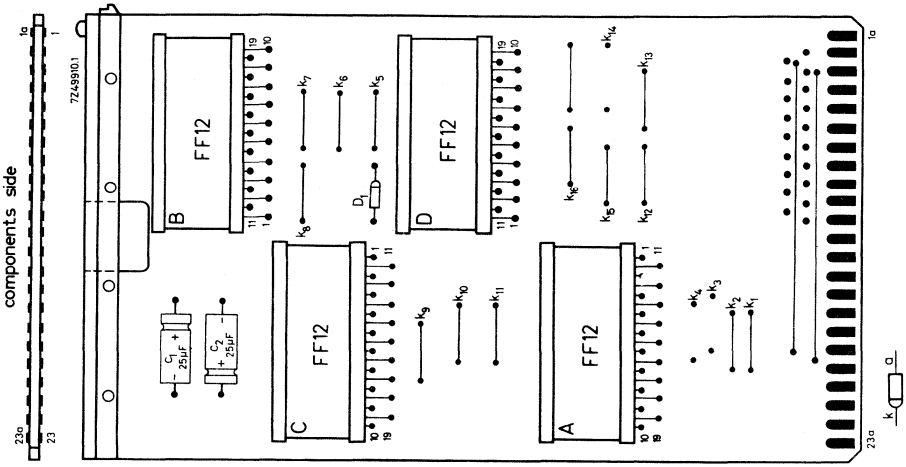



Fig.8. DCA10B

Terminals (Fig.8)

Similar to DCA 10 A, with exception of terminals 4a, 5a, 6, 6a, 7a, 8a, 9a, 10, 10a, 11a, which are inoperative.

INPUT REQUIREMENTS

Similar to DCA 10 A.

OUTPUT DATA (at $V_P$ = 11.4 V and $V_N$ = −12.6 V, unless specified differently)

In excess of the internal load, represented by the circuit blocks mounted on the printed-wiring board, the Q-outputs of each flip-flop in the decade counter may furthermore be loaded as specified in the table below.

| flip-flop | FF 12-A | | FF 12-B | | FF 12-C | | FF 12-D | |
|---|---|---|---|---|---|---|---|---|
| output terminal | $\overline{Q}$ | Q | $\overline{Q}$ | Q | $\overline{Q}$ | Q | $\overline{Q}$ | Q |
| | 3a | 2 | 7 | 8 | 9 | 3 | 5 | 4 |
| available direct current: $I_{QD}$ in mA | 7.1 | 6 | 7.1 | 6 | 7.1 | 6 | 6 | 7.1 |
| available transient charge when $V_Q$ changes from 2/3 Vp to 0.5 V in 1.5 µs: $Q_{QT}$ in nC | 25.8 | 22.4 | 25.8 | 22.4 | 25.8 | 22.4 | 25.8 | 25.8 |

For $T_{amb}$ = min. −25 °C the available direct current $I_{QD}$ has to be reduced with 1.6 mA and similarly the available transient charge $Q_{QT}$ with 5 nC.

CIRCUIT DATA

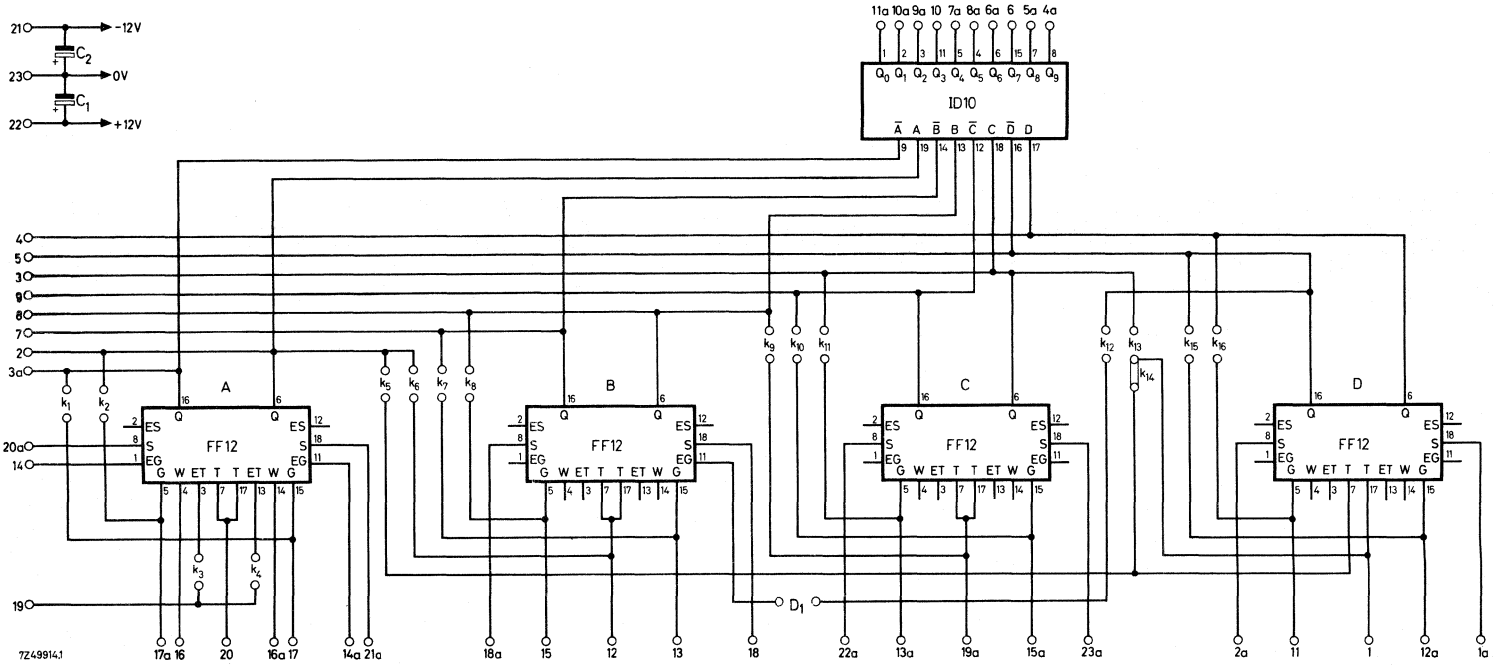



Fig. 9

Terminals (Fig.10)

Similar to DCA 10 A.

INPUT REQUIREMENTS

Similar to DCA 10 A, with the exception of the trigger input requirements due to the fact that in this version the trigger inputs of all the flip-flops have to be interconnected externally.
The input requirements for this common trigger line are:

Required direct current when $V_T$ = max. 0.3 V: $-I_{TD}$ = max. 4.4 mA

Required transient charge when $V_T$ changes from 2/3 $V_P$ to 0.5 V in 1.5 $\mu$s: $-Q_{TT}$ = max. 13.6 nC

OUTPUT DATA (at $V_P$ = 11.4 V and $V_N$ = −12.6 V, unless specified differently)

Buffer memory section

In excess of the internal load, represented by the circuit blocks mounted on the printed-wiring board, including the numerical indicator driver ID 10, the Q-outputs of each flip-flop in the buffer memory may furthermore be loaded as specified in the table below.
The loadability of the flip-flop outputs can be increased by putting an external resistor in parallel with the built-in collector resistor of the corresponding output. This resistor has to be connected between the output terminal and $V_P$.
For each additional driven input a parallel resistor of 51 kΩ ±5% is required.
The total number of driven inputs is also specified in the table below.

| flip-flop | | FF 12-A | | FF 12-B | | FF 12-C | | FF 12-D | |
|---|---|---|---|---|---|---|---|---|---|
| output terminal | | $\overline{Q}$ | Q | $\overline{Q}$ | Q | $\overline{Q}$ | Q | $\overline{Q}$ | Q |
| | | 3a | 2 | 7 | 8 | 9 | 3 | 5 | 4 |
| max. number of 10-series circuit blocks, that may be driven provided each driven input represents a load of $-I_D$ = max. 1.1 mA and $-Q_T$ = max. 3.4 nC | $T_{amb}$ = min. 0 °C | 6 | 6 | 4 | 7 | 4 | 4 | 4 | 6 |
| | $T_{amb}$ = min. −25 °C | 6 | 6 | 4 | 5 | 4 | 4 | 4 | 6 |
| max. number of driven 10-series circuit blocks, with external parallel collector resistor(s) | $T_{amb}$ = min. 0 °C | 7 | 7 | 6 | 7 | 6 | 6 | 6 | 7 |
| | $T_{amb}$ = min. −25 °C | 6 | 6 | 5 | 5 | 5 | 5 | 5 | 6 |

Numerical indicator tube driver section

Similar to DCA 10 A.

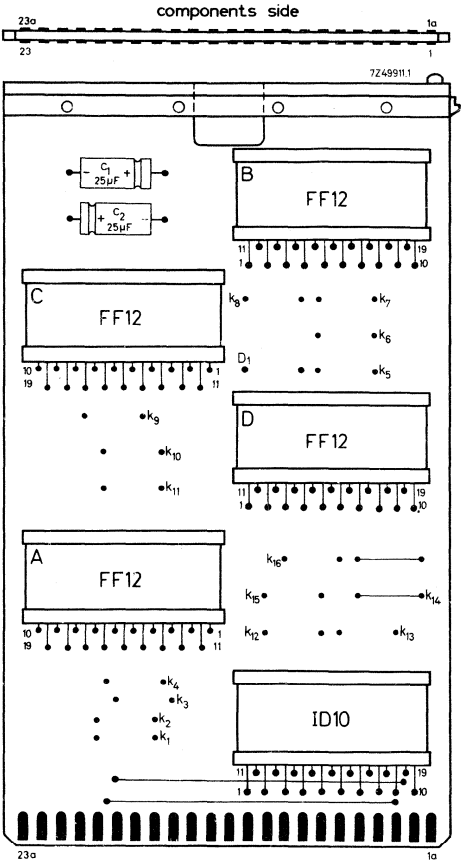



Fig.10. DCA 10 C

# BUFFER MEMORY DCA 10 D

## CIRCUIT DATA

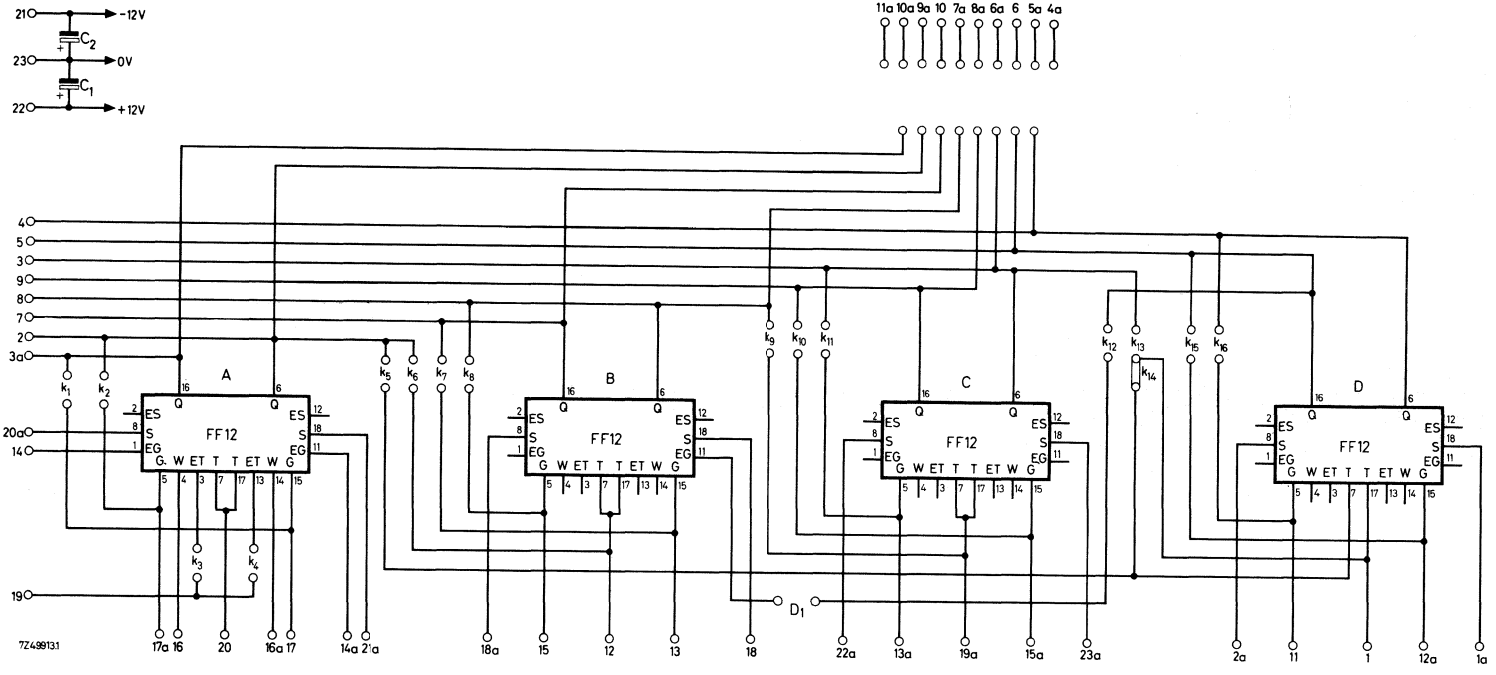



Fig.11

Terminals (Fig.12)

Similar to DCA 10 A, with the exception of terminals 4a, 5a, 6, 6a, 7a, 8a, 9a, 10, 10a and 11a, which are inoperative.

INPUT REQUIREMENTS

Similar to DCA 10 C.

OUTPUT DATA (at $V_P$ = 11.4 V and $V_N$ = −12.6 V, unless specified differently)

In excess of the internal load, represented by the circuit blocks mounted on the printed-wiring board, the Q-outputs of each flip-flop in the buffer memory may furthermore be loaded as specified in the table below.

| flip-flop | FF 12-A | | FF 12-B | | FF 12-C | | FF 12-D | |
|---|---|---|---|---|---|---|---|---|
| output terminal | $\overline{Q}$ | Q | $\overline{Q}$ | Q | $\overline{Q}$ | Q | $\overline{Q}$ | Q |
| | 3a | 2 | 7 | 8 | 9 | 3 | 5 | 4 |
| available direct current: $I_{QD}$ in mA | 8.2 | 8.2 | 8.2 | 8.2 | 8.2 | 8.2 | 8.2 | 8.2 |
| available transient charge when $V_Q$ changes from 2/3 $V_P$ to 0.5 V in 1.5 $\mu$s: $Q_{QT}$ in nC | 27 | 27 | 27 | 27 | 27 | 27 | 27 | 27 |

For $T_{amb}$ = min. −25 °C the available direct current $I_{QD}$ has to be reduced with 1.6 mA and similarly the available transient charge $Q_{QT}$ with 5 nC.

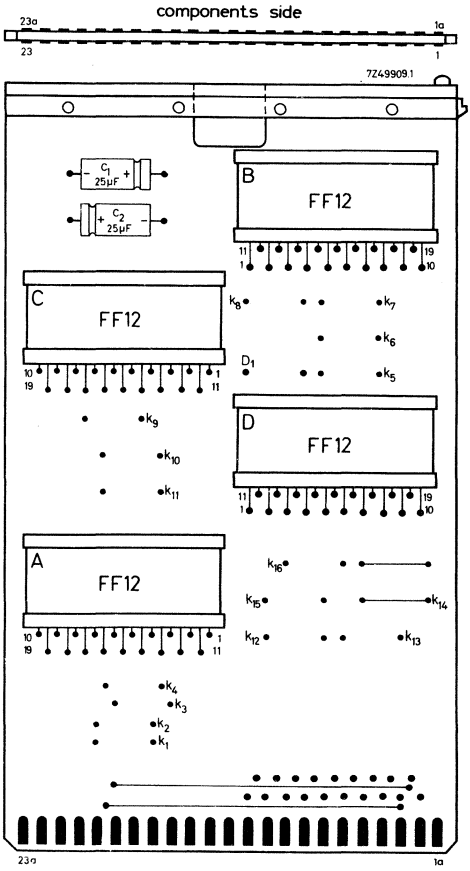



Fig.12. DCA 10 D

BINARY COUNTER DCA 10 E

CIRCUIT DATA

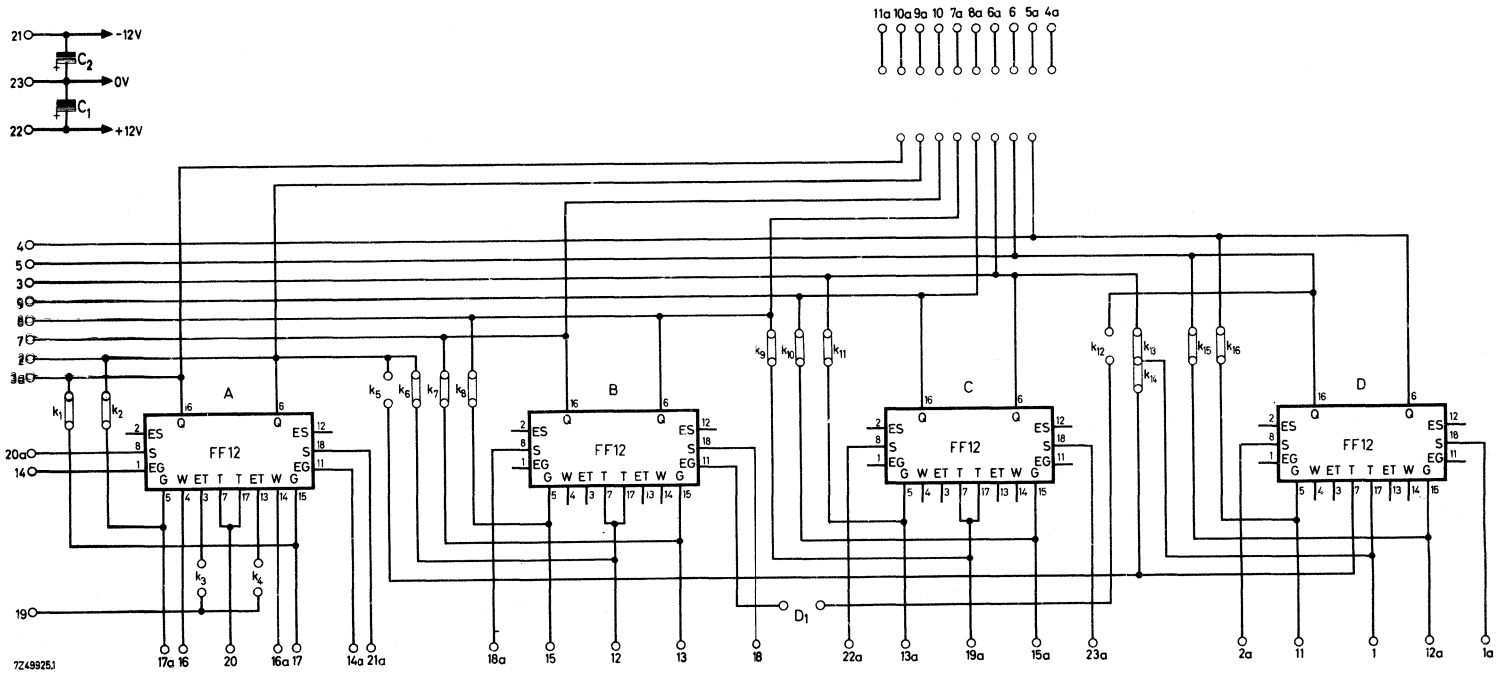



Fig.13

Terminals (Fig.14)

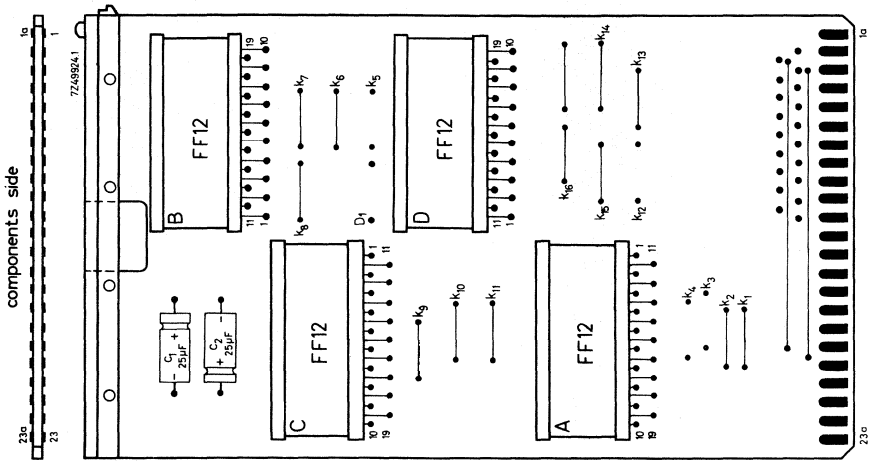



Fig.14. DCA 10 E

Similar to DCA 10 B.

INPUT REQUIREMENTS

Similar to DCA 10 A.

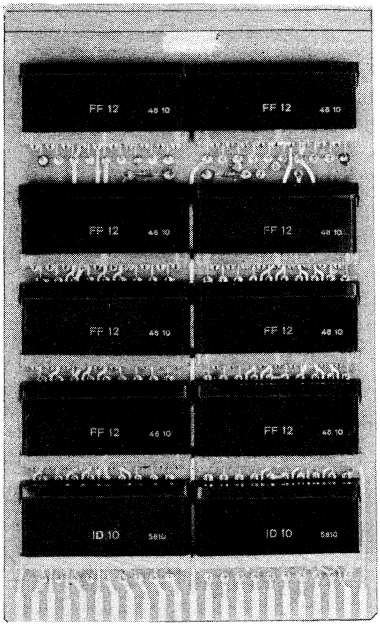
OUTPUT DATA (at $V_P$ = 11.4 V and $V_N$ = −12.6 V, unless specified differently)

In excess of the internal load, represented by the circuit blocks on the printed-wiring board, the Q-outputs of each flip-flop in the binary counter may furthermore be loaded as specified in the table below.

| flip-flop | FF 12-A | | FF 12-B | | FF 12-C | | FF 12-D | |
|---|---|---|---|---|---|---|---|---|
| output terminal | $\overline{Q}$ | Q | $\overline{Q}$ | Q | $\overline{Q}$ | Q | $\overline{Q}$ | Q |
| | 3a | 2 | 7 | 8 | 9 | 3 | 5 | 4 |
| available direct current: $I_{QD}$ in mA | 7.1 | 6 | 7.1 | 6 | 7.1 | 6 | 7.1 | 7.1 |
| available transient charge when $V_Q$ changes from 2/3 Vp to 0.5 V in 1.5 $\mu$s: $Q_{QT}$ in nC | 25.8 | 22.4 | 25.8 | 22.4 | 25.8 | 22.4 | 25.8 | 25.8 |

For $T_{amb}$ = min. −25 °C the available direct current $I_{QD}$ has to be reduced with 1.6 mA and similarly the available transient charge $Q_{QT}$ with 5 nC.

# DUAL DECADE COUNTER AND NUMERICAL INDICATOR TUBE DRIVER ASSEMBLY




RZ 22603-9

This assembly consists of eight circuit blocks FF 12, with or without a circuit block ID 10, mounted on a printed-wiring board. It is available in two versions.

- 2.DCA 11 A, catalog number 2722 009 02051.

  This assembly contains eight flip-flops FF 12, intended to be used as a dual decade counter, operating in the 1-2-4-8 code, each decade provided with a common reset line. It contains also two numerical indicator tube drivers ID 10, providing the BCD - to decimal decoding - and driving circuits for the numerical indicator tube ZM 1000, ZM 1020 or ZM 1080.
  The circuit diagram and the required interconnections are shown in Figs. 1 and 2.

- 2.DCA 11 B, catalog number 2722 009 02061.

  This assembly is identical to the 2.DCA 11 A, but without the circuit blocks ID 10 mounted on the board. The lay-out of the printed-wiring board allows the mounting of the ID 10's separately (see Figs. 7 and 8).

The bare printed-wiring board (catalog number 4322 026 38710), provided with plated-through holes and double-sided goldplated contacts, is made of glass-epoxy material. Moreover the printed-wiring board is delivered with an extractor and a locking device.
With the mating connector (catalog number 2422 020 52591), not supplied with the assembly, the printed-wiring board of standard dimensions (121.8 mm x 207.0 mm x 1.6 mm) can be used directly in the standard mounting chassis (catalog number 4322 026 38240).
The circuit blocks are secured to the printed-wiring board by means of locking caps (catalog number 4322 026 32150).

| | | |
|---|---|---|
| Counting rate | | max. 30 kHz |
| Ambient-temperature range | | |
| | operating | −25 to +55 °C<br>below 0 °C : derated output data |
| | storage | −55 to +75 °C |
| Weight | | approx. 500 g |

The data specified below apply to the 2.DCA 11 A in particular.
For the sake of simplicity for the version 2.DCA 11 B only data are specified separately, which differ from those of the 2.DCA 11 A.

# DUAL DECADE COUNTER AND NUMERICAL INDICATOR TUBE DRIVER 2.DCA 11 A

## CIRCUIT DATA

For circuit diagram see next pages.

D126

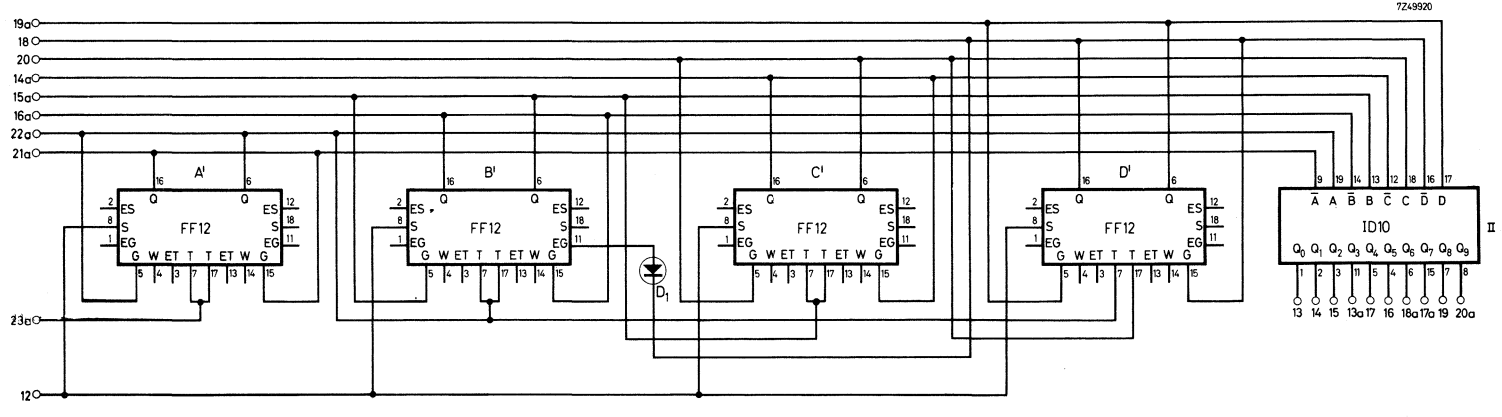



Fig.1a. 2.DCA 11 A

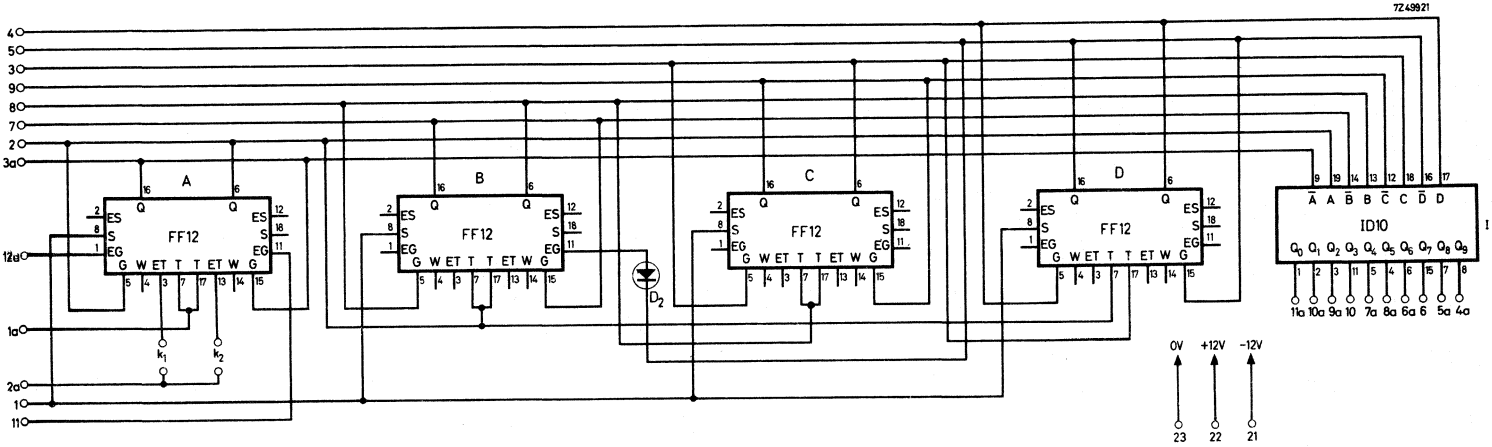



Fig.1b. 2.DCA 11 A

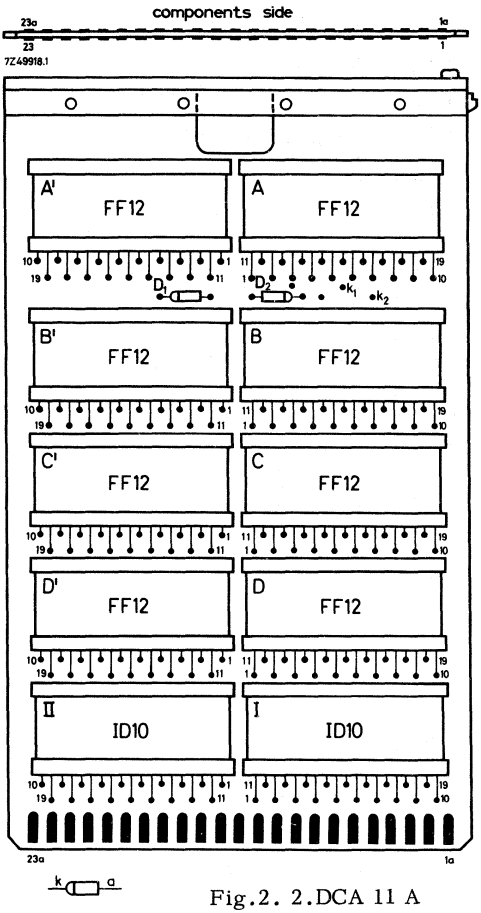



Fig.2. 2.DCA 11 A

Terminals

1 = common reset input S of decade counter I
2 = output Q of flip-flop A
3 = output Q of flip-flop C
4 = output Q of flip-flop D
5 = output $\overline{Q}$ of flip-flop D
6 = numerical output 7 of ID 10-I
7 = output $\overline{Q}$ of flip-flop B
8 = output Q of flip-flop B
9 = output $\overline{Q}$ of flip-flop C
10 = numerical output 3 of ID 10-I
11 = extension gate input EG of flip-flop A

12 = common reset input S of decade II
13 = numerical output 0 of ID 10-II
14 = numerical output 1 of ID 10-II
15 = numerical output 2 of ID 10-II
16 = numerical output 5 of ID 10-II
17 = numerical output 4 of ID 10-II
18 = output $\overline{Q}$ of flip-flop D'
19 = numerical output 8 of ID 10-II
20 = output Q of flip-flop C'
21 = common negative supply −12 V
22 = common positive supply +12 V
23 = common supply 0 V

1a = trigger input T of flip-flop A
2a = additional trigger input T of flip-flop A
3a = output $\overline{Q}$ of flip-flop A
4a = numerical output 9 of ID 10-I
5a = numerical output 8 of ID 10-I
6a = numerical output 6 of ID 10-I
7a = numerical output 4 of ID 10-I
8a = numerical output 5 of ID 10-I
9a = numerical output 2 of ID 10-I
10a = numerical output 1 of ID 10-I
11a = numerical output 0 of ID 10-I
12a = extension gate input EG of flip-flop A
13a = numerical output 3 of ID 10-II
14a = output $\overline{Q}$ of flip-flop C'
15a = output Q of flip-flop B'
16a = output $\overline{Q}$ of flip-flop B'
17a = numerical output 7 of ID 10-II
18a = numerical output 6 of ID 10-II
19a = output Q of flip-flop D'
20a = numerical output 9 of ID 10-II
21a = output $\overline{Q}$ of flip-flop A'
22a = output Q of flip-flop A'
23a = trigger input T of flip-flop A'

Power supply

Terminal 21: $V_N = -12\ V \pm 5\%$, $-I_N = 8\ mA$
22: $V_P = +12\ V \pm 5\%$, $I_P = 60\ mA$
23: $V_E = 0\ V$ common

} The current values are nominal

INPUT REQUIREMENTS (at $V_P$ = 11.4 V and $V_N$ = −12.6 V unless specified differently)

Set/reset input (S-terminals)

The flip-flops of the decades I and II are reset simultaneously at the terminals 1 and 12 respectively, when a "positive low" voltage (between 0 V and 0.3 V) is applied to the corresponding S-terminal.

| | | | | | |
|---|---|---|---|---|---|
| Required direct current | $-I_{SD}$ | = min. | 7.8 | mA | |
| Required transient charge when $V_S$ changes from 2/3 $V_P$ to 0.5 V in 1.5 μs | $-Q_{ST}$ | = max. | 11.2 | nC | |

When the decade is not reset, the voltage $V_S$ must be kept between max. $V_P$ and min. 2/3 $V_P$.

Time data

| | | | | | |
|---|---|---|---|---|---|
| Pulse duration | $t_p$ | = min. | 8 | μs | See point 4* |
| Recovery time | $t_{rec}$ | = min. | 15 | μs | |
| Time delay between S- and T-signal | $t_{st}$ | = min. | 15 | μs | See point 5* |

Extension gate input (EG-terminals)

A d.c. voltage level can be applied to the EG-terminals 12a and 11 via diodes type OA 95. A "positive low" voltage closes the gate, whilst a "positive high" voltage (between 2/3 $V_P$ and $V_P$) opens the gate.

Gate open

| | | | | | |
|---|---|---|---|---|---|
| Voltage | $V_G$ | = min. | 2/3 | $V_P$ | |
| | | = max. | | $V_P$ | |

Gate closed

| | | | | | |
|---|---|---|---|---|---|
| Voltage | $V_G$ | = min. | 0 | V | |
| | | = max. | 0.3 | V | |
| Required direct current | $-I_{GD}$ | = max. | 1.1 | mA | |
| Required transient charge when $V_G$ changes from 2/3 $V_P$ to 0.5 V in 1.5 μs | $-Q_{GT}$ | = max. | 1.2 | nC | |

Time data

| | | | | | |
|---|---|---|---|---|---|
| Trigger gate setting time | $t_{gs}$ | = min. | 29 | μs | See point 6* |
| Trigger gate inhibiting time | $t_{gi}$ | = min. | 29 | μs | See point 7* |

* Section "Time definitions" of "Circuit blocks 10-Series".

Trigger input (T-terminals)

A negative-going voltage step or trigger pulse is applied to the interconnected trigger inputs T of flip-flops A and A' (terminals 23a and 1a respectively). Decade counter I can be provided with a second trigger input (terminal 2a). Two diodes BAY 38 have to be mounted on the printed-wiring board.
Each trigger pulse applied to the terminal T switches the decade counter, provided that the G-inputs (EG-inputs via diode) are left floating or at min. 2/3 $V_P$ (gate open).

| | | Gate open | Gate closed |
|---|---|---|---|
| | $V_G$ | = min. 2/3 $V_P$<br>= max. $V_P$ | = min. 0 V<br>= max. 0.3 V |
| Required direct current when $V_T$ = max. 0.3 V | $-I_{TD}$ | = max. 1.1 mA | = 0 mA |
| Required transient charge when $V_T$ changes from 2/3 $V_P$ to 0.5 V in 1.5 $\mu$s | $-Q_{TT}$ | = max. 3.4 nC | = 0 nC |
| Time data | | | |
| Fall time | $t_f$ | = max. 1.5 $\mu$s | See point 3 * |
| Pulse duration | $t_p$ | = min. 2 $\mu$s | |
| Trigger gate setting time | $t_{gs}$ | = min. 29 $\mu$s | |

OUTPUT DATA (at $V_P$ = 11.4 V and $V_N$ = -12.6 V, unless specified differently)

Decade counter section

In excess of the internal load, represented by the circuit blocks mounted on the printed-wiring board, including the numerical indicator tube driver ID 10, the Q-outputs of each flip-flop in the decade counter may furthermore be loaded as specified in the following table.

The loadability of the flip-flop outputs can be increased by connecting an external resistor in parallel with the built-in collector resistor of the corresponding output. This resistor has to be connected between the output terminal and $V_P$. For each additional driven input, a parallel resistor of 51 k$\Omega \pm 5\%$ is required. The total number of driven inputs is also specified in the following table.

Wiring capacitance at each Q-output max. 175 pF

* Section "Time definitions" of "Circuit blocks 10-series".

| flip-flop | | FF 12-A(A') | | FF 12-B(B') | | FF 12-C(C') | | FF 12-D(D') | |
|---|---|---|---|---|---|---|---|---|---|
| output terminal | | $\overline{Q}$ | Q | $\overline{Q}$ | Q | $\overline{Q}$ | Q | $\overline{Q}$ | Q |
| | | 3a(21a) | 2(22a) | 7(16a) | 8(15a) | 9(14a) | 3(20) | 5(18) | 4(19a) |
| max. number of 10-series circuit blocks, that may be driven, provided each driven input represents a load of $-I_D$ = max. 1.1 mA and $-Q_T$ = max. 3.4 nC | $T_{amb}$ = min. 0 °C | 5 | 2 | 3 | 5 | 3 | 3 | 2 | 5 |
| | $T_{amb}$ = min. −25 °C | 5 | 2 | 3 | 3 | 3 | 3 | 2 | 5 |
| max. number of driven 10-series circuit blocks, with external parallel collector resistor(s) | $T_{amb}$ = min. 0 °C | 6 | 5 | 5 | 5 | 5 | 4 | 4 | 6 |
| | $T_{amb}$ = min. −25 °C | 5 | 3 | 4 | 3 | 4 | 3 | 3 | 5 |

Output levels during counting

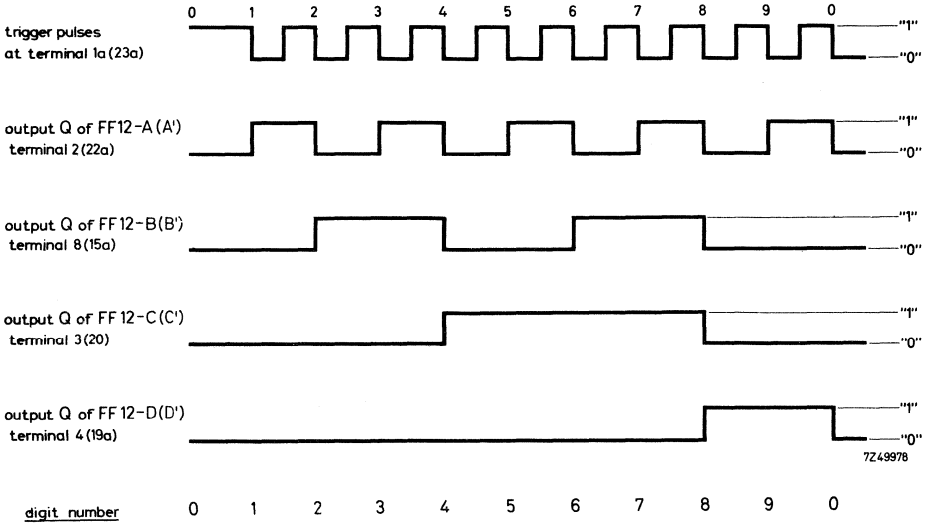



Fig.3

The output levels at the Q-outputs of each flip-flop are shown in figure 3.
Note that, when a Q-output is at "positive low" ("0") level the corresponding $\overline{Q}$-output is at "positive high" ("1") level and vice versa.
After 10 negative-going pulses at the trigger input terminal 1a (23a) the output Q of flip-flop D (D') delivers the negative-going carry pulse for the next decade, while the decade counter has resumed its initial position, namely all Q-output terminals being at "positive low" level.
The relation between a digit number (output ID 10) and the corresponding state of each flip-flop is shown in figure 3 as well.

Numerical indicator tube driver section

The outputs $Q_0$ (terminals 11a and 13) up to and including $Q_9$ (terminals 4a and 20a) of the ID 10-I and ID 10-II respectively have to be connected to the pins $k_0$ up to and including $k_9$ of the corresponding numerical indicator tube ZM 1000, ZM 1020 or ZM 1080. The anode of these tubes has to be connected via a resistor ($R_a$) to the high voltage power supply ($V_b$).
The current available at these ten numerical outputs of the ID 10 can cope with the required cathode current $I_k$ of the indicator tubes ZM 1000, ZM 1020 and ZM 1080, when the following conditions are observed:
- operating-temperature range
- power supply $V_b$ for ZM 1000, ZM 1020 and ZM 1080
- anode series resistor $R_a$.

In the following graphs these data are specified.

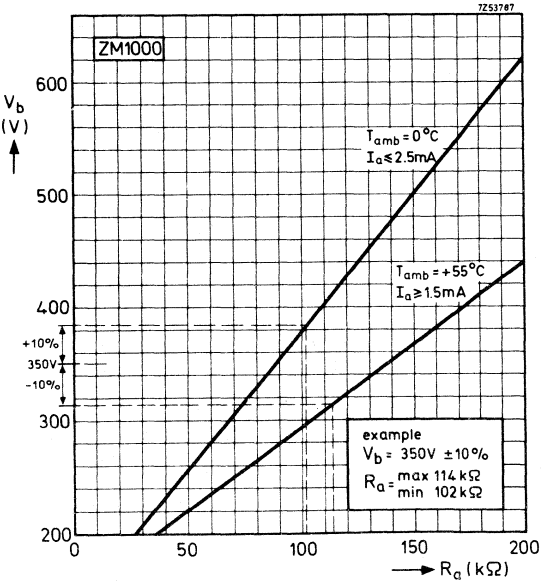



Fig.4

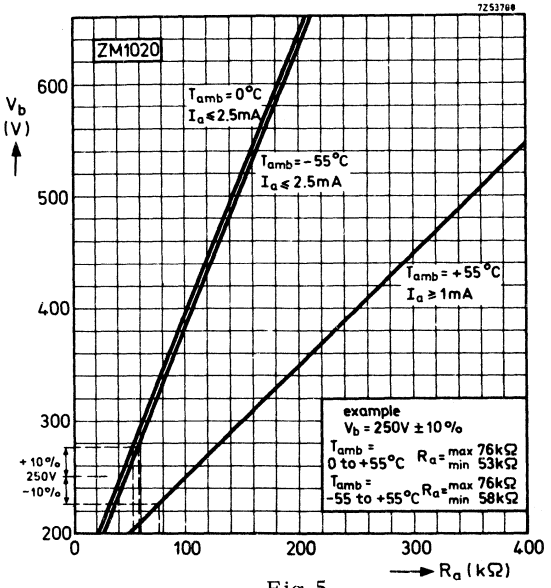



Fig.5

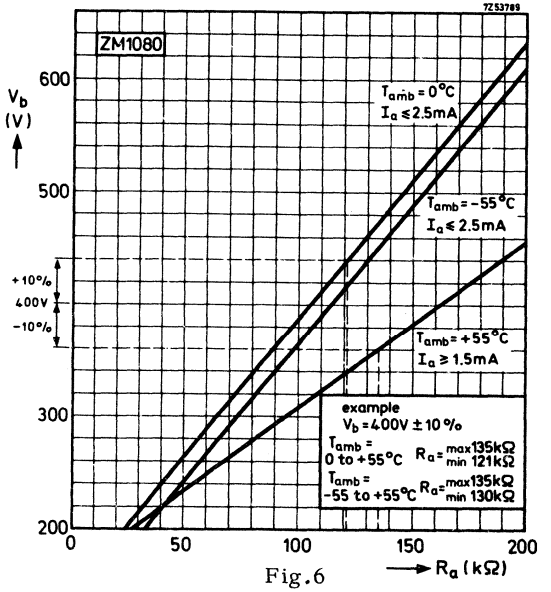



Fig.6

Wiring capacitance at each Q-output of the ID 10 max. 500 pF

DUAL DECADE COUNTER 2.DCA 11 B

CIRCUIT DATA

For circuit diagram see next pages.

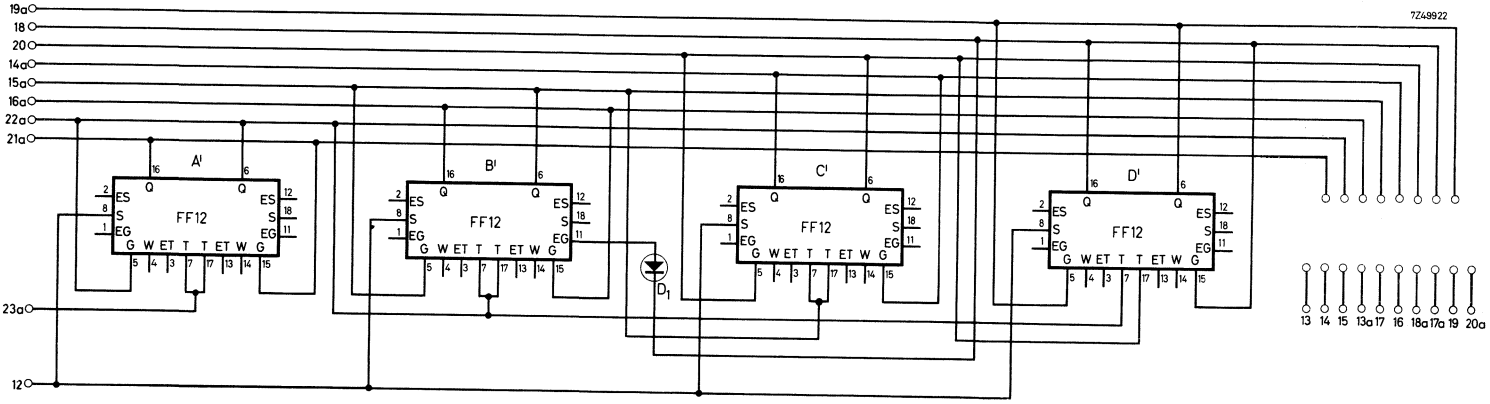



Fig.7a. 2.DCA 11 B

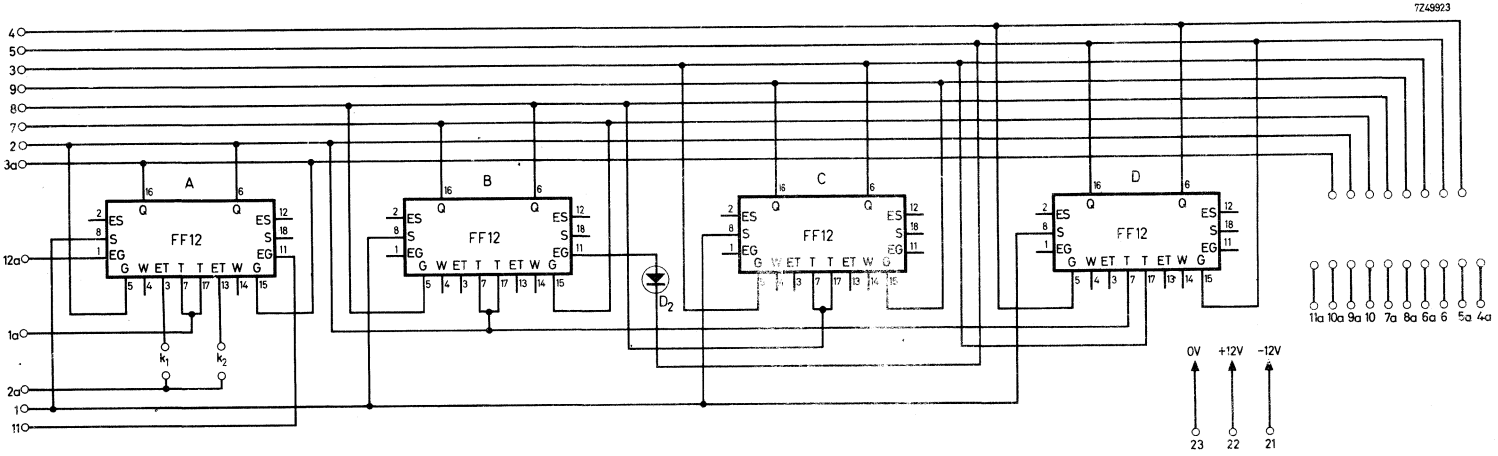



Fig.7b. 2.DCA 11 B

Terminals (Fig.8)

Similar to 2.DCA 11 A, with the exception of terminals 4a, 5a, 6, 6a, 7a, 8a, 9a, 10, 10a, 11a, 13, 13a, 14, 15, 16, 17, 17a, 18a, 19 and 20a, which are inoperative.

INPUT REQUIREMENTS

Similar to 2.DCA 11 A.

OUTPUT DATA (at $V_P$ = 11.4 V and $V_N$ = −12.6 V, unless specified differently)

In excess of the internal load, represented by the circuit blocks mounted on the printed-wiring board, the Q-outputs of each flip-flop in the decade counter may furthermore be loaded as specified in the table below.

| flip-flop | FF 12-A (A') | | FF 12-B (B') | | FF 12-C (C') | | FF 12-D (D') | |
|---|---|---|---|---|---|---|---|---|
| output terminal | $\overline{Q}$ | Q | $\overline{Q}$ | Q | $\overline{Q}$ | Q | $\overline{Q}$ | Q |
| | 3a(21a) | 2(22a) | 7(16a) | 8(15a) | 9(14a) | 3(20) | 5(18) | 4(19a) |
| available direct current: min. $I_{QD}$ in mA | 7.1 | 6 | 7.1 | 6 | 7.1 | 6 | 6 | 7.1 |
| available transient charge when $V_Q$ changes from 2/3 $V_P$ to 0.5 V in 1.5 μs: min. $Q_{QT}$ in nC | 25.8 | 22.4 | 25.8 | 22.4 | 25.8 | 22.4 | 25.8 | 25.8 |

For $T_{amb}$ = min. −25 °C the available direct current $I_{QD}$ has to be reduced with 1.6 mA and similarly the available transient charge $Q_{QT}$ with 5 nC.

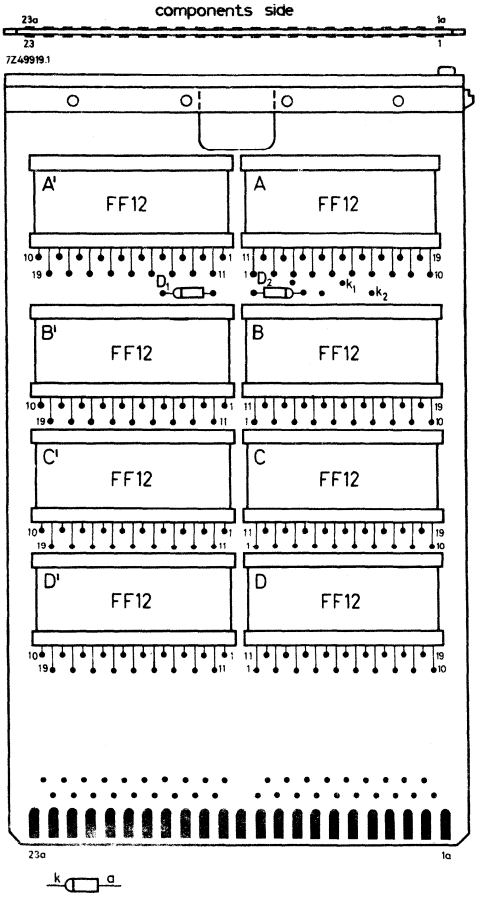
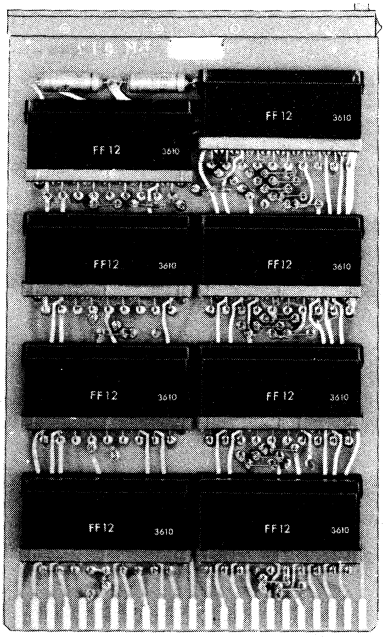



Fig.8. 2.DCA 11 B

# DUAL DECADE COUNTER ASSEMBLY




RZ 22603-10

This assembly consists of eight circuit blocks FF 12 mounted on a printed-wiring board. It is available in three versions.

- 2. DCA 12 A, catalog number 2722 009 02071

  This assembly contains eight flip-flops FF 12, intended to be used as a dual decade counter, operating in the 1 - 2 - 4 - 8 code.
  The circuit diagram and the required interconnections made on the printed-wiring board are shown in Figs. 1 and 2.

- 2. DCA 12 B, catalog number 2722 009 02081.

  This assembly contains four flip-flops FF12, intended for use as a decade counter operating in the 1 - 2 - 4 - 8 code, and four flip-flops FF 12 intended for use as a buffer memory.
  The circuit diagram and the required interconnections made on the printed-wiring board are shown in Figs. 4 and 5.

The contents of the decade counter can be stored in the buffer memory by means of one trigger pulse on the common trigger line of the buffer memory section (terminal 4).
When the contents of the buffer memory has to be numerically indicated the numerical indicator tube driver ID 10 for ZM 1000, ZM 1020 and ZM 1080 can be connected directly to the Q-output terminals of the four flip-flops forming the buffer memory.

- 2. DCA 12 C, catalog number 2722 009 02091.

This assembly contains two chains of four flip-flops FF 12, intended to be used either as binary counters, scalers of 16 or as a binary scaler of 256, the latter when both chains are put in series. The circuit diagram and the required interconnections made on the printed-wiring board are shown in Figs.6 and 7.
To obtain a scaler of maximum 256 the required interconnection between terminal 9a and 19 has to be made externally.
For reset purposes of all eight flip-flops, terminals 3 and 20 have to be interconnected externally.

All these versions are provided with the capacitors $C_1$ and $C_2$, which filter the supply voltages from noise. These capacitors are mounted on the printed-wiring board.

The bare printed-wiring board (catalog number 4322 026 38720), provided with plated-through holes and double-sided gold plated contacts, is made of glass-epoxy material. Moreover the printed-wiring board is delivered with an extractor and a locking device.
With the mating connector (catalog number 2422 020 52591), not supplied with the assembly, the printed-wiring board of standard dimensions (121.8 mm x 207.0 mm x 1.6 mm) can be used directly in the standard mounting chassis (catalog number 4322 026 38240).

The circuit blocks are secured to the printed-wiring board by means of locking caps (catalog number 4322 026 32150).

| | |
|---|---|
| Counting rate | max. 30 kHz |
| Ambient-temperature range | |
| operating | −25 to +55 °C<br>below 0 °C: derated output data |
| storage | −55 to +75 °C |
| Weight | approx. 450 g |

The data specified below apply to the 2.DCA 12 A in particular.
For the sake of simplicity for the versions 2.DCA 12 B and 2.DCA 12 C only data are specified separately, which differ from those of the 2.DCA 12 A.

DUAL DECADE COUNTER 2.DCA 12 A

CIRCUIT DATA

For circuit diagram see next pages.

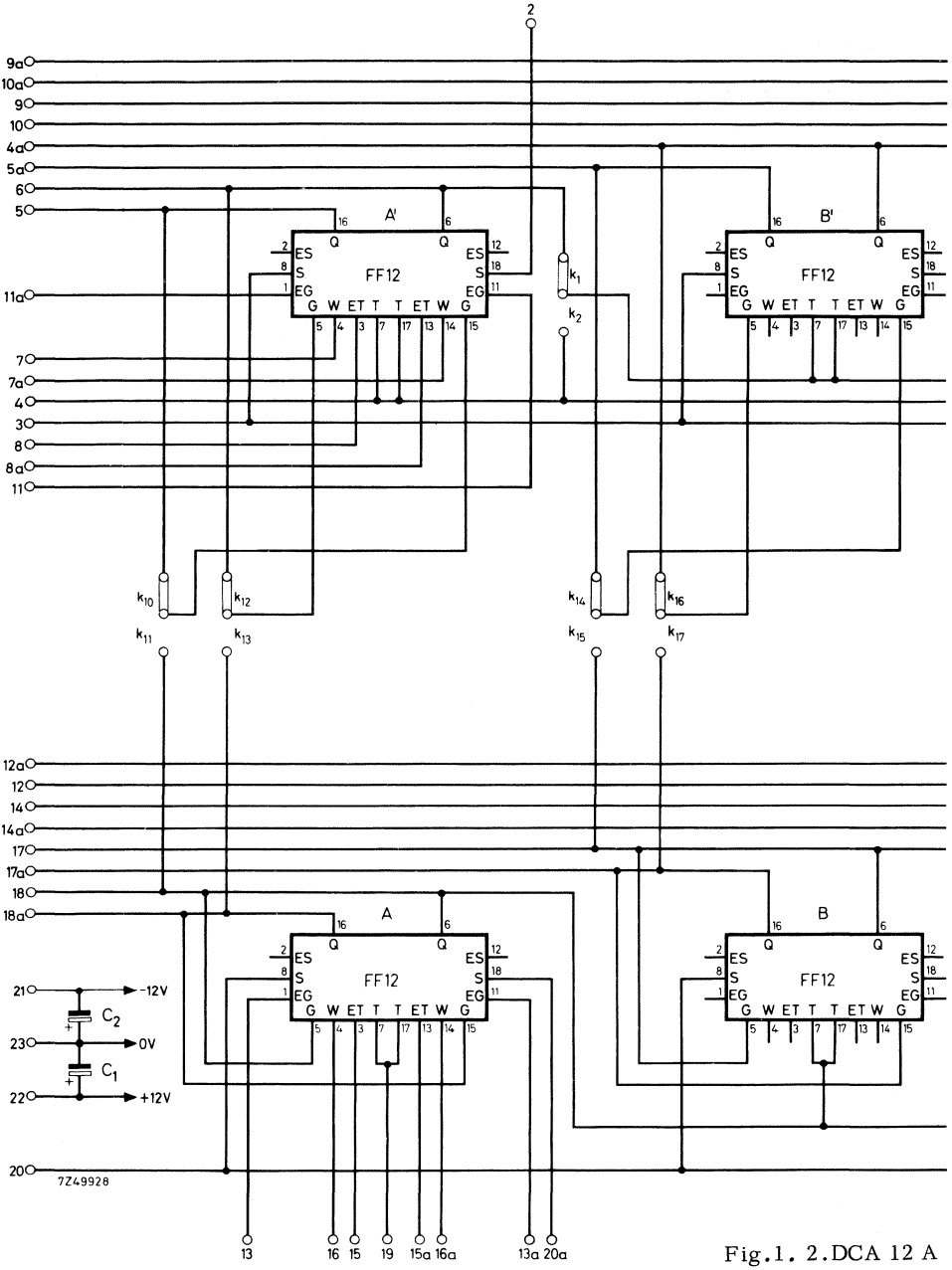



Fig.1. 2.DCA 12 A

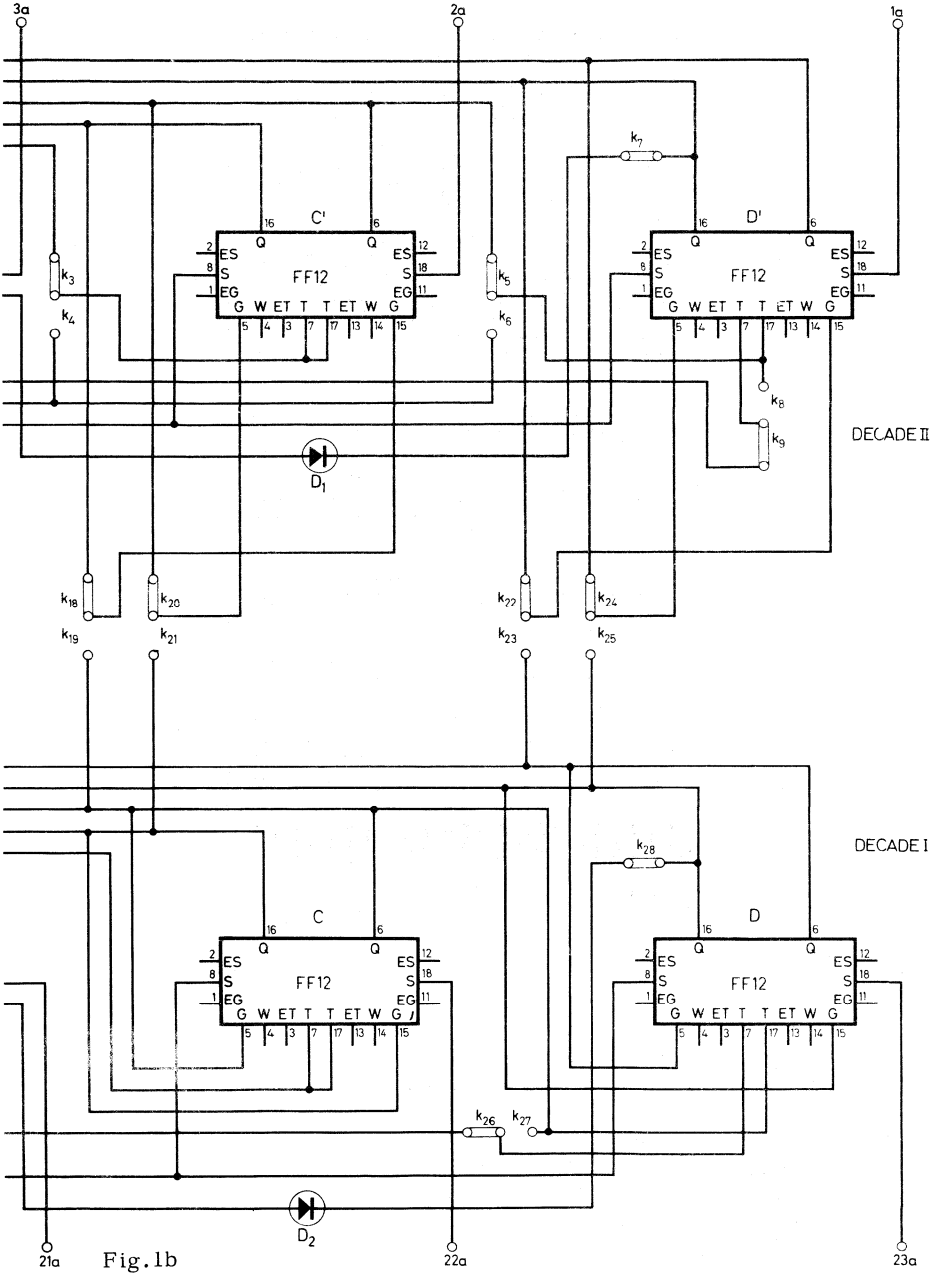

3a
2a
1a
C'
D'
C
D
FF12
ES
S
EG
Q
G W ET T T ET W G
k3
k4
k5
k6
k7
k8
k9
k18
k19
k20
k21
k22
k23
k24
k25
k26
k27
k28
D1
D2
DECADE II
DECADE I
21a
22a
23a

Fig.1b

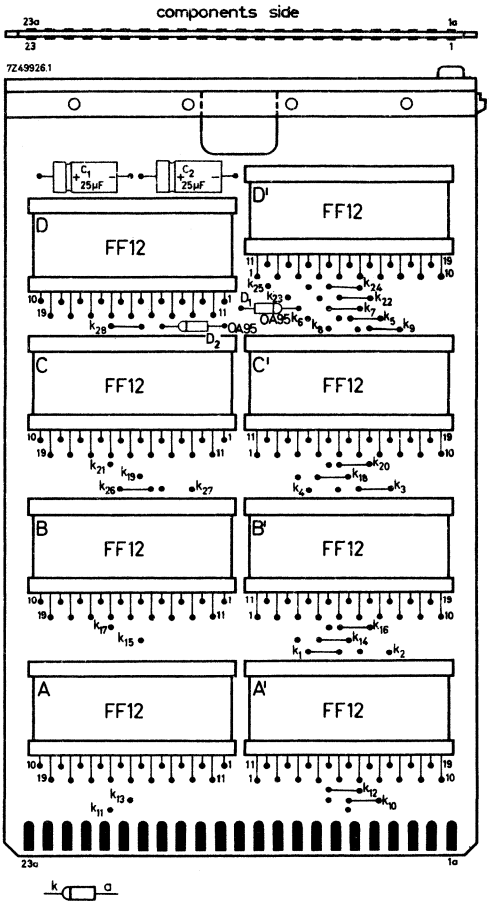



Fig.2. 2.DCA 12 A

Terminals

1 = not connected
2 = set input S of flip-flop A'
3 = common reset input S of decade II
4 = trigger input T of decade II or buffer memory
5 = output $\overline{Q}$ of flip-flop A'
6 = output Q of flip-flop A'
7 = base input W of flip-flop A'
8 = extension trigger input ET of flip-flop A'
9 = output Q of flip-flop C'
10 = output $\overline{Q}$ of flip-flop C'

11 = extension gate input EG of flip-flop A'
12 = output $\overline{Q}$ of flip-flop D
13 = extension gate input EG of flip-flop A
14 = output Q of flip-flop C
15 = extension trigger input ET of flip-flop A
16 = base input W of flip-flop A
17 = output Q of flip-flop B
18 = output Q of flip-flop A
19 = trigger input T of decade counter I
20 = common reset input S of decade counter I
21 = common negative supply −12 V
22 = common positive supply +12 V
23 = common supply 0 V

1a = set input S of flip-flop D'
2a = set input S of flip-flop C'
3a = set input S of flip-flop B'
4a = output Q of flip-flop B'
5a = output $\overline{Q}$ of flip-flop B'
6a = not connected
7a = base input W of flip-flop A'
8a = extension trigger input ET of flip-flop A'
9a = output Q of flip-flop D'
10a = output $\overline{Q}$ of flip-flop D'
11a = extension gate input EG of flip-flop A'
12a = output Q of flip-flop D
13a = extension gate input EG of flip-flop A
14a = output $\overline{Q}$ of flip-flop C
15a = extension trigger input ET of flip-flop A
16a = base input W of flip-flop A
17a = output $\overline{Q}$ of flip-flop B
18a = output $\overline{Q}$ of flip-flop A
19a = not connected
20a = set input S of flip-flop A
21a = set input S of flip-flop B
22a = set input S of flip-flop C
23a = set input S of flip-flop D

Power supply

Terminal 21 : $V_N$ = −12 V + 5 %, $-I_N$ = 8.5 mA
22 : $V_P$ = +12 V ± 5 %, $I_P$ = 60 mA
23 : $V_E$ = 0 V common

} The current values are nominal

INPUT REQUIREMENTS (at $V_p$ = 11.4 V and $V_N$ = −12.6 V unless specified differently)

Set/reset inputs (S-terminals)

For reset- or preset purposes a "positive low" voltage $V_S$ is required between 0 V and 0.3 V, otherwise this voltage must be kept between Vp and 2/3 Vp.

Common reset (terminals 3 and 20)

With one pulse at terminals 3 or 20 all flip-flops in the decade will be reset simultaneously.

| | | | | |
|---|---|---|---|---|
| Required direct current | $-I_{SD}$ | = min. 7.8 | mA | |
| Required transient charge when $V_S$ changes from 2/3 Vp to 0.5 V in 1.5 µs | $-Q_{ST}$ | = min. 11.2 | nC | |
| Time data | | | | |
| Pulse duration | $t_p$ | = min. 8 | µs | See point 4* |
| Recovery time | $t_{rec}$ | = min. 15 | µs | |
| Time delay between S- and T-signal | $t_{st}$ | = min. 15 | µs | See point 5* |

Individual flip-flop preset (terminals 2, 3a, 2a, 1a and 20a, 21a, 22a, 23a)

For this purpose one S-input of each flip-flop in the decade has been brought out.

| | | | |
|---|---|---|---|
| Required direct current | $-I_{SD}$ | = max. 1.95 | mA |
| Required transient charge when $V_S$ changes from 2/3 $V_p$ to 0.5 V in 1.5 µs | $-Q_{ST}$ | = max. 2.8 | nC |

Extension gate input (EG-terminals)

A d.c. voltage level can be applied to the EG-terminals 13a and 13 of flip-flop FF 12-A and 11 and 11a of flip-flop FF 12-A', via a diode type OA 95.
A "positive low" voltage closes the gate, whilst a "positive high" voltage (between 2/3 Vp and Vp) opens the gate.

| | | | |
|---|---|---|---|
| Gate open | | | |
| Voltage | $V_G$ | = min. 2/3 | $V_P$ |
| | | = max. | $V_P$ |

* Section "Time definitions" of "Circuit blocks 10-Series".

Gate closed

| | | | | |
|---|---|---|---|---|
| Voltage | $V_G$ | = min. 0 / max. 0.3 | V / V | |
| Required direct current | $-I_{GD}$ | = max. 1.1 | mA | |
| Required transient charge when $V_G$ changes from 2/3 $V_p$ to 0.5 V in 1.5 $\mu$s | $-Q_{GT}$ | = max. 1.2 | nC | |

Time data

| | | | | |
|---|---|---|---|---|
| Trigger gate setting time | $t_{gs}$ | = min. 29 | $\mu$s. | See point 6 * |
| Trigger gate inhibiting time | $t_{gi}$ | = min. 29 | $\mu$s. | See point 7 * |

Trigger input (T-terminals 19 and 4)

A negative-going voltage step or trigger pulse is applied to the interconnected trigger inputs T of flip-flops A and A' (terminals 19 and 4 respectively).
Each trigger pulse applied to the terminals T switches the decade counters, provided that the G-inputs (EG-inputs via diode) are left floating or at min. 2/3 Vp (gate open).

| | | | | |
|---|---|---|---|---|
| Required direct current when $V_T$ = max. 0.3 V | $-I_{TD}$ | = max. 1.1 | mA | |
| Required transient charge when $V_T$ changes from 2/3 $V_p$ to 0.5 V in 1.5 $\mu$s | $-Q_{TT}$ | = max. 3.4 | nC | |

Time data

| | | | | |
|---|---|---|---|---|
| Fall time | $t_f$ | = max. 1.5 | $\mu$s | See point 3 * |
| Pulse duration | $t_p$ | = min. 2 | $\mu$s | |
| Trigger gate setting time | $t_{gs}$ | = min. 29 | $\mu$s | |

Base inputs (W-terminals)

Capacitance (wiring plus output of TG 13, TG 14 or TG 15) max. 95 pF

Note

The output capacitance of the trigger gates TG 13, TG 14 and TG 15 is max. 5 pF.

* Section "Time definitions" of "Circuit blocks 10-Series".

OUTPUT DATA (at $V_P$ = 11.4 V and $V_N$ = −12.6 V, unless specified differently)

In excess of the internal load, represented by the circuit blocks on the printed-wiring board, the Q-outputs of each flip-flop in the decade counters may furthermore be loaded as specified in the table below.

| flip-flop | FF 12-A (A') | | FF 12-B (B') | | FF 12-C (C') | | FF 12-D (D') | |
|---|---|---|---|---|---|---|---|---|
| output terminal | $\overline{Q}$ | Q | $\overline{Q}$ | Q | $\overline{Q}$ | Q | $\overline{Q}$ | Q |
| | 18a (5) | 18 (6) | 17a (5a) | 17 (4a) | 14a (10) | 14 (9) | 12 (10a) | 12a (9a) |
| available direct current: min. $I_{QD}$ in mA | 7.1 | 6 | 7.1 | 6 | 7.1 | 6 | 6 | 7.1 |
| available transient charge when $V_Q$ changes from 2/3 $V_P$ to 0.5 V in 1.5 $\mu$s: min. $Q_{QT}$ in nC | 25.8 | 22.4 | 25.8 | 22.4 | 25.8 | 22.4 | 25.8 | 25.8 |

For $T_{amb}$ = min. −25 °C the available direct current $I_{QD}$ has to be reduced with 1.6 mA and similarly the available transient charge $Q_{QT}$ with 5 nC.

Wiring capacitance at each Q-output max. 175 pF

Output levels during counting

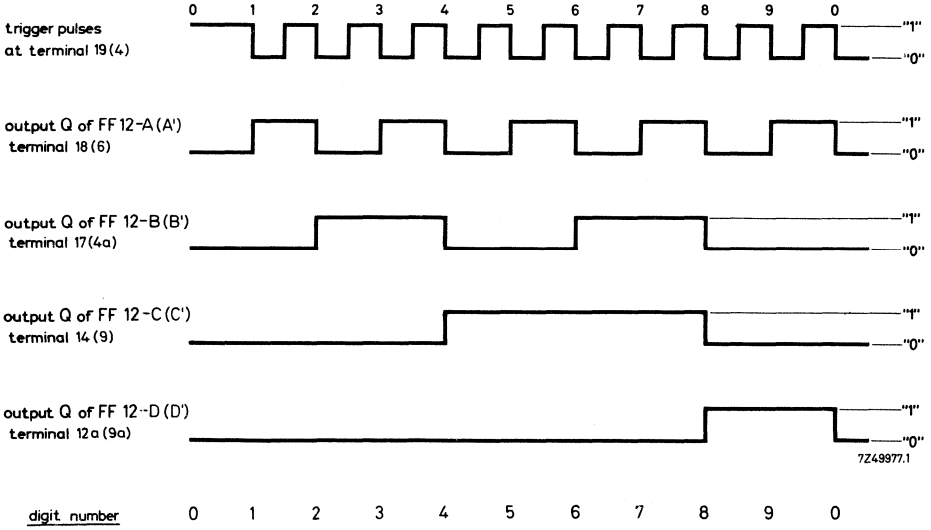



Fig.3

## DECADE COUNTER AND BUFFER MEMORY 2.DCA 12B

For circuit diagram
see next page

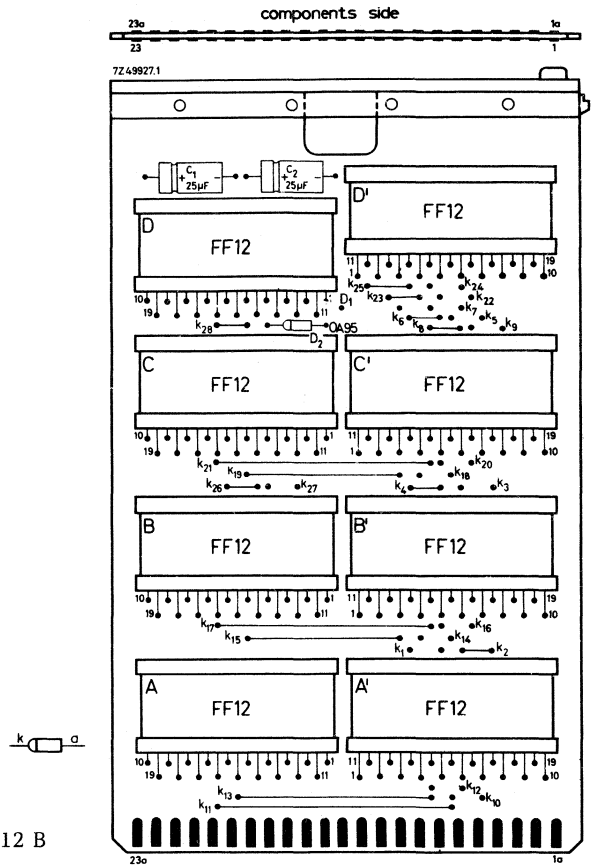






Fig.5. 2.DCA 12 B

INPUT REQUIREMENTS (at $V_P$ = 11.4 V and $V_N$ = -12.6 V unless specified differently)

Set/reset input (S-terminals)

Common reset decade counter (terminal 20)

With one pulse at terminal 20 all flip-flops in the decade will be reset simultaneously. For further data, see 2.DCA 12 A.

Common reset buffer memory (terminal 3)

With one pulse at terminal 3 all flip-flops in the buffer memory will be reset simultaneously.
Pulse duration $t_p$ = min. 2 $\mu$s
For further set/reset data, see 2.DCA 12 A.

CIRCUIT DATA

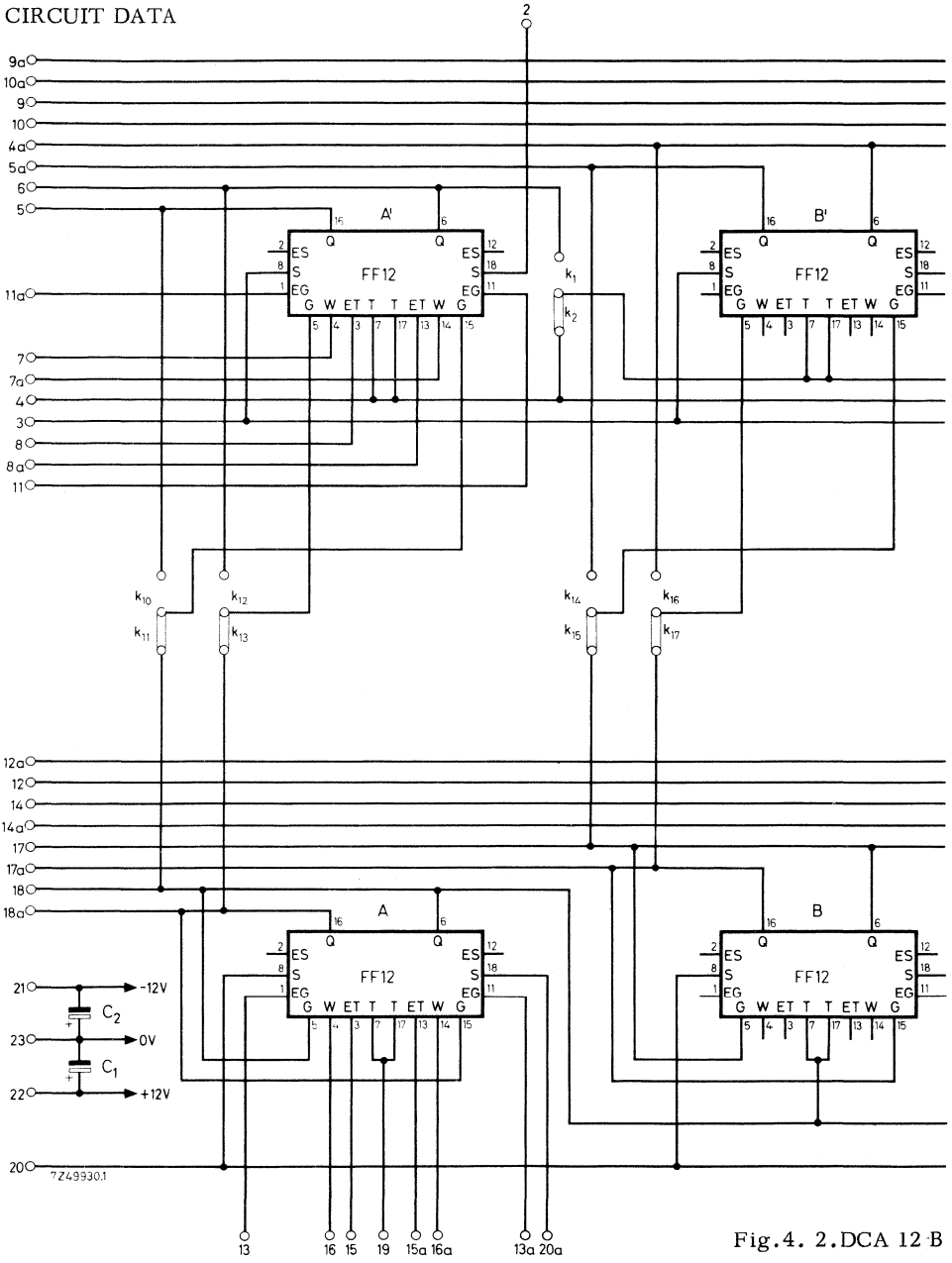
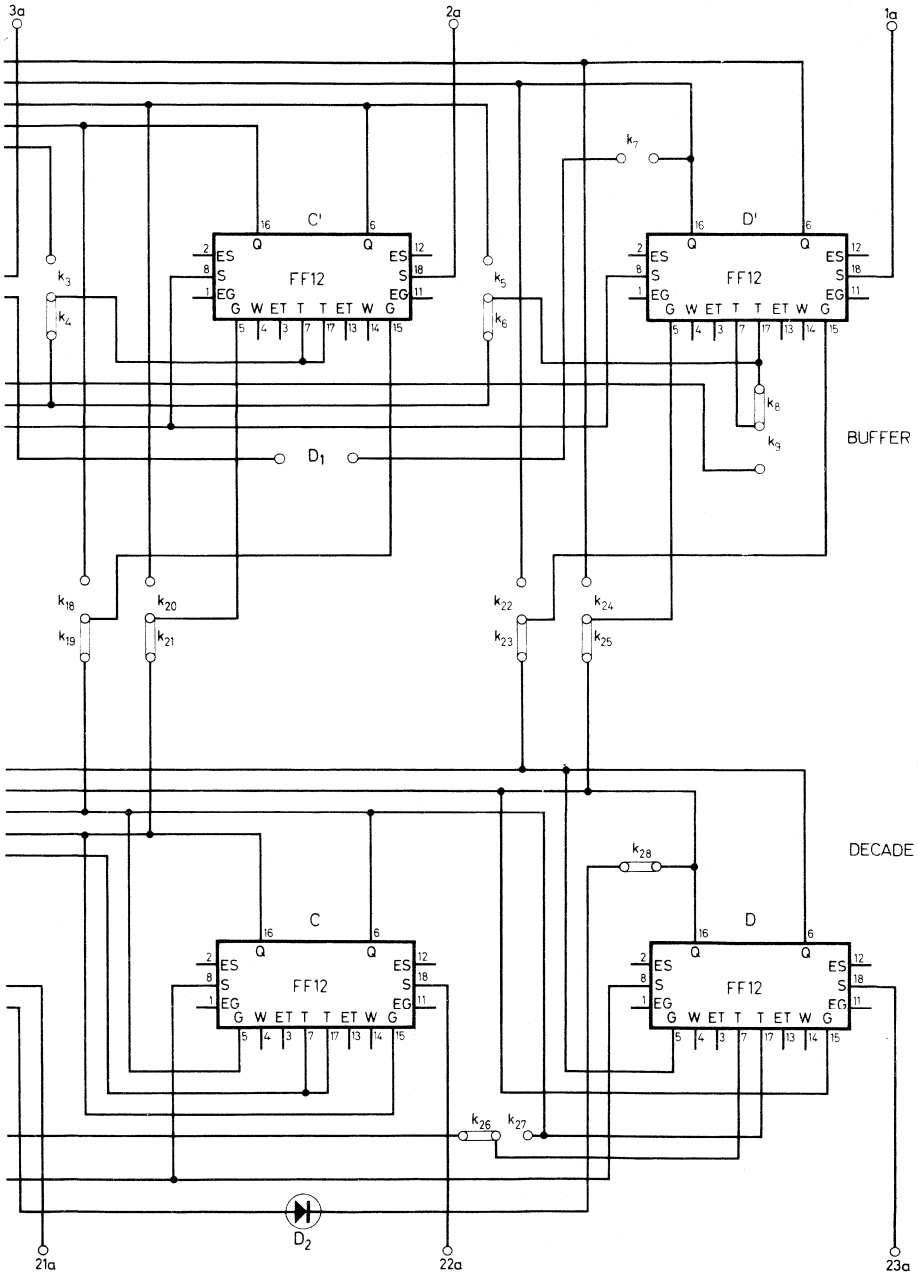



Fig.4. 2.DCA 12 B


3a
2a
1a
C'
D'
C
D
FF12
Q
ES
S
EG
G W ET T T ET W G
$k_3$
$k_4$
$k_5$
$k_6$
$k_7$
$k_8$
$k_9$
$k_{18}$
$k_{19}$
$k_{20}$
$k_{21}$
$k_{22}$
$k_{23}$
$k_{24}$
$k_{25}$
$k_{26}$
$k_{27}$
$k_{28}$
$D_1$
$D_2$
BUFFER
DECADE
21a
22a
23a

Trigger input (T-terminals 19 and 4)

Trigger input decade counter (terminal 19)

A negative-going voltage step or trigger pulse is applied to the interconnected trigger inputs T of flip-flop A (terminal 19).
Each trigger pulse applied to the terminal T of flip-flop A switches the decade counter, provided that the G-inputs (EG-inputs via diode) are left floating or at minimum 2/3 $V_P$ (gate open).
For further trigger data, see 2.DCA 12 A.

Trigger input buffer memory (terminal 4)

With one trigger pulse applied to the interconnected terminals T of the buffer memory (terminal 4) the contents of the decade counter is shifted into the buffer memory.

| | | |
|---|---|---|
| Required direct current when $V_T$ = max. 0.3 V | $-I_{TD}$ = max. 4.4 mA | |
| Required transient charge when $V_T$ changes from 2/3 $V_P$ to 0.5 V in 1.5 $\mu$s | $-Q_{TT}$ = max. 13.6 nC | |
| Time data | | |
| Fall time | $t_f$ = max. 1.5 $\mu$s | See point 3* |
| Pulse duration | $t_p$ = min. 2 $\mu$s | |
| Trigger gate setting time | $t_{gs}$ = min. 29 $\mu$s | |

OUTPUT DATA (at $V_P$ = 11.4 V and $V_N$ = −12.6 V unless specified differently)

In excess of the internal load, represented by the circuit blocks on the printed-wiring board, the Q-outputs of each flip-flop in the decade counter and in the buffer memory may furthermore be loaded as specified in the tables below.

Decade counter section

| flip-flop | FF 12-A | | FF 12-B | | FF 12-C | | FF 12-D | |
|---|---|---|---|---|---|---|---|---|
| output terminal | $\overline{Q}$ | Q | $\overline{Q}$ | Q | $\overline{Q}$ | Q | $\overline{Q}$ | Q |
| | 18a | 18 | 17a | 17 | 14a | 14 | 12 | 12a |
| available direct current: min. $I_{QD}$ in mA | 6 | 4.9 | 6 | 4.9 | 6 | 4.9 | 4.9 | 6 |
| available transient charge when $V_Q$ changes from 2/3 $V_P$ to 0.5 V in 1.5 $\mu$s: min. $Q_{QT}$ in nC | 24.6 | 21.2 | 24.6 | 21.2 | 24.6 | 21.2 | 24.6 | 24.6 |

* Section "Time definitions" of "Circuit blocks 10 series".

Buffer memory section

| flip-flop | FF 12-A' | | FF 12-B' | | FF 12-C' | | FF 12-D' | |
|---|---|---|---|---|---|---|---|---|
| output terminal | $\overline{Q}$ | Q | $\overline{Q}$ | Q | $\overline{Q}$ | Q | $\overline{Q}$ | Q |
| | 5 | 6 | 5a | 4a | 10 | 9 | 10a | 9a |
| available direct current: min. $I_{QD}$ in mA | 8.2 | 8.2 | 8.2 | 8.2 | 8.2 | 8.2 | 8.2 | 8.2 |
| available transient charge when $V_Q$ changes from 2/3 $V_P$ to 0.5 V in 1.5 $\mu$s: min. $Q_{QT}$ in nC | 27 | 27 | 27 | 27 | 27 | 27 | 27 | 27 |

For $T_{amb}$ = min. −25 °C the available direct current $I_{QD}$ has to be reduced with 1.6 mA and similarly the available transient charge $Q_{QT}$ with 5 nC.

Buffer memory loaded with the numerical indicator tube driver ID 10

When the buffer memory is loaded with the circuit block ID 10, the available output data of each flip-flop is specified separately in the table below.
The loadability of the flip-flop outputs can be increased by connecting an external resistor in parallel with the built-in collector resistor of the corresponding output. This resistor has to be connected between the output terminal and $V_P$. For each additional driven input, a parallel resistor of 51 kΩ ± 5 % is required. The total number of driven inputs is also specified in the table below.

| flip-flop | | FF 12-A' | | FF 12-B' | | FF 12-C' | | FF 12-D' | |
|---|---|---|---|---|---|---|---|---|---|
| output terminal | | $\overline{Q}$ | Q | $\overline{Q}$ | Q | $\overline{Q}$ | Q | $\overline{Q}$ | Q |
| | | 5 | 6 | 5a | 4a | 10 | 9 | 10a | 9a |
| max. number of 10-series circuit blocks, that may be driven, provided each driven input represents a load of $-I_D$ = max. 1.1 mA and $-Q_T$ = max. 3.4 nC | $T_{amb}$ = min. 0 °C | 6 | 6 | 4 | 6 | 4 | 4 | 4 | 6 |
| | $T_{amb}$ = min. −25 °C | 6 | 6 | 4 | 5 | 4 | 4 | 4 | 6 |
| max. number of driven 10-series circuit blocks, with external parallel collector resistor (s) | $T_{amb}$ = min. 0 °C | 7 | 7 | 6 | 6 | 6 | 6 | 6 | 7 |
| | $T_{amb}$ = min. −25 °C | 6 | 6 | 5 | 5 | 5 | 5 | 5 | 6 |

BINARY COUNTER 2.DCA 12 C

CIRCUIT DATA

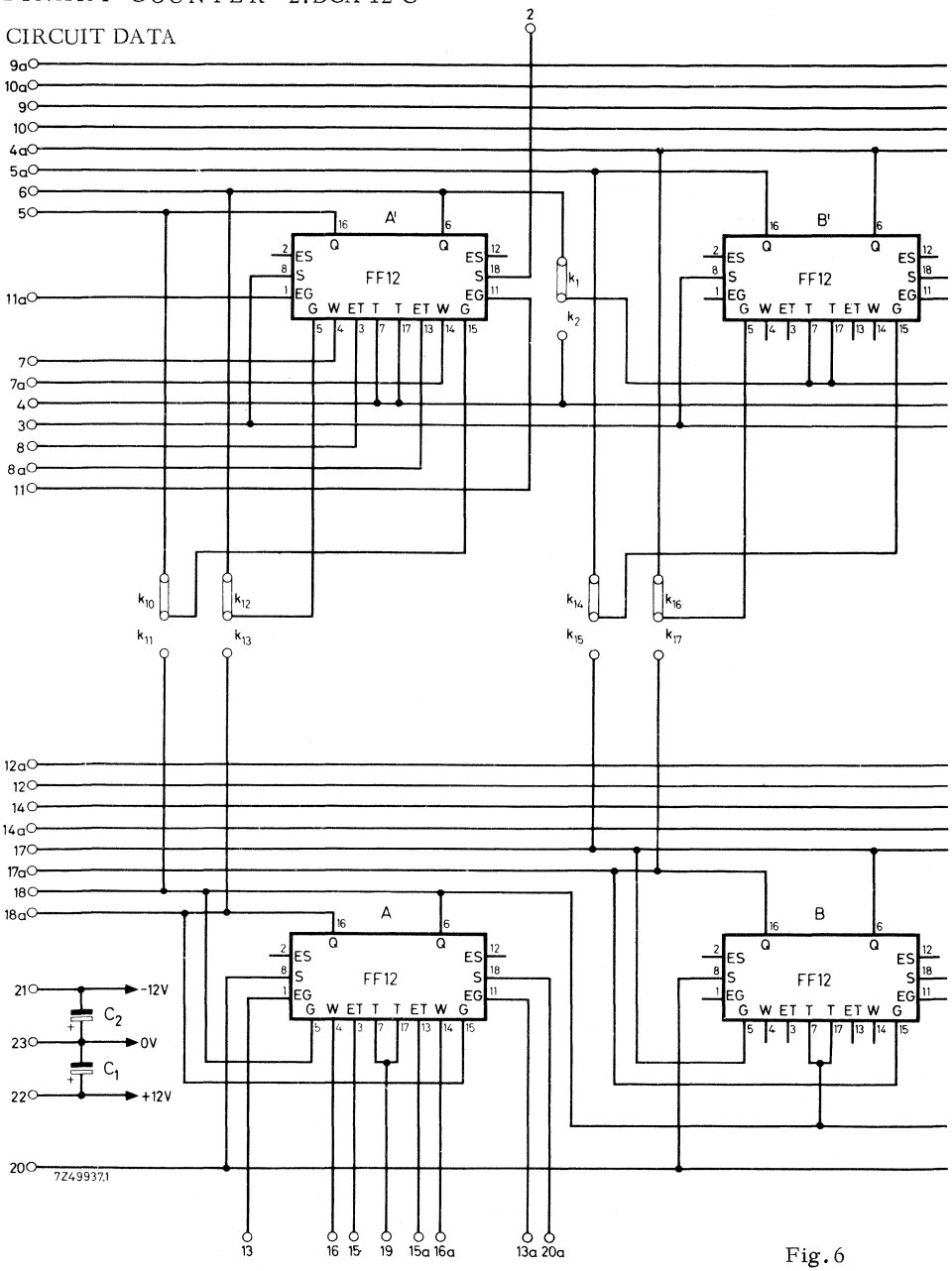
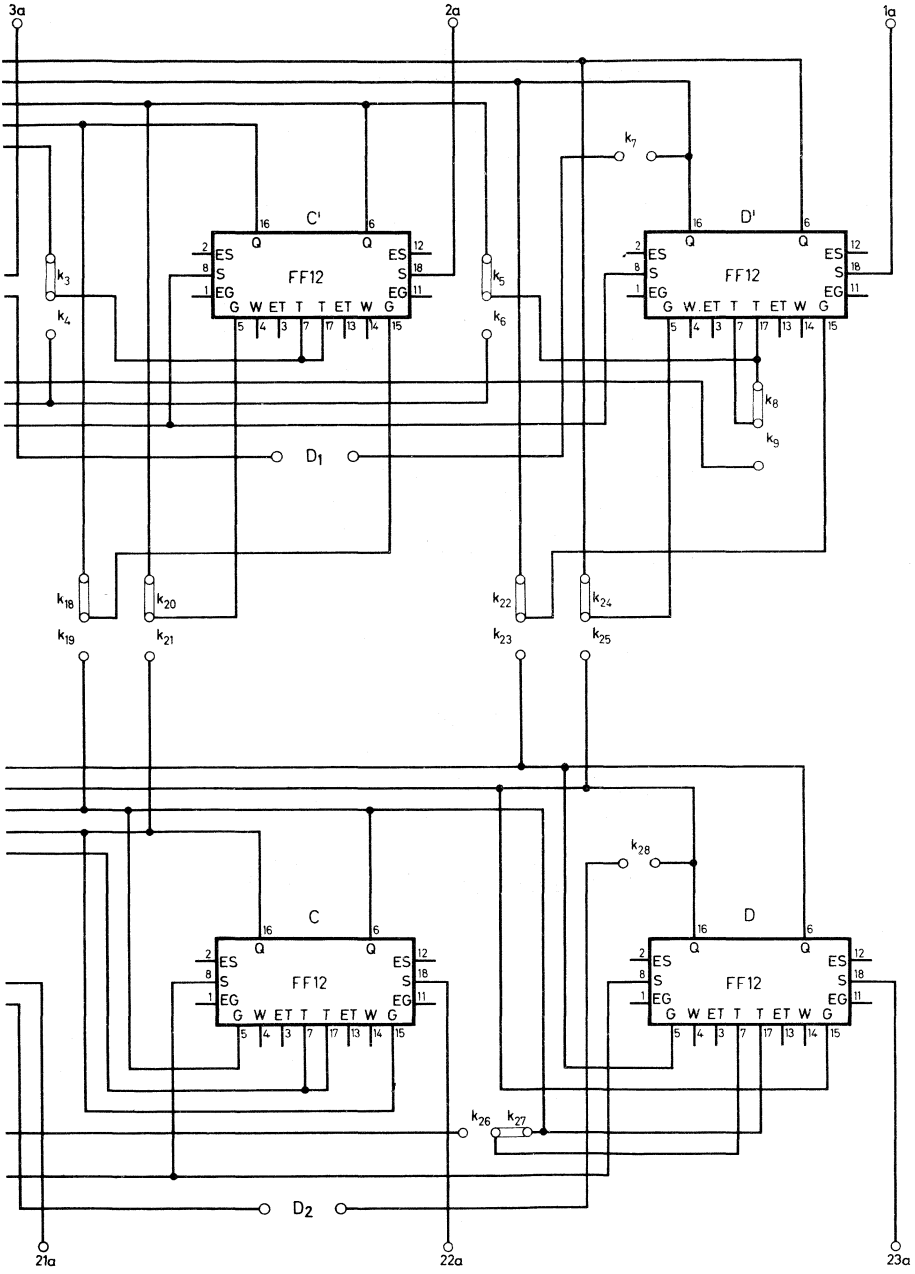



Fig. 6


3a
2a
1a
C'
D'
C
D
FF12
ES
S
EG
Q
G W ET T T ET W G
$k_3$
$k_4$
$k_5$
$k_6$
$k_7$
$k_8$
$k_9$
$k_{18}$
$k_{19}$
$k_{20}$
$k_{21}$
$k_{22}$
$k_{23}$
$k_{24}$
$k_{25}$
$k_{26}$
$k_{27}$
$k_{28}$
$D_1$
$D_2$
21a
22a
23a

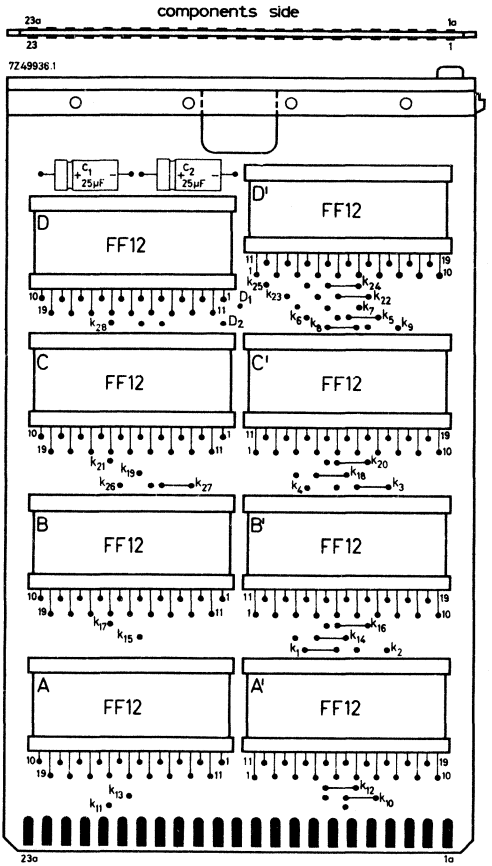



Fig.7. 2.DCA 12C

INPUT REQUIREMENTS

Similar to 2.DCA 12 A, with the exception of:

Common reset (terminals 3 and/or 20)

Pulse duration $t_p$ = min. 2 $\mu$s per flip-flop

OUTPUT DATA (at $V_P$ = 11.4 V and $V_N$ = −12.6 V unless specified differently)

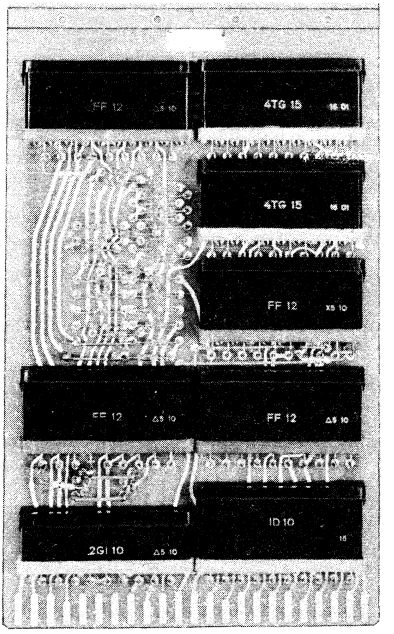
In excess of the internal load, represented by the circuit blocks on the printed-wiring board, the Q-outputs of each flip-flop in the binary counter (scaler of 16) may furthermore be loaded as specified in the table below.

| flip-flop | FF 12-A (A') | | FF 12-B (B') | | FF 12-C (C') | | FF 12-D (D') | |
|---|---|---|---|---|---|---|---|---|
| output terminal | $\overline{Q}$ | Q | $\overline{Q}$ | Q | $\overline{Q}$ | Q | $\overline{Q}$ | Q |
| | 18a (5) | 18 (6) | 17a (5a) | 17 (4a) | 14a (10) | 14 (9) | 12 (10a) | 12a (9a) |
| available direct current: min. $I_{QD}$ in mA | 7.1 | 6 | 7.1 | 6 | 7.1 | 6 | 7.1 | 7.1 |
| available transient charge when $V_Q$ changes from 2/3 $V_P$ to 0.5 V in 1.5 $\mu$s: min. $Q_{QT}$ in nC | 25.8 | 22.4 | 25.8 | 22.4 | 25.8 | 22.4 | 25.8 | 25.8 |

For $T_{amb}$ = min. −25 °C the available direct current $I_{QD}$ has to be reduced with 1.6 mA and similarly the available transient charge $Q_{QT}$ with 5 nC.

When the flip-flops are connected to form a binary counter, scaler of 256, the available $I_{QD}$ and $Q_{QT}$ of output Q of FF 12-D (D') have to be decreased till 6 mA and 22.4 nC respectively.

# REVERSIBLE DECADE COUNTER AND NUMERICAL INDICATOR TUBE DRIVER ASSEMBLY




RZ 22603-13

The assembly consists of four circuit blocks FF 12, two circuit blocks 4.TG 15, a circuit block 2.GI 10 and a circuit block ID 10, mounted on a printed-wiring board.
Versions without the 2.GI 10 and/or the ID 10 are also available.

- BCA 10 A, catalog number 2722 009 02101.

  This assembly contains four flip-flops FF 12, two quadruple trigger gates 4.TG 15 and a dual positive gate inverter amplifier 2.GI 10, interconnected as a reversible decade counter, operating in the 1-2-4-8 code for both forward and reverse counting. It contains also the numerical indicator tube driver ID 10 providing the BCD - to decimal decoding - and driving circuits for the numerical indicator tube ZM1000, ZM1020 or ZM1080. One half of the 2.GI 10 is inoperative in the BCA 10 A and can therefore be used for other purposes in the logic.
  The required interconnections are shown in Figs. 1 and 2.

- BCA 10 B, catalog number 2722 009 02111.

  This assembly is identical to the BCA 10 A but without the circuit block ID 10 mounted on the board. The lay-out of the printed-wiring board allows the mounting of the ID 10 separately (see Figs. 7 and 8).

- BCA 10 C, catalog number 2722 009 02121

  This assembly is identical to the BCA 10 A but here reverse counting is performed in the 1-2-4-2 (jump at 8) code. Therefore the circuit block 2.GI 10 is not mounted.
  The required interconnections are shown in Figs. 9 and 10.

- BCA 10 D, catalog number 2722 009 02131.

  This assembly is identical to the BCA 10 C but without the circuit block ID 10 mounted on the board. The lay-out of the printed-wiring board allows the mounting of the ID 10 separately (see Figs. 11 and 12).

In all versions the counting direction is determined by the voltage levels applied to terminals 18 and 19.
For forward counting holds:

- the positive level has to be applied to terminal 19,
- the "0" level has to be applied to terminal 18,
- the trigger pulse has to be applied to terminal 13.

For reverse counting holds:

- the positive level has to be applied to terminal 18,
- the "0" level has to be applied to terminal 19,
- the trigger pulse has to be applied to terminal 2a.

When two of these assemblies are operating in series the following interconnections have to be made.

For forward counting: terminal 5a of the first decade has to be connected to terminal 13 of the second decade.
For reverse counting: terminal 6a of the first decade has to be connected to terminal 2a of the second decade.

The bare printed-wiring board (catalog number 4322 026 38730), provided with plated-through holes and double-sided goldplated contacts, is made of glass-epoxy material. Moreover the printed-wiring board is delivered with an extractor and a locking device.
With the mating connector (catalog number 2422 020 52591), not supplied with the assembly, the printed-wiring board of standard dimensions (121.8 mm x 207.0 mm x 1.6 mm) can be used directly in the standard mounting chassis (catalog number 4322 026 38240).

The circuit blocks are secured to the printed-wiring board by means of locking caps (catalog number 4322 026 32150).

| | |
|---|---|
| Counting rate | max. 30 kHz |
| Ambient-temperature range | |
| operating | −25 to +55 °C<br>below 0 °C: derated output data |
| storage | −55 to +75 °C |
| Weight | approx. 400 g |

The data specified below apply to the BCA 10 A in particular.
For the sake of simplicity for the other versions only data are specified separately, which differ from those of the BCA 10 A.

# REVERSIBLE DECADE COUNTER AND NUMERICAL INDICATOR TUBE DRIVER BCA 10 A

## CIRCUIT DATA

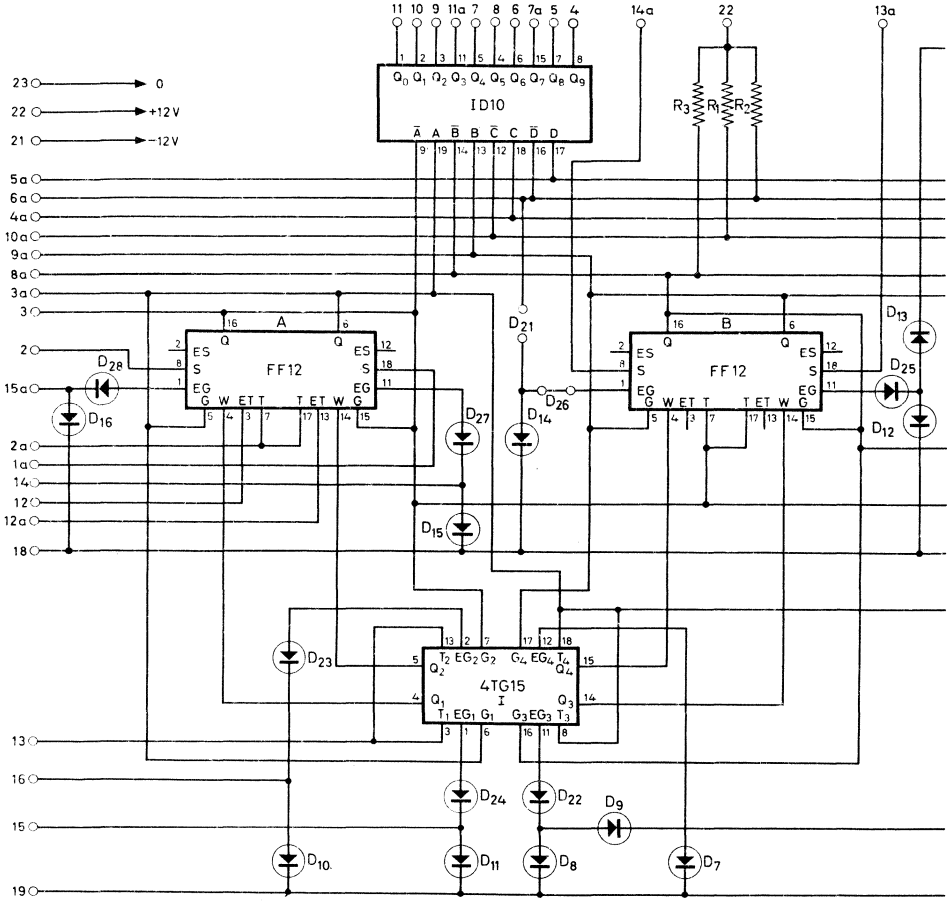
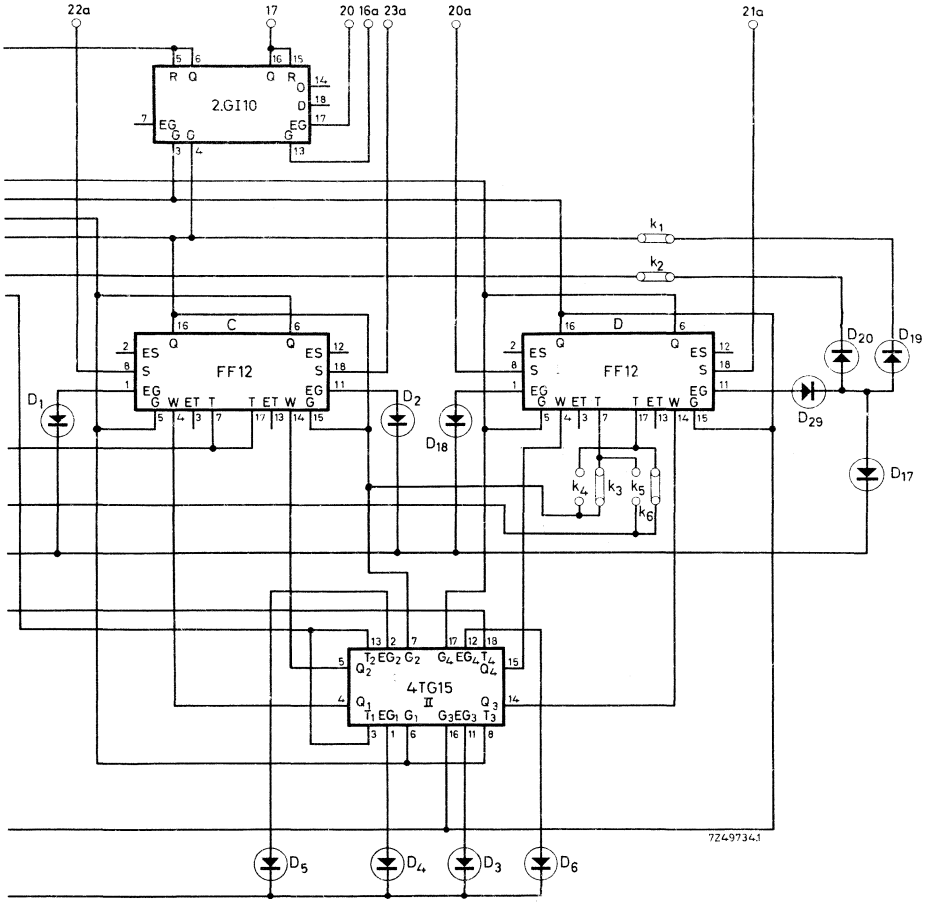



Fig.1


22a
17
20 16a 23a
20a
21a
2.GI10
FF12
C
D
4TG15
II
$k_1$
$k_2$
$k_3$
$k_4$
$k_5$
$k_6$
$D_1$
$D_2$
$D_{18}$
$D_{20}$
$D_{19}$
$D_{29}$
$D_{17}$
$D_5$
$D_4$
$D_3$
$D_6$
72497341

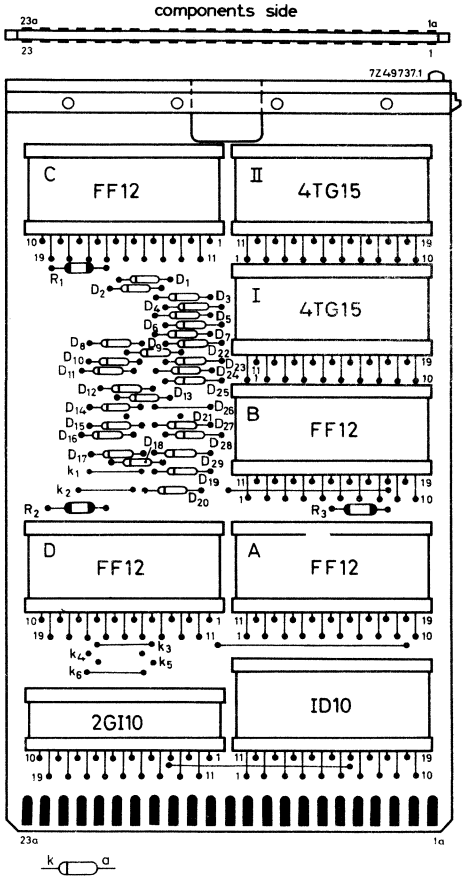



Fig.2. BCA 10 A

Terminals

1 = not connected
2 = set input S of flip-flop A
3 = output $\overline{Q}$ of flip-flop A
4 = numerical output 9 of ID 10
5 = numercial output 8 of ID 10
6 = numercial output 6 of ID 10
7 = numerical output 4 of ID 10
8 = numerical output 5 of ID 10
9 = numerical output 2 of ID 10
10 = numerical output 1 of ID 10

11 = numerical output 0 of ID 10
12 = extension trigger input ET of flip-flop A
13 = trigger input forward counting
14 = extension gate input EG of flip-flop A
15 = extension gate input EG of trigger gate 4.TG 15-I
16 = extension gate input EG of trigger gate 4.TG 15-I
17 = output Q of GI 10
18 = condition input for counting direction
19 = condition input for counting direction
20 = extension gate input EG of GI 10
21 = common negative supply −12 V
22 = common positive supply +12 V
23 = common supply 0 V

1a = set input S of flip-flop A
2a = trigger input reverse counting
3a = output Q of flip-flop A
4a = output Q of flip-flop C
5a = output Q of flip-flop D
6a = output $\overline{Q}$ of flip-flop D
7a = numerical output 7 of ID 10
8a = output $\overline{Q}$ of flip-flop B
9a = output Q of flip-flop B
10a = output $\overline{Q}$ of flip-flop C
11a = numerical output 3 of ID 10
12a = extension trigger input ET of flip-flop A
13a = set input S of flip-flop B
14a = set input S of flip-flop B
15a = extension gate input EG of flip-flop A
16a = gate input G of GI 10
17a = not connected
18a = not connected
19a = not connected
20a = set input S of flip-flop D
21a = set input S of flip-flop D
22a = set input S of flip-flop C
23a = set input S of flip-flop C

Power supply

Terminal 21 : $V_N$ = −12 V ± 5 %, $-I_N$ = 6.5 mA
22 : $V_P$ = +12 V ± 5 %, $I_P$ = 36 mA
} The current values are nominal
23 : $V_E$ = 0 V common

INPUT REQUIREMENTS (at $V_P$ = 11.4 V and $V_N$ = -12.6 V unless specified differently)

Set/reset input (S-terminals)

Each S-input of the four flip-flops is brought out separately. A "positive low" voltage (between 0 V and 0.3 V) drives the corresponding transistor into the non-conducting state.

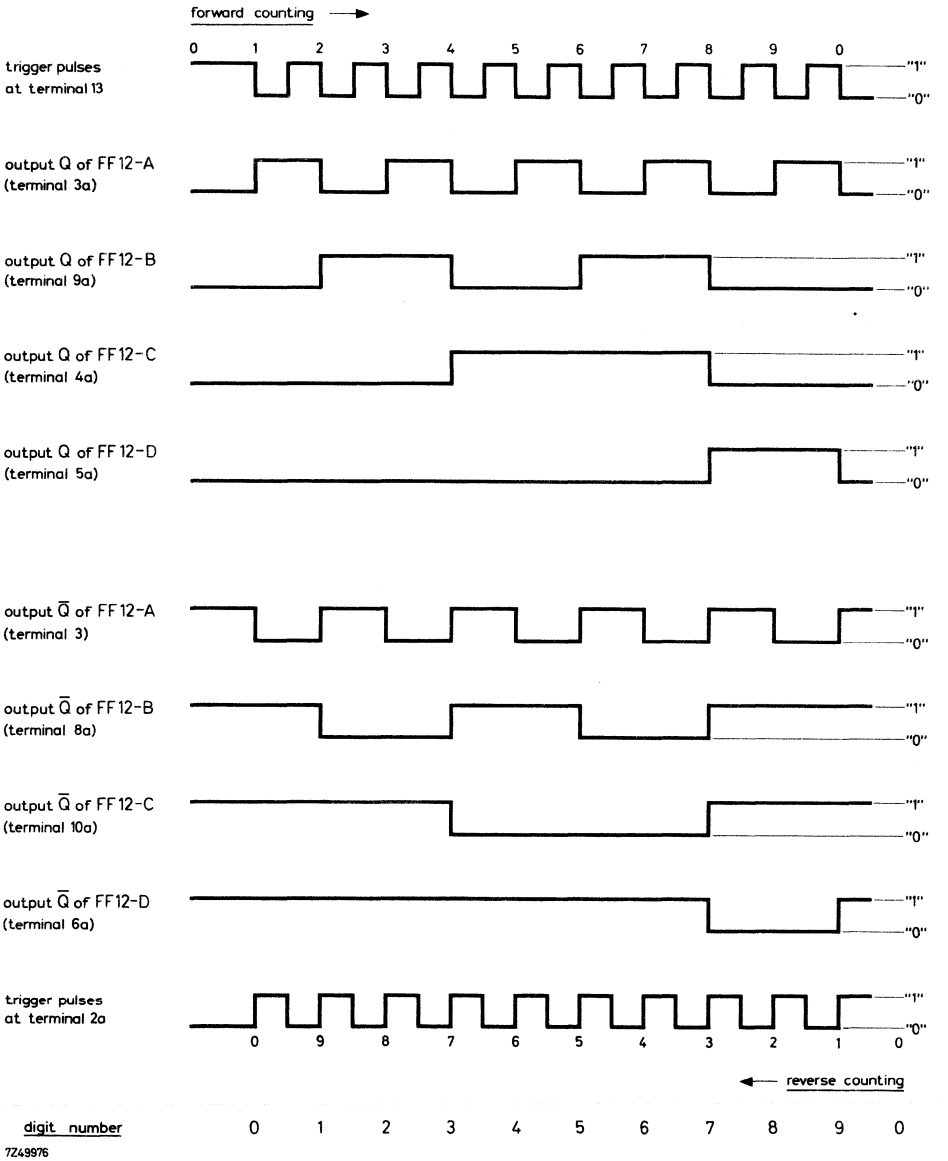
| | | | | | |
|---|---|---|---|---|---|
| Transistor conducting | | | | | |
| Voltage | $V_S$ | = min. | 2/3 $V_P$ | | |
| | | = max. | $V_P$ | | |
| Transistor non-conducting | | | | | |
| Voltage | $V_S$ | = min. | 0 | V | |
| | | = max. | 0.3 | V | |
| Required direct current | $-I_{SD}$ | = max. | 1.95 | mA | |
| Required transient charge when $V_S$ changes from 2/3 $V_P$ to 0.5 V in 1.5 $\mu$s | $-Q_{ST}$ | = max. | 2.8 | nC | |
| When the four flip-flops are reset simultaneously | | | | | |
| Required direct current | $-I_{SD}$ | = min. | 7.8 | mA | |
| Required transient charge when $V_S$ changes from 2/3 $V_P$ to 0.5 V in 1.5 $\mu$s | $-Q_{ST}$ | = max. | 11.2 | nC | |
| Time data | | | | | |
| Pulse duration | $t_p$ | = min. | 8 | $\mu$s | See point 4 * |
| Recovery time | $t_{rec}$ | = min. | 15 | $\mu$s | |
| Time delay between S- and T-signal | $t_{st}$ | = min. | 15 | $\mu$s | See point 5 * |

Condition inputs for controlling counting direction (terminals 18 and 19)

For forward counting the "positive high" level is applied to terminal 19 and the "positive low" level to terminal 18.
For reverse counting the "positive low" level is applied to terminal 19 and the "positive high" level to terminal 18.
When both terminals 18 and 19 carry the "positive low" level, the unit is blocked for both directions of counting.

---

* Section "Time definitions" of "Circuit blocks 10-Series".


forward counting
0 1 2 3 4 5 6 7 8 9 0
trigger pulses at terminal 13
output Q of FF12-A (terminal 3a)
output Q of FF12-B (terminal 9a)
output Q of FF12-C (terminal 4a)
output Q of FF12-D (terminal 5a)
output $\overline{Q}$ of FF12-A (terminal 3)
output $\overline{Q}$ of FF12-B (terminal 8a)
output $\overline{Q}$ of FF12-C (terminal 10a)
output $\overline{Q}$ of FF12-D (terminal 6a)
trigger pulses at terminal 2a
"1"
"0"
0 9 8 7 6 5 4 3 2 1 0
reverse counting
digit number
0 1 2 3 4 5 6 7 8 9 0
7Z49976

Output levels during counting

The output levels at the Q- and $\overline{Q}$-outputs of each flip-flop are shown in Fig.3. Note that when a Q-output is at "positive low" level the corresponding $\overline{Q}$-output is at "positive high" level and vice versa.
After 10 negative-going pulses at the trigger input terminal 13 for forward counting, the output Q of flip-flop D delivers the negative going carry pulse for the next decade, whilst the decade counter has resumed its initial position, namely all Q-output terminals being at "positive low" ("0") level.
When in this state of the counter a trigger pulse is applied to the trigger input terminal 2a, the output $\overline{Q}$ of flip-flop D delivers the negative going carry pulse to the next decade for reverse counting.
The relation between a digit number (output ID 10) and the corresponding state of each flip-flop is shown in the figure as well.

Numerical indicator tube driver section

The outputs $Q_0$ (terminal 11) up to and including $Q_9$ (terminal 4) of the ID 10 have to be connected to the pins $k_0$ up to and including $k_9$ of the numerical indicator tube ZM 1000, ZM 1020 and ZM 1080.
The anode of these tubes has to be connected via a resistor ($R_a$) to the high voltage power supply ($V_b$).

The current available at these 10 numerical outputs of the ID 10 can cope with the required cathode current $I_k$ of the indicator tubes ZM 1000, ZM 1020 and ZM 1080, when the following conditions are observed:

- operating-temperature range
- power supply $V_b$ for ZM 1000, ZM 1020 and ZM 1080
- anode series resistor $R_a$.

In the following graphs these data are specified.

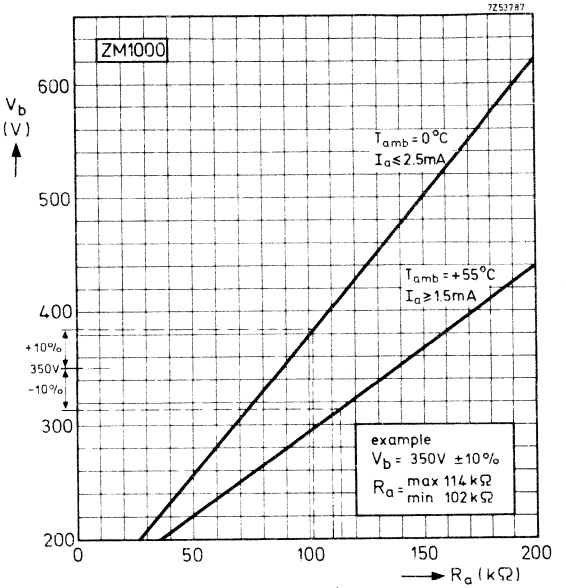

7Z53787
ZM1000
$V_b$ (V)
600
500
400
300
200
+10%
350V
-10%
$T_{amb}$ = 0°C
$I_a \leq 2.5$mA
$T_{amb}$ = +55°C
$I_a \geq 1.5$mA
example
$V_b$ = 350V ±10%
$R_a$ = max 114kΩ
min 102kΩ
0
50
100
150
200
$R_a$ (kΩ)

Fig.4

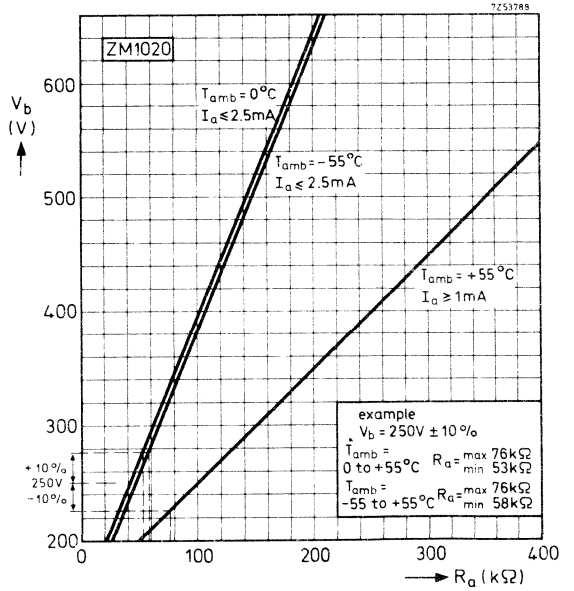

7Z53788
ZM1020
$V_b$ (V)
600
500
400
300
200
+10%
250V
-10%
$T_{amb}$ = 0°C
$I_a \leq 2.5$mA
$T_{amb}$ = -55°C
$I_a \leq 2.5$mA
$T_{amb}$ = +55°C
$I_a \geq 1$mA
example
$V_b$ = 250V ±10%
$T_{amb}$ = 0 to +55°C $R_a$ = max 76kΩ min 53kΩ
$T_{amb}$ = -55 to +55°C $R_a$ = max 76kΩ min 58kΩ
0
100
200
300
400
$R_a$ (kΩ)

Fig.5

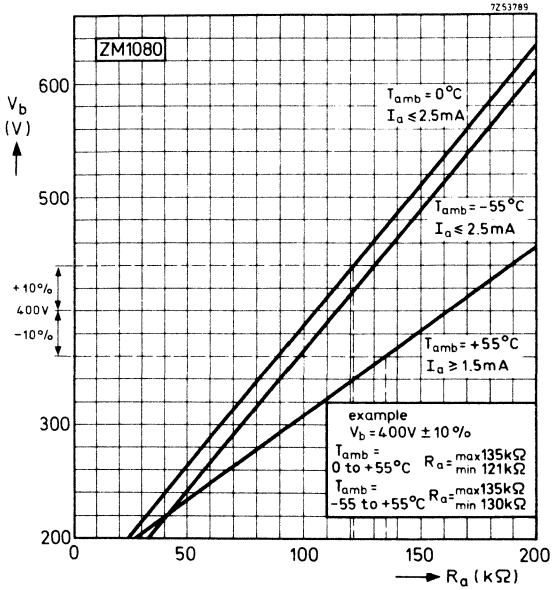



Fig.6

Wiring capacitance at each Q-output of the ID 10: max. 500 pF

REVERSIBLE DECADE COUNTER BCA 10 B

CIRCUIT DATA

For circuit diagram see next pages.

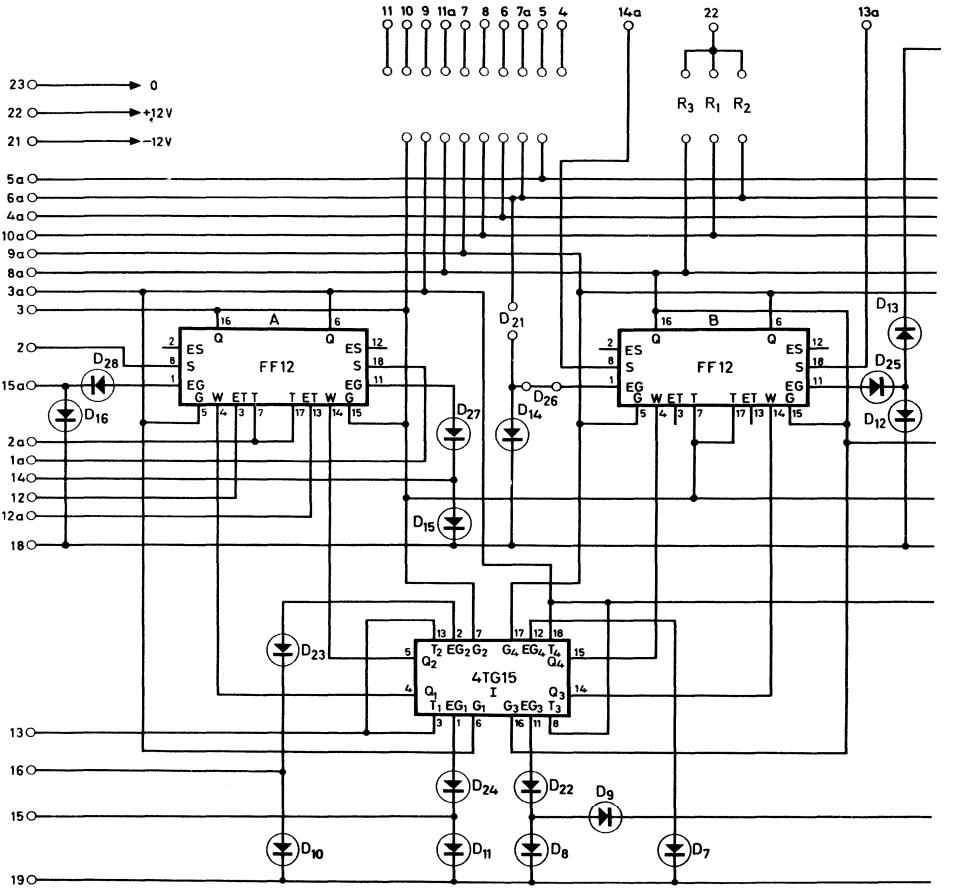
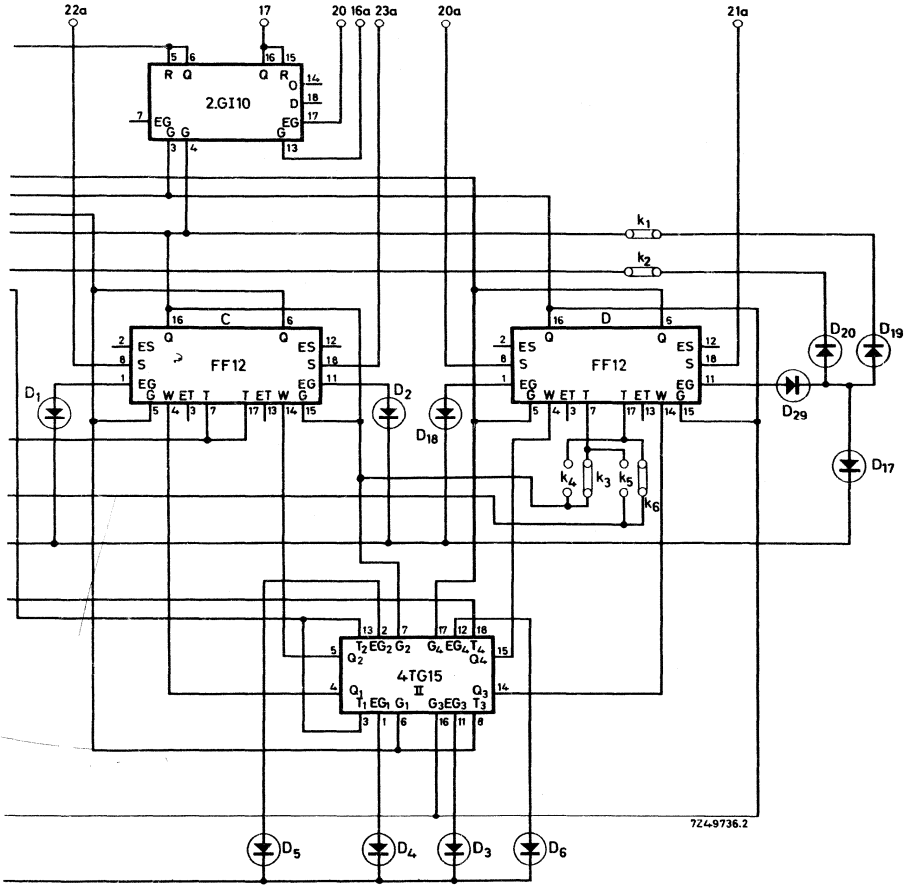

11 10 9 11a 7 8 6 7a 5 4
14a
22
13a
R3 R1 R2
23 0
22 +12V
21 −12V
5a 6a 4a 10a 9a 8a 3a 3 2 15a 2a 1a 14 12 12a 18
13 16 15 19
FF12
A
B
4TG15
D28 D16 D21 D27 D14 D26 D13 D25 D12 D15 D23 D24 D22 D9 D10 D11 D8 D7

Fig.7. BCA 10B


22a
17
20
16a
23a
20a
21a
2.GI10
FF12
FF12
4TG15
k1
k2
k3
k4
k5
k6
D1
D2
D5
D4
D3
D6
D18
D17
D20
D19
D29
7249736.2

Terminals (Fig.8)

Similar to BCA 10 A, with the exception of terminals 4, 5, 6, 7, 7a, 8, 9, 10, 11 and 11a, which are inoperative.

INPUT REQUIREMENTS

Similar to BCA 10 A.

OUTPUT DATA (at $V_P$ = 11.4 V and $V_N$ = −12.6 V, unless specified differently)

In excess of the internal load, represented by the circuit blocks mounted on the printed-wiring board, the Q-outputs of each flip-flop in the decade counter may furthermore be loaded as specified in the table below.

| flip-flop | FF 12-A | | FF 12-B | | FF 12-C | | FF 12-D | |
|---|---|---|---|---|---|---|---|---|
| output terminal | $\overline{Q}$ | Q | $\overline{Q}$ | Q | $\overline{Q}$ | Q | $\overline{Q}$ | Q |
| | 3 | 3a | 8a | 9a | 10a | 4a | 6a | 5a |
| available direct current min. $I_{QD}$ in mA | 3.8 | 3.8 | 3.8 | 4.9 | 3.8 | 4.9 | 3.8 | 6 |
| available transient charge when $V_Q$ changes from 2/3 $V_P$ to 0.5 V in 1.5 $\mu$s: min. $Q_{QT}$ in nC | 22.4 | 22.4 | 22.4 | 22.4 | 22.4 | 22.4 | 23.7 | 25.8 |

For $T_{amb}$ = min. −25 °C the available direct current $I_{QD}$ has to be reduced with 1.6 mA and similarly the available transient charge $Q_{QT}$ with 5 nC.

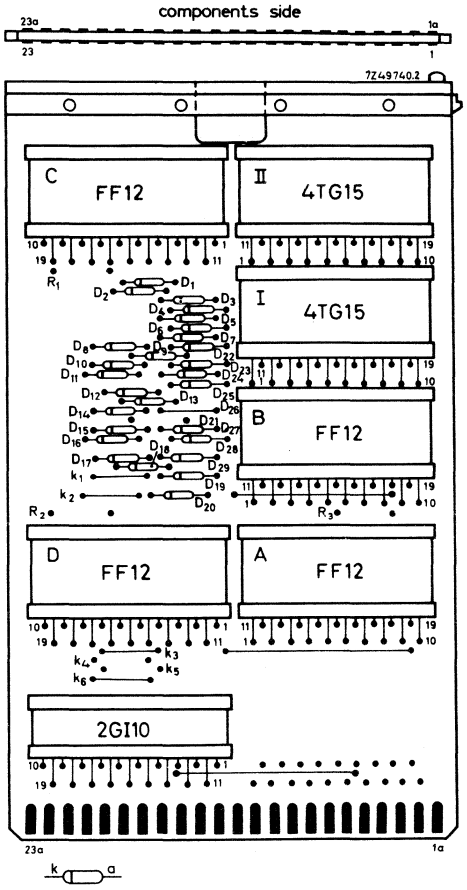

components side
23a
1a
23
1
7Z49740.2
C
FF12
II
4TG15
I
4TG15
B
FF12
D
FF12
A
FF12
2GI10
R1
R2
R3
k1
k2
k3
k4
k5
k6
k
a

Fig.8. BCA 10 B

## REVERSIBLE DECADE COUNTER AND NUMERICAL INDICATOR TUBE DRIVER BCA 10 C

CIRCUIT DATA

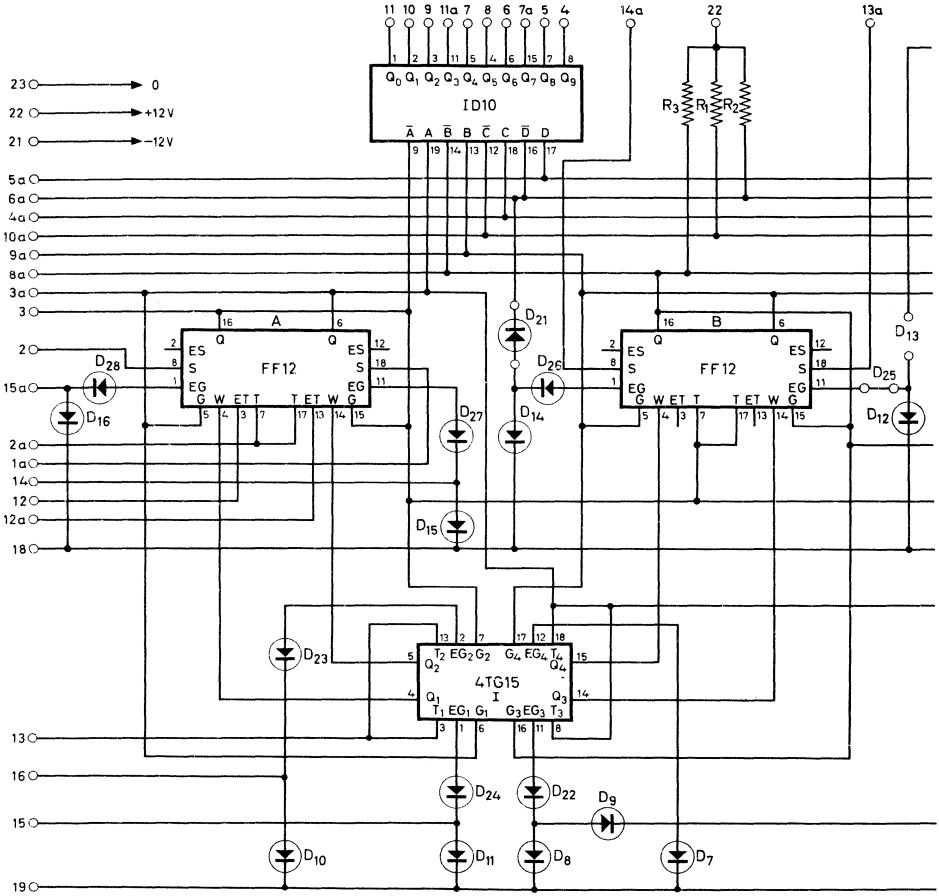
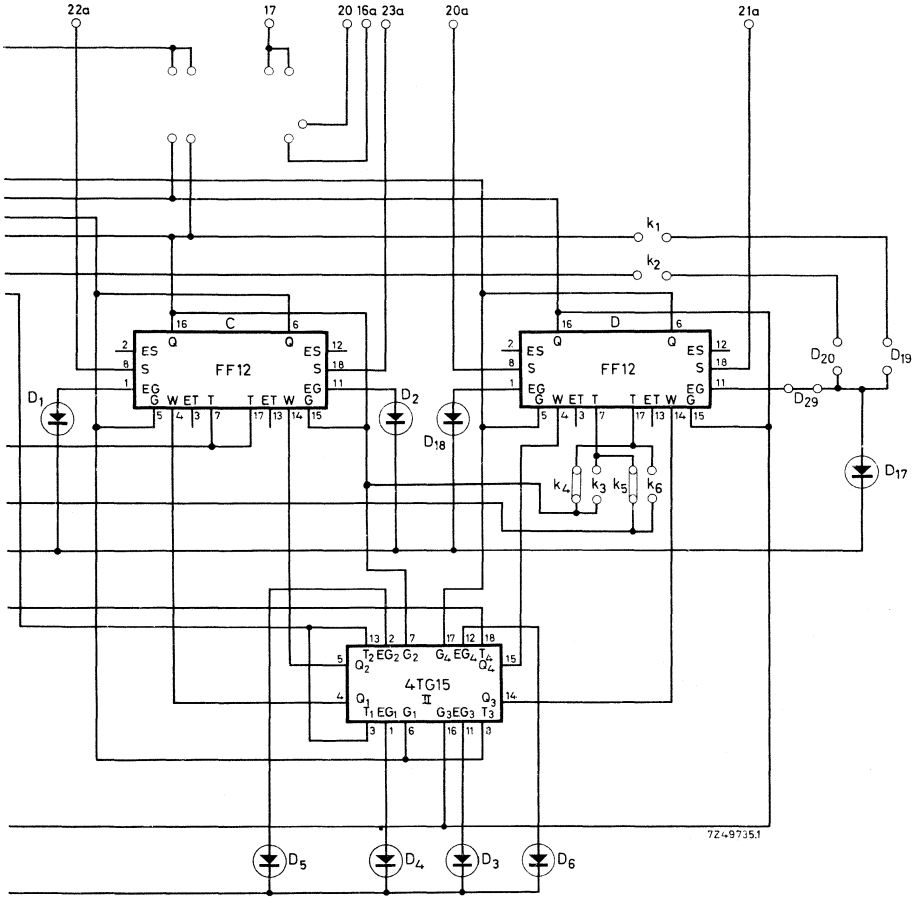



Fig.9


22a
17
20 16a 23a
20a
21a
k1
k2
C
D
FF12
FF12
D1
D2
D18
D20
D19
D29
D17
k4 k3 k5 k6
4TG15
II
D5
D4
D3
D6
7Z49735.1

Terminals (Fig.10)

Similar to BCA 10 A, with the exception of terminals 16a, 17 and 20, which are inoperative.

INPUT REQUIREMENTS

Similar to BCA 10 A.

OUTPUT DATA (at $V_P$ = 11.4 V and $V_N$ = −12.6 V, unless specified differently)

Decade counter section

In excess of the internal load, represented by the circuit blocks mounted on the printed-wiring board including the numerical indicator tube driver ID 10, the Q-outputs of each flip-flop in the decade counter may furthermore be loaded as specified in the table below.

The loadability of the flip-flops FF 12-A, FF 12-C and FF 12-D can be increased by connecting an external resistor of 51 kΩ±5% in parallel with the built-in collector resistor of the corresponding output. This resistor has to be connected between the output terminal and $V_P$.

| flip-flop | | FF 12-A | | FF 12-B | | FF 12-C | | FF 12-D | |
|---|---|---|---|---|---|---|---|---|---|
| output terminal | | $\overline{Q}$ | Q | $\overline{Q}$ | Q | $\overline{Q}$ | Q | $\overline{Q}$ | Q |
| | | 3 | 3a | 8a | 9a | 10a | 4a | 6a | 5a |
| max. number of 10-series circuit blocks, that may be driven, provided each driven input represents a load of $-I_D$ = max. 1.1 mA and $-Q_T$ = max. 3.4 nC | $T_{amb}$ = min. 0 °C | 1 | 1 | 3 | 3 | 3 | 1 | 2 | 4 |
| | $T_{amb}$ = min. −25 °C | 1 | 1 | 2 | 2 | 2 | 1 | 1 | 4 |
| max. number of driven 10-series circuit blocks, with external parallel collector resistor(s) | $T_{amb}$ = min. 0 °C | 3 | 3 | 3 | 3 | 3 | 3 | 2 | 5 |
| | $T_{amb}$ = min. −25 °C | 2 | 2 | 2 | 2 | 2 | 2 | 1 | 4 |

Numerical indicator tube driver section

Similar to BCA 10 A.

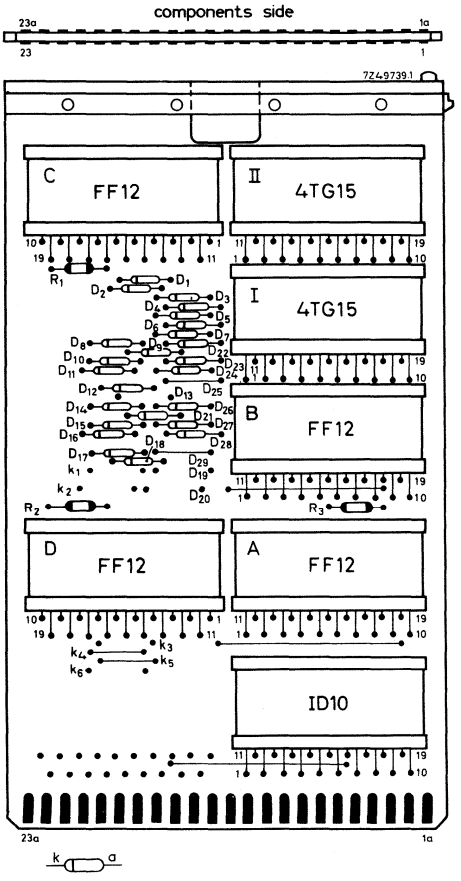



Fig.10. BCA 10 C

REVERSIBLE DECADE COUNTER BCA 10 D

CIRCUIT DATA

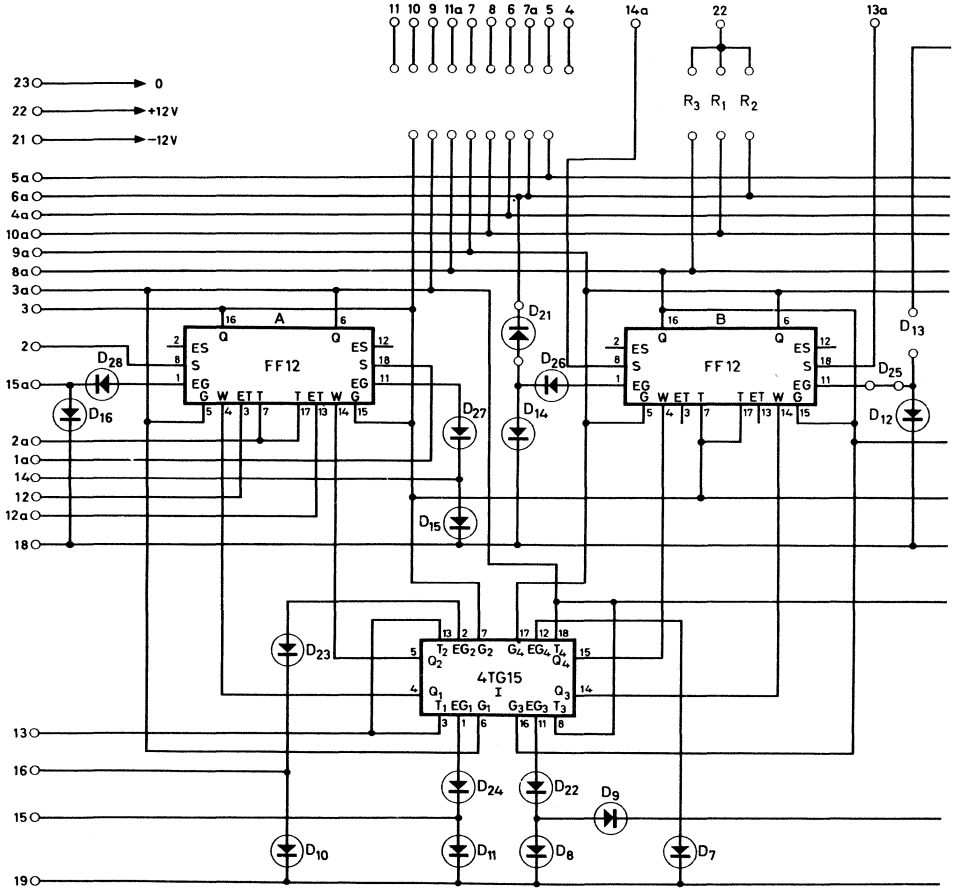
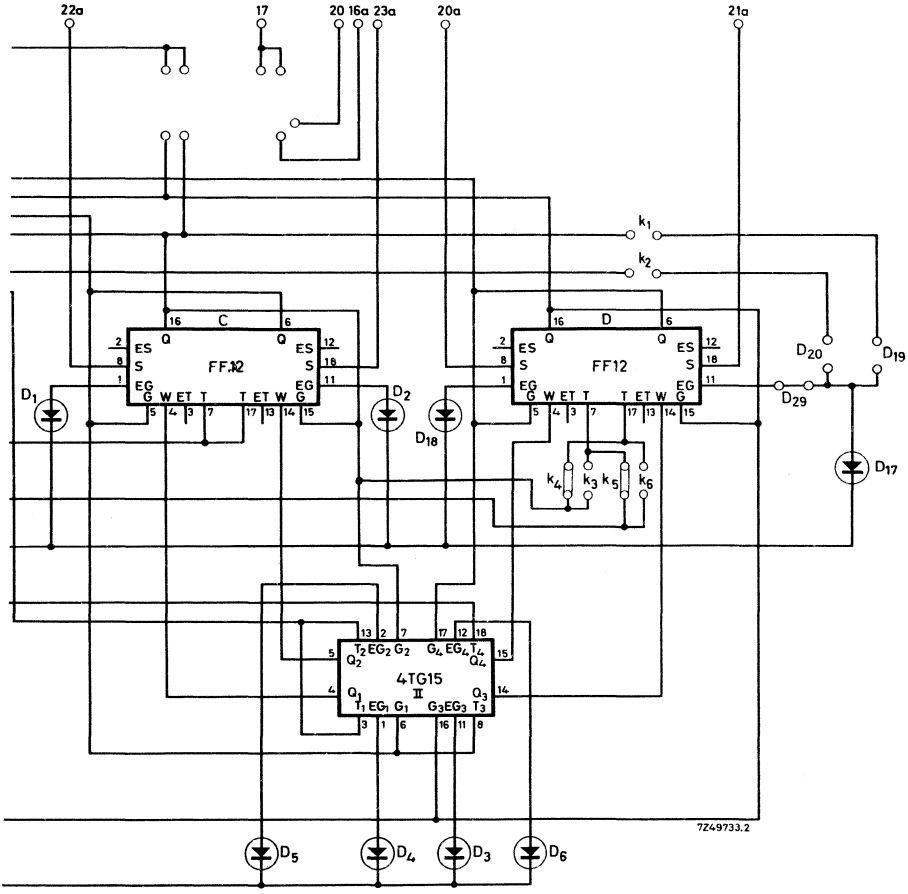



Fig.11


22a
17
20
16a
23a
20a
21a
k1
k2
FF12
C
D
ES
S
EG
Q
W
ET
T
G
D1
D2
D18
D20
D19
D29
D17
k3
k4
k5
k6
4TG15
II
D5
D4
D3
D6
7Z49733.2

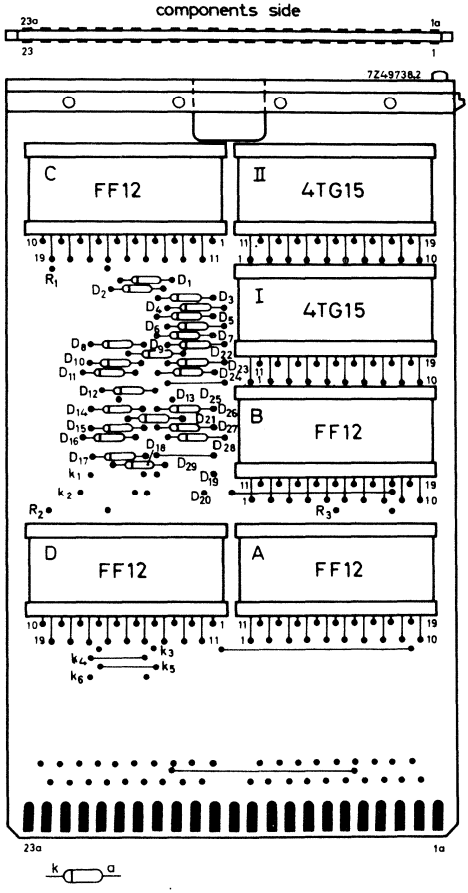



Fig.12. BCA 10 D

Terminals (Fig.12)

Similar to BCA 10 A, with the exception of terminals 4, 5, 6, 7, 7a, 8, 9, 10, 11, 11a, 16a, 17 and 20, which are inoperative.

INPUT REQUIREMENTS

Similar to BCA 10 A.

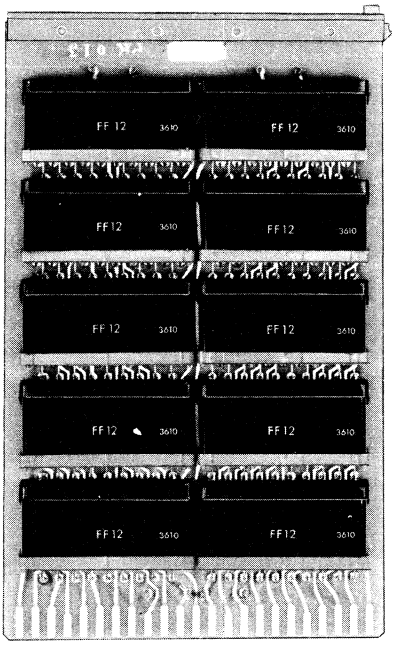
OUTPUT DATA (at $V_P$ = 11.4 V and $V_N$ = −12.6 V, unless specified differently)

In excess of the internal load, represented by the circuit blocks mounted on the printed-wiring board, the Q-outputs of each flip-flop in the decade counter may furthermore be loaded as specified in the table below.

| flip-flop | FF 12-A | | FF 12-B | | FF 12-C | | FF 12-D | |
|---|---|---|---|---|---|---|---|---|
| output terminal | $\overline{Q}$ | Q | $\overline{Q}$ | Q | $\overline{Q}$ | Q | $\overline{Q}$ | Q |
| | 3 | 3a | 8a | 9a | 10a | 4a | 6a | 5a |
| available direct current: min. $I_{QD}$ in mA | 3.8 | 3.8 | 4.9 | 4.9 | 4.9 | 4.9 | 3.8 | 6 |
| available transient charge when $V_Q$ changes from 2/3 $V_P$ to 0.5 V in 1.5 $\mu$s: min. $Q_{QT}$ in nC | 22.4 | 22.4 | 22.4 | 22.4 | 22.4 | 22.4 | 25.8 | 25.8 |

For $T_{amb}$ = min. −25 °C the available direct current $I_{QD}$ has to be reduced with 1.6 mA and similarly the available transient charge $Q_{QT}$ with 5 nC.

# DUAL SHIFT REGISTER ASSEMBLY




RZ 22603-7

This assembly can be applied to fulfil three major functions as described below.

- Dual 5-stages one-directional shift register (see Figs.1 and 2)
  The information that has to be serially shifted into the register, has to be applied to the gate inputs G of flip-flop FF 12-A (terminals 7 and 7a) or gate inputs G of flip-flop FF 12-A' (terminals 17a and 17).
  The trigger (shift) pulses have to be applied to the common trigger terminals 4 or 19.
  Both shift registers are provided with a common reset line (terminals 3a and 19a) while of each individual flip-flop in both shift registers, one S-input is brought out for pre-set purposes.
  The positions $k_1$, $k_2$, $k_3$ and $k_4$ on the printed-wiring board have to be left open.

- Dual one-directional decade ring counter (see Figs.1 and 2)

For this function the Q-outputs of flip-flop FF 12-E (FF 12-E') have to be cross-connected externally with the gate inputs G of flip-flop FF 12-A (FF 12-A'). The necessary interconnections are:
terminal 10a (13) with 7a (17) and
terminal 10 (12) with 7 (17a).
The trigger (shift) pulses have to be applied to the common trigger terminal 4 (19).
Both ring counters are provided with a common reset line (terminals 3a and 19a). Any disturbance in the code sequence can automatically be corrected after maximum one cycle of 10 pulses, by mounting two diodes AAY 21 per ring counter on the printed-wiring board. In Fig.2 the diode positions are indicated as $k_1$, $k_2$, $k_3$ and $k_4$; the diodes have to be mounted with the anode located at "a".
If these correction circuits are applied the EG-terminals 11 and 11a (12a and 13a) may not be used for blocking purposes of flip-flop FF 12-A (FF 12-A').

- Single 10-stages one-directional shift register (see Figs.1 and 2)

This function can be obtained by putting the two 5-stages shift registers in series.
The following external interconnections have to be made:
terminal 10a with 17a
terminal 10 with 17
terminal 4 with 19 (common trigger line)
terminal 3a with 19a (common reset line).
Each individual flip-flop in the shift register has one S-input brought out for preset purposes.
The positions $k_1$, $k_2$, $k_3$ and $k_4$ on the printed-wiring board have to be left open.

In the three above mentioned functions the trigger pulses can be inhibited by means of a "positive low" voltage applied to the EG-terminals 11 and 11a (12a and 13a) of the first flip-flop FF 12-A (FF 12-A').

The bare printed-wiring board (catalog number 4322 026 38740), provided with plated-through holes and double-sided goldplated contacts, is made of glass-epoxy material. Moreover, the printed-wiring board is delivered with an extractor and a locking device.
With the mating connector (catalog number 2422 020 52591), not supplied with the assembly, the printed-wiring board of standard dimensions (121.8 mm x 207.0 mm x 1.6 mm) can be used directly in the standard mounting chassis (catalog number 4322 026 38240).

The circuit blocks are secured to the printed-wiring board by means of locking caps (catalog number 4322 026 32150).

| | |
|---|---|
| Counting rate | max. 30 kHz |
| Ambient temperature range | |
| operating | -25 to +55 °C<br>below 0 °C: derated output data |
| storage | -55 to +75 °C |
| Weight | approx. 500 g |

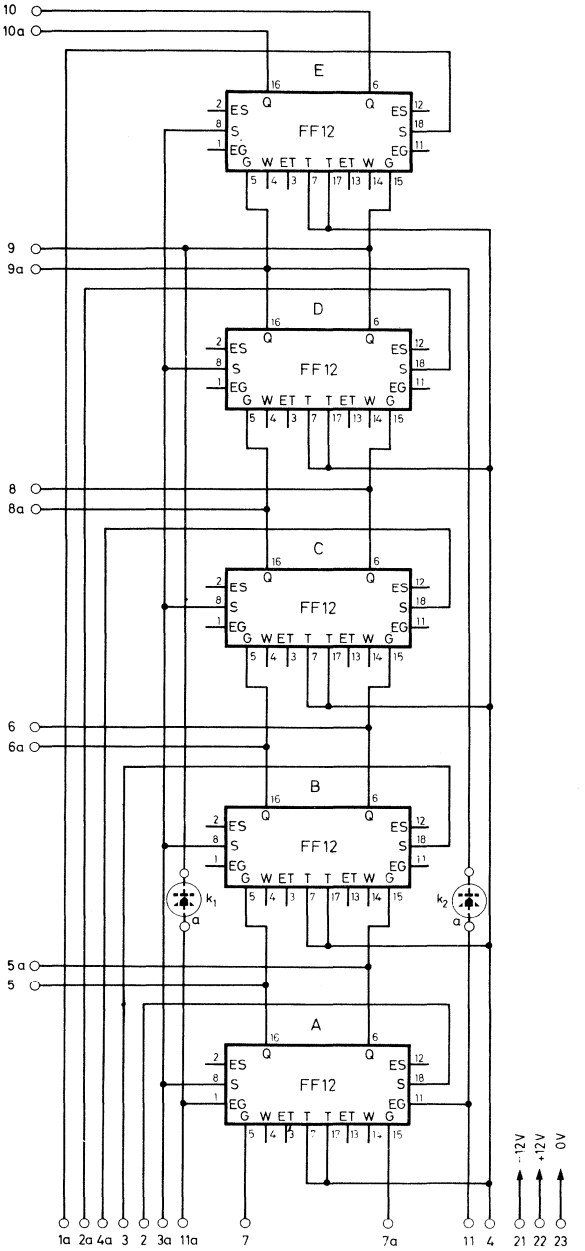

10
10a
E
9
9a
D
8
8a
C
6
6a
B
5a
5
A
FF12
ES
S
EG
Q
W ET T T ET W G
k1
k2
a
-12V
+12V
0V
1a 2a 4a 3 2 3a 11a 7 7a 11 4 21 22 23

Fig.1a

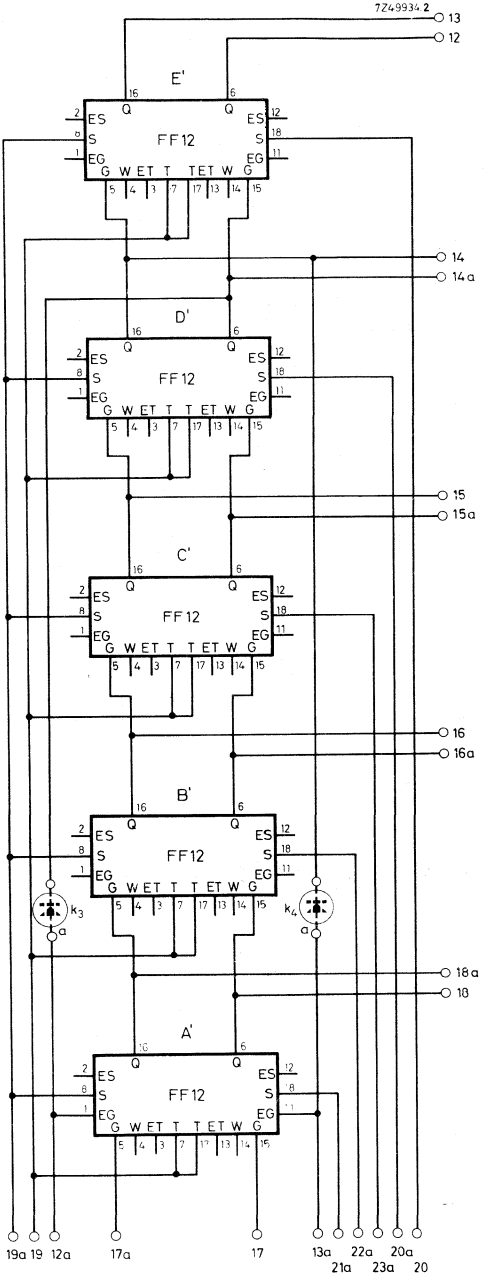

7249934.2
13
12
E'
FF12
14
14a
D'
FF12
15
15a
C'
FF12
16
16a
B'
FF12
18a
18
A'
FF12
19a 19 12a 17a 17 13a 21a 22a 23a 20a 20

Fig.1b

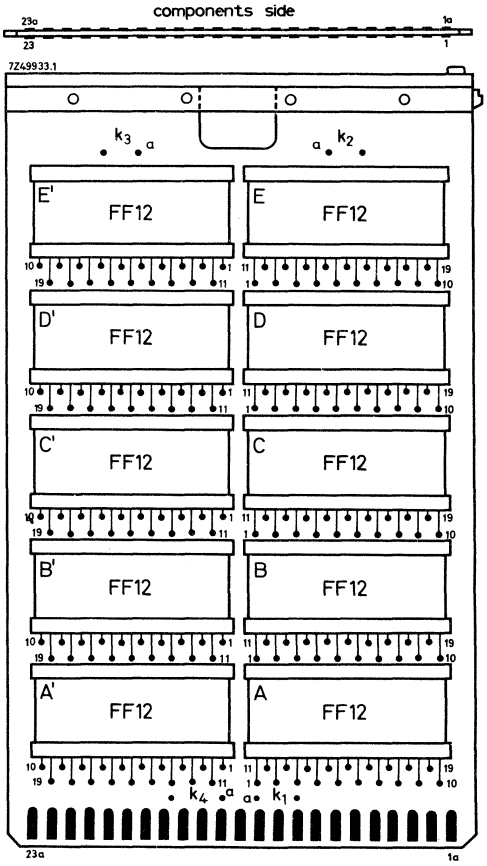



Fig.2

Terminals

1 = not connected
2 = set input S of flip-flop A
3 = set input S of flip-flop B
4 = trigger input T
5 = output $\overline{Q}$ of flip-flop A
6 = output Q of flip-flop B
7 = gate input G of flip-flop A
8 = output Q of flip-flop C
9 = output Q of flip-flop D
10 = output Q of flip-flop E

11 = extension gate input EG of flip-flop A
12 = output Q of flip-flop E'
13 = output $\overline{Q}$ of flip-flop E'
14 = output $\overline{Q}$ of flip-flop D'
15 = output $\overline{Q}$ of flip-flop C'
16 = output $\overline{Q}$ of flip-flop B'
17 = gate input G of flip-flop A'
18 = output Q of flip-flop A'
19 = trigger input T
20 = set input S of flip-flop E'
21 = common negative supply −12 V
22 = common positive supply + 12 V
23 = common supply 0 V

1a = set input S of flip-flop E
2a = set input S of flip-flop D
3a = common reset input S
4a = set input S of flip-flop C
5a = output Q of flip-flop A
6a = output $\overline{Q}$ of flip-flop B
7a = gate input G of flop-flop A
8a = output $\overline{Q}$ of flip-flop C
9a = output $\overline{Q}$ of flip-flop D
10a = output $\overline{Q}$ of flip-flop E
11a = extension gate input EG of flip-flop A
12a = extension gate input EG of flip-flop A'
13a = extension gate input EG of flip-flop A'
14a = output Q of flip-flop D'
15a = output Q of flip-flop C'
16a = output Q of flip-flop B'
17a = gate input G of flip-flop A'
18a = output $\overline{Q}$ of flip-flop A'
19a = common reset input S
20a = set input S of flip-flop D'
21a = set input S of flip-flop A'
22a = set input S of flip-flop B'
23a = set input S of flip-flop C'

Power supply

Terminal 21 : $V_N = -12\ V \pm 5\ \%$, $-I_N = 11\ mA$
22 : $V_P = +12\ V \pm 5\ \%$, $I_P = 70\ mA$
23 : $V_E = 0\ V$ common

} The current values are nominal

INPUT REQUIREMENTS (at $V_P$ = 11.4 V and $V_N$ = −12.6 V, unless specified differently)

Set/reset inputs (S-terminals)

For reset- and preset purposes a "positive low" voltage $V_S$ is required between 0 V and 0.3 V, otherwise this voltage must be kept between $V_P$ and 2/3 $V_P$.

Common reset (terminals 3a and 19a)

With one pulse at these terminals all flip-flops will be reset simultaneously.

| | Ring counter or 5-stages shift register | 10-stages shift register |
|---|---|---|
| Required direct current | $-I_{SD}$ = max. 9.75 mA | = max. 19.50 mA |
| Required transient charge when $V_S$ changes from 2/3 $V_P$ to 0.5 V in 1.5 μs | $-Q_{ST}$ = max. 14 nC | = max. 28 nC |
| Time data | | |
| Pulse duration | $t_p$ = min. 2 μs | = min. 2 μs } See point 4 * |
| Recovery time | $t_{rec}$ = min. 15 μs | = min. 15 μs } See point 4 * |
| Time delay between S- and T-signal | $t_{st}$ = min. 15 μs | = min. 15 μs } See point 5 * |

Individual flip-flop preset (terminals 1a, 2, 2a, 3, 4a and 20, 20a, 21a, 22a, 23a)

For this purpose one S-input of each individual flip-flop in the register(s) has been brought out.

| | |
|---|---|
| Required direct current | $-I_{SD}$ = max. 1.95 mA |
| Required transient charge when $V_S$ changes from 2/3 $V_P$ to 0.5 V in 1.5 μs | $-Q_{ST}$ = max. 2.8 nC |

* Section "Time definitions" of "Circuit blocks 10-Series".

Gate input (G-terminals 7, 7a and 17a, 17)

A d.c. voltage level is applied to terminal G.
A "positive low" voltage closes the gate, whilst a "positive high" voltage (between 2/3 $V_P$ and $V_P$) opens the gate.

| | | | | | |
|---|---|---|---|---|---|
| Gate open | | | | | |
| Voltage | $V_G$ | = | min. 2/3<br>max. | $V_P$<br>$V_P$ | |
| Gate closed | | | | | |
| Voltage | $V_G$ | = | min. 0<br>max. 0.3 | V<br>V | |
| Required direct current | $-I_{GD}$ | = | max. 1.1 | mA | |
| Required transient charge when $V_G$ changes from 2/3 $V_P$ to 0.5 V in 1.5 $\mu$s | $-Q_{GT}$ | = | max. 1.2 | nC | |
| Time data | | | | | |
| Trigger gate setting time | $t_{gs}$ | = | min. 29 | $\mu$s | See point 6 * |
| Trigger gate inhibiting time | $t_{gi}$ | = | min. 29 | $\mu$s | See point 7 * |

Trigger input (T-terminals 4 and 19)

Negative-going trigger pulses have to be applied to the common trigger (shift) terminals 4 and 19.

| | | Ring counter or 5-stages shift register | 10-stages shift register |
|---|---|---|---|
| Required direct current when $V_T$ = max. 0.3 V | $-I_{TD}$ | = max. 5.5 mA | = max.11 mA |
| Required transient charge when $V_T$ changes from 2/3 $V_P$ to 0.5 V in 1.5 $\mu$s | $-Q_{TT}$ | = max. 17 nC | = max.34 nC |
| Time data | | | |
| Fall time | $t_f$ | = max. 1.5 $\mu$s | See point 3 * |
| Pulse duration | $t_p$ | = min. 2 $\mu$s | |
| Trigger gate setting time | $t_{gs}$ | = min. 29 $\mu$s | |
| Time delay between T- and S-signals | $t_{ts}$ | = min. 15 $\mu$s | See point 5 * |

* Section "Time definitions" of "Circuit blocks 10-Series".

OUTPUT DATA (at $V_P$ = 11.4 V and $V_N$ = −12.6 V, unless specified differently)

The available output data of each flip-flop depend on the circuit configuration.

Dual 5-stages one-directional shift register

In excess of the internal load, represented by the circuit blocks, mounted on the printed-wiring board, the Q-outputs of each flip-flop in the shift register may furthermore be loaded as specified in the table below.

| flip-flop | FF 12-A(A') | | FF 12-B(B') | | FF 12-C(C') | | FF 12-D(D') | | FF 12-E(E') | |
|---|---|---|---|---|---|---|---|---|---|---|
| output terminal | $\overline{Q}$ | Q | $\overline{Q}$ | Q | $\overline{Q}$ | Q | $\overline{Q}$ | Q | $\overline{Q}$ | Q |
| | 5(18a) | 5a(18) | 6a(16) | 6(16a) | 8a(15) | 8(15a) | 9a(14) | 9(14a) | 10a(13) | 10(12) |
| available direct current: min. $I_{QD}$ in mA | 7.1 | 7.1 | 7.1 | 7.1 | 7.1 | 7.1 | 7.1 | 7.1 | 8.2 | 8.2 |
| available transient charge when $V_Q$ changes from 2/3 $V_P$ to 0.5 V in 1.5 μs: min. $Q_{QT}$ in nC | 25.8 | 25.8 | 25.8 | 25.8 | 25.8 | 25.8 | 25.8 | 25.8 | 27 | 27 |

For $T_{amb}$ = min. −25 °C the available direct current $I_{QD}$ has to be reduced with 1.6 mA and similarly the available transient charge $Q_{QT}$ with 5 nC.

Dual one-directional decade ring counter

In excess of the internal load (with feedback diodes on $k_1$, $k_2$, $k_3$ and $k_4$), represented by the circuit blocks, mounted on the printed-wiring board, the Q-outputs of each flip-flop in the ring counter may furthermore be loaded as specified in the table below.

| flip-flop | FF 12-A(A') | | FF 12-B(B') | | FF 12-C(C') | | FF 12-D(D') | | FF 12-E(E') | |
|---|---|---|---|---|---|---|---|---|---|---|
| output terminal | $\overline{Q}$ | Q | $\overline{Q}$ | Q | $\overline{Q}$ | Q | $\overline{Q}$ | Q | $\overline{Q}$ | Q |
| | 5(18a) | 5a(18) | 6a(16) | 6(16a) | 8a(15) | 8(15a) | 9a(14) | 9(14a) | 10a(13) | 10(12) |
| available direct current: min. $I_{QD}$ in mA | 7.1 | 7.1 | 7.1 | 7.1 | 7.1 | 7.1 | 6 | 6 | 7.1 | 7.1 |
| available transient charge when $V_Q$ changes from 2/3 $V_P$ to 0.5 V in 1.5 μs: min. $Q_{QT}$ in nC | 25.8 | 25.8 | 25.8 | 25.8 | 25.8 | 25.8 | 24.6 | 24.6 | 25.8 | 25.8 |

For $T_{amb}$ = min. −25 °C the available direct current $I_{QD}$ has to be reduced with 1.6 mA and similarly the available transient charge $Q_{QT}$ with 5 nC.

## Output levels of the flip-flops in a decade ring counter configuration

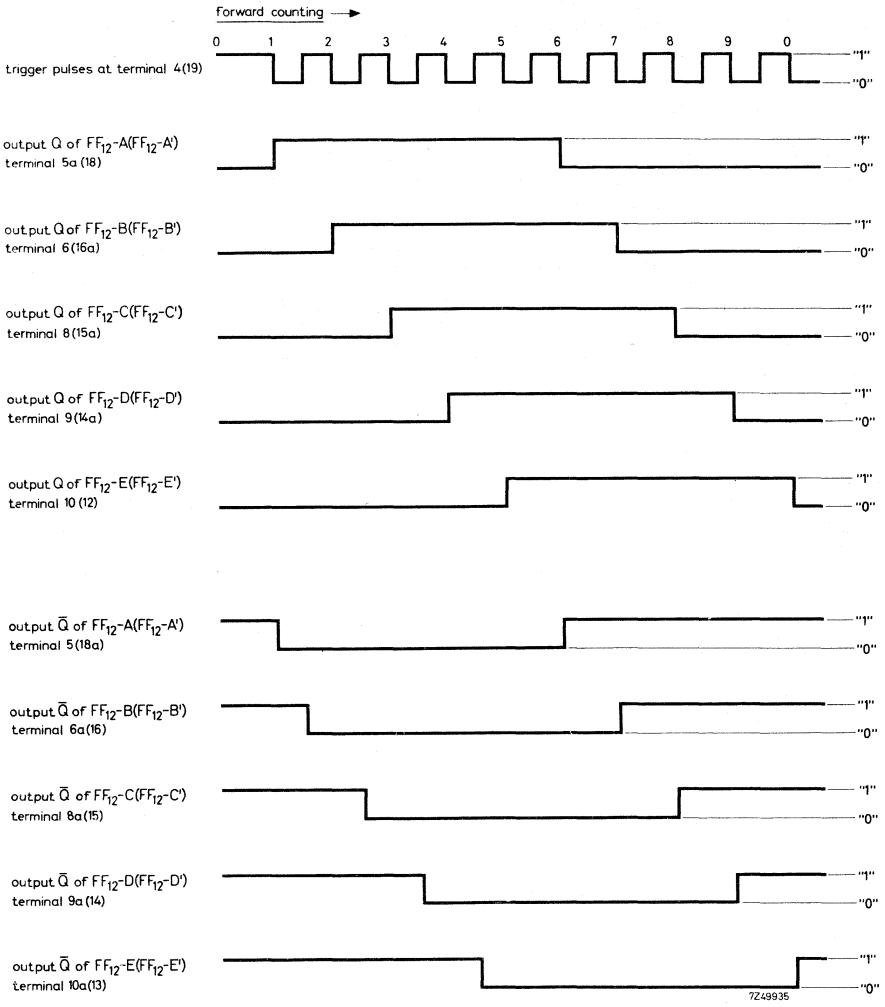



Fig. 3

Note that when a Q-output is at "0" level the corresponding $\overline{Q}$-output is at the "1" level and vice versa.
After 10 trigger (shift) pulses at the trigger input terminal 4 (19), the output terminal 10 (12) delivers one negative-going voltage step, whilst the ring counter has resumed its initial position, namely all Q-outputs being at "0" level.

Single 10-stages one-directional shift register

In excess of the internal load, represented by the circuit blocks, mounted on the printed-wiring board, the Q-outputs of each flip-flop in the shift register may furthermore be loaded as specified in the table below.

| flip-flop | FF 12-A(A') | | FF 12-B(B') | | FF 12-C(C') | | FF 12-D(D') | | FF 12-E(E') | |
|---|---|---|---|---|---|---|---|---|---|---|
| output terminal | $\overline{Q}$ | Q | $\overline{Q}$ | Q | $\overline{Q}$ | Q | $\overline{Q}$ | Q | $\overline{Q}$ | Q |
| | 5(18a) | 5a(18) | 6a(16) | 6(16a) | 8a(15) | 8(15a) | 9a(14) | 9(14a) | 10a(13) | 10(12) |
| available direct current: min. $I_{QD}$ in mA | 7.1 | 7.1 | 7.1 | 7.1 | 7.1 | 7.1 | 7.1 | 7.1 | 7.1(8.2) | 7.1(8.2) |
| available transient charge when $V_Q$ changes from 2/3 $V_P$ to 0.5 V in 1.5 $\mu$s: min. $Q_{QT}$ in nC | 25.8 | 25.8 | 25.8 | 25.8 | 25.8 | 25.8 | 25.8 | 25.8 | 25.8(27) | 25.8(27) |

For $T_{amb}$ = min. −25 °C the available direct current $I_{QD}$ has to be reduced with 1.6 mA and similarly the available transient charge $Q_{QT}$ with 5 nC.

Wiring capacitance at each Q-output max. 175 pF

"Positive high" level

| | | | |
|---|---|---|---|
| Voltage | $V_C$ | = min. 2/3 $V_P$<br>= max. $V_P$ | |

"Positive low" level

| | | | |
|---|---|---|---|
| Voltage | $V_C$ | = min. 0<br>= max. 0.3 | V<br>V |
| Total required direct current | $-I_{CD}$ | = max. 4.4 | mA |
| Total required transient charge when $V_C$ changes from 2/3 $V_P$ to 0.5 V in 1.5 $\mu$s | $-Q_{CT}$ | = max. 4.8 | nC |

Trigger input (terminals 13 and 2a)

For forward counting the trigger pulse has to be applied to terminal 13.
For reverse counting the trigger pulse has to be applied to terminal 2a.

| | | $V_C$ "positive high" | $V_C$ "positive low" |
|---|---|---|---|
| Required direct current when $V_T$ = max. 0.3 V | $-I_{TD}$ | = max. 1.1 mA | = 0 mA |
| Required transient charge when $V_T$ changes from 2/3 $V_P$ to 0.5 V in 1.5 $\mu$s | $-Q_{TT}$ | = max. 3.4 nC | = 0 nC |
| Input noise level | $V_n$ | = max. 1.2 $V_{p-p}$ | |

Time data

| | | | |
|---|---|---|---|
| Fall time | $t_f$ | = max. 1.5 $\mu$s | See point 3 * |
| Pulse duration | $t_p$ | = min. 2 $\mu$s | |
| Trigger gate setting time | $t_{gs}$ | = min. 29 $\mu$s | |

OUTPUT DATA (at $V_P$ = 11.4 V and $V_N$ = −12.6 V, unless specified differently)

Decade counter section

In excess of the internal load, represented by the circuit blocks mounted on the printed-wiring board including the numerical indicator tube driver ID 10, the Q-outputs of each flip-flop in the decade counter may furthermore be loaded as specified in the following table.

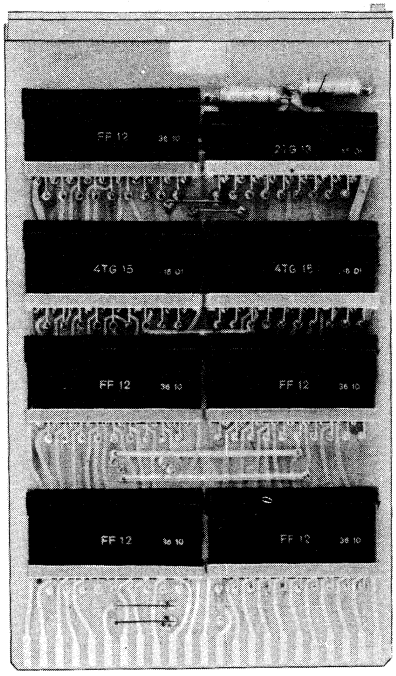
* Section "Time definitions" of "Circuit blocks 10-Series".

The loadability of the flip-flops FF 12-A, FF 12-C and FF 12-D can be increased by connecting an external resistor of 51 kΩ ±5% in parallel with the built-in collector resistor of the corresponding output, as specified in the table below. This resistor has to be connected between the output terminal and $V_P$.

| flip-flop | | FF 12-A | | FF 12-B | | FF 12-C | | FF 12-D | |
|---|---|---|---|---|---|---|---|---|---|
| output terminal | | $\overline{Q}$ | Q | $\overline{Q}$ | Q | $\overline{Q}$ | Q | $\overline{Q}$ | Q |
| | | 3 | 3a | 8a | 9a | 10a | 4a | 6a | 5a |
| max. number of 10-series circuit blocks, that may be driven, provided each driven input represents a load of $-I_D$ = max. 1.1 mA and $-Q_T$ = max. 3.4 nC | $T_{amb}$ = min. 0 °C | 1 | 1 | 2 | 3 | 2 | 1 | 2 | 4 |
| | $T_{amb}$ = min. −25 °C | 1 | 1 | 1 | 2 | 1 | 1 | 1 | 4 |
| max. number of driven 10-series circuit blocks with external parallel collector resistor(s) | $T_{amb}$ = min. 0 °C | 3 | 3 | 2 | 3 | 2 | 3 | 2 | 5 |
| | $T_{amb}$ = min. −25 °C | 2 | 2 | 1 | 2 | 1 | 2 | 1 | 4 |

Wiring capacitance at each Q-output max. 150 pF

# REVERSIBLE SHIFT REGISTER ASSEMBLY




RZ 22752-2

This assembly can be applied to fulfil three major functions as described below.

5-stages reversible shift register (see Figs.1 and 2)

For this function the gate inputs G of the trigger gates 4.TG 15 have to be interconnected externally with the corresponding Q-outputs of the flip-flops FF 12-B up to and including FF 12-E.
The necessary interconnections are:

terminal 10a with 3a
terminal 9a with 4a
terminal 9 with 17
terminal 2a with 17a
terminal 14a with 18
terminal 14 with 18a
terminal 19 with 21a
terminal 19a with 22a

The following signals have to be applied for forward and reverse shifting:

Forward shifting

The information that has to be shifted in the register, has to be applied to the gate inputs G of flip-flop FF 12-A (terminals 7 and 7a).
The trigger pulse has to be applied to the common trigger line of the flip-flops FF 12-A up to and including FF 12-E (terminal 4).

Reverse shifting

The information that has to be shifted in the register, has to be applied to the gate inputs G of the trigger gate 2. TG 13 (terminals 12 and 12a).
The trigger pulse has to be applied to the common trigger line of the trigger gates 4. TG 15 and 2. TG 13 (terminal 13).

The positions $k_1$, $k_2$, $k_3$ and $k_4$ on the printed-wiring board have to be left open.

Reversible decade ring counter (see Figs. 1 and 2)

For this function the interconnections as specified above remain unchanged. Moreover the Q-outputs of flip-flop FF 12-E have to be cross-connected externally with the gate inputs G of flip-flop FF 12-A, while the Q-outputs of flip-flop FF 12-A have to be cross-connected with the gate inputs G of trigger gate 2. TG 13.

The necessary interconnections are:

terminal 21a with 7a
terminal 22a with 7
terminal 6 with 12a
terminal 5 with 12

Trigger pulses for forward counting have to be applied to the common trigger line of the flip-flops FF 12-A up to and including FF 12-E (terminal 4); for reverse counting the trigger pulses have to be applied to the common trigger line of the trigger gates 4. TG 15 and 2. TG 13 (terminal 13).

Any disturbance in the code sequence can automatically be corrected after maximum one cycle of 10 pulses, by mounting on the printed-wiring board two diodes AAY21 for each counting direction. In Fig. 2 the diode positions are indicated as $k_1$, $k_2$, $k_3$ and $k_4$; the diodes have to be mounted with the anode located at "a". If these correction circuits are applied, the EG-terminals 11 and 11a may not be used for blocking purposes of flip-flop FF 12-A.

One-directional shift register with additional inputs for parallel information shift (see Figs. 1 and 2)

When information has to be inserted in the shift register in a parallel way, the binary signals have to be applied to the following terminals:

10a and 9a for flip flop FF 12-A
9 and 2a for flip flop FF 12-B
14a and 14 for flip-flop FF 12-C
19 and 19a for flip-flop FF 12-D
12 and 12a for flip-flop FF 12-E.

With one shift pulse at the common trigger line (terminal 13) the externally applied information is shifted into the shift register.
Therefore the shift register is suitable for serial-parallel work.
The positions $k_1$, $k_2$, $k_3$ and $k_4$ on the printed-wiring board have to be left open.

The capacitors $C_1$ and $C_2$ are mounted on the printed-wiring board for noise filtering purposes of the supply lines.

The bare printed-wiring board (catalog number 4322 026 38750), provided with plated-through holes and double-sided goldplated contacts, is made of glass-epoxy material. Moreover, the printed-wiring board is delivered with an extractor and a locking device. With the mating connector (catalog number 2422 020 52591), not supplied with the assembly, the printed-wiring board of standard dimensions (121.8 mm x 207.0 mm x 1.6 mm) can be used directly in the standard mounting chassis (catalog number 4322 026 38240).

The circuit blocks are secured to the printed-wiring board by means of locking caps (catalog number 4322 026 32150).

| | |
|---|---|
| Counting rate | max. 30 kHz |
| Ambient-temperature range | |
| operating | −25 to +55 °C<br>below 0 °C: derated output data |
| storage | −55 to +75 °C |
| Weight | approx. 400 g |

CIRCUIT DATA

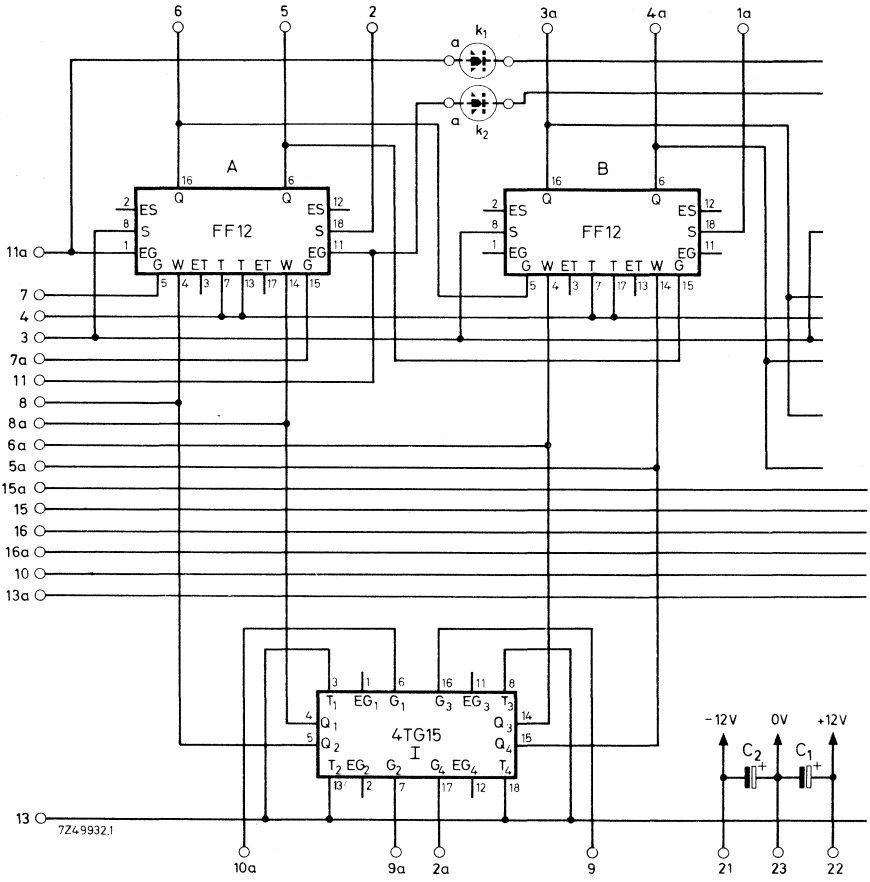



Fig. 1a

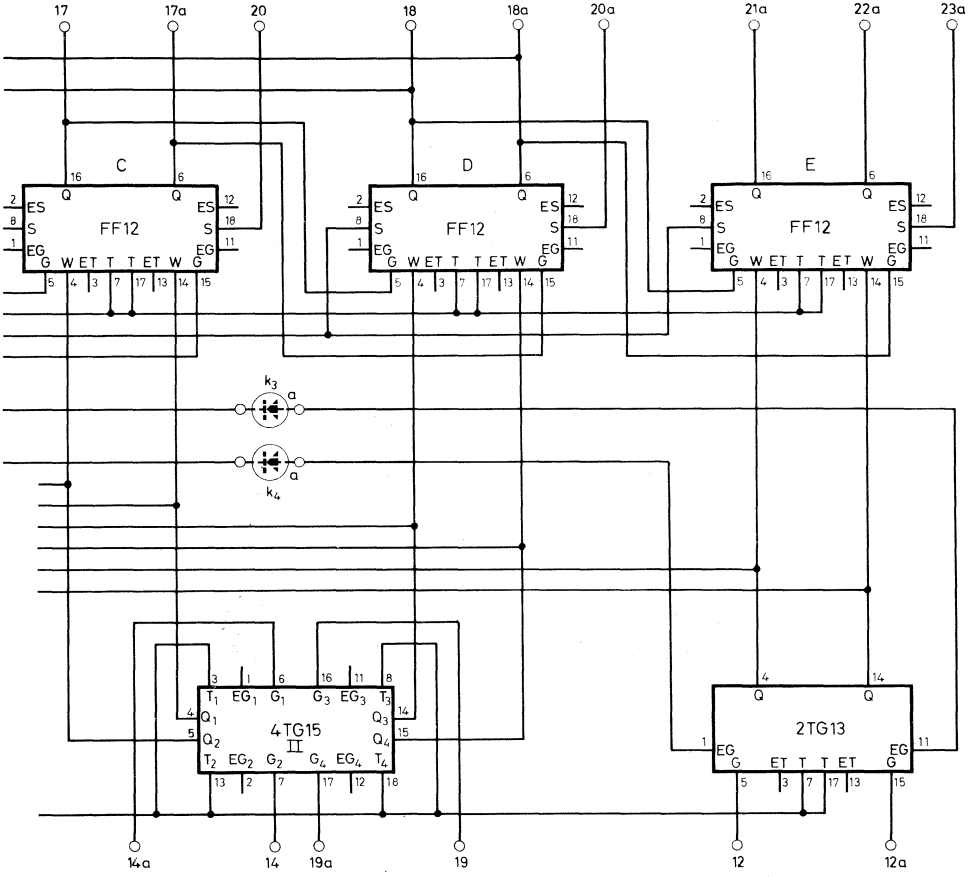

17
17a
20
18
18a
20a
21a
22a
23a
C
D
E
FF12
FF12
FF12
ES
S
EG
Q
G W ET T T ET W G
$k_3$
$k_4$
a
4TG15
II
2TG13
14a
14
19a
19
12
12a

Fig. 1b

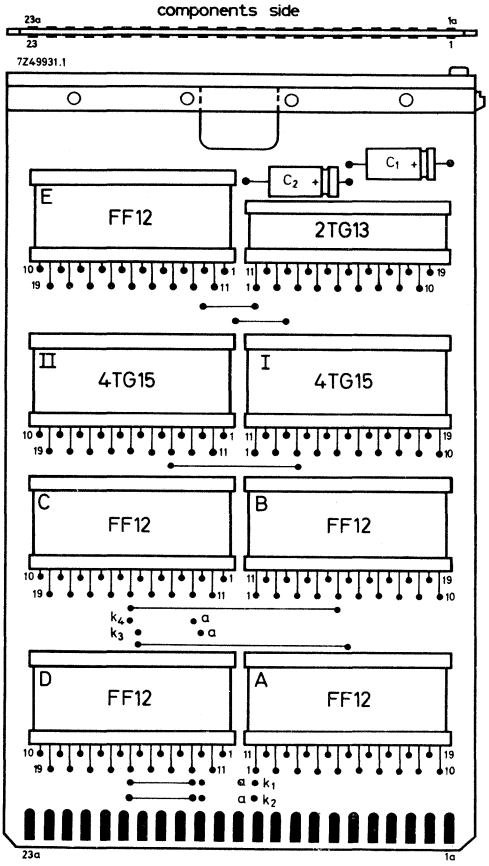



Fig.2

Terminals

1 = not connected
2 = set input S of flip-flop A
3 = common set input S
4 = trigger input for forward counting
5 = output Q of flip-flop A
6 = output $\overline{Q}$ of flip-flop A
7 = gate input G of flip-flop A
8 = base input W of flip-flop A
9 = gate input G of 4.TG 15-I
10 = base input W of flip-flop E

11 = extension gate input EG of flip-flop A
12 = gate input G of 2.TG 13
13 = trigger input for reverse counting
14 = gate input G of 4.TG 15-II
15 = base input W of flip-flop C
16 = base input W of flip-flop D
17 = output $\overline{Q}$ of flip-flop C
18 = output $\overline{Q}$ of flip-flop D
19 = gate input G of 4.TG 15-II
20 = set input S of flip-flop C
21 = common negative supply −12 V
22 = common positive supply +12 V
23 = common supply 0 V

1a = set input S of flip-flop B
2a = gate input G of 4.TG 15-I
3a = output $\overline{Q}$ of flip-flop B
4a = output Q of flip-flop B
5a = base input W of flip-flop B
6a = base input W of flip-flop B
7a = gate input G of flip-flop A
8a = base input W of flip-flop A
9a = gate input G of 4.TG 15-I
10a = gate input G of 4.TG 15-I
11a = extension gate input EG of flip-flop A
12a = gate input G of 2.TG 13
13a = base input W of flip-flop E
14a = gate input G of 4.TG 15-II
15a = base input W of flip-flop C
16a = base input W of flip-flop D
17a = output Q of flip-flop C
18a = output Q of flip-flop D
19a = gate input G of 4.TG 15-II
20a = set input S of flip-flop D
21a = output $\overline{Q}$ of flip-flop E
22a = output Q of flip-flop E
23a = set input S of flip-flop E

Power supply

Terminal 21 : $V_N = -12\ V \pm 5\%$, $-I_N = 9.0$ mA
22 : $V_P = +12\ V \pm 5\%$, $I_P = 45$ mA
} The current values are nominal
23 : $V_E = 0$ V common

INPUT REQUIREMENTS (at $V_P$ = 11.4 V and $V_N$ = -12.6 V unless specified differently)

Set/reset inputs (S-terminals)

For reset- or preset purposes a "positive low" voltage $V_S$ is required between 0 V and 0.3 V, otherwise this voltage must be kept between $V_P$ and 2/3 $V_P$.

Common reset (terminal 3)

With one pulse at terminal 3 all flip-flops will be reset simultaneously.

| | | | |
|---|---|---|---|
| Required direct current | $-I_{SD}$ = max. 9.75 mA | | |
| Required transient charge when $V_S$ changes from 2/3 $V_P$ to 0.5 V in 1.5 $\mu$s | $-Q_{ST}$ = max. 14 nC | | |
| Time data | | | |
| Pulse duration | $t_p$ = min. 2 $\mu$s | } | See point 4* |
| Recovery time | $t_{rec}$ = min. 15 $\mu$s | } | |
| Time delay between S- and T-signal | $t_{st}$ = min. 15 $\mu$s | | See point 5* |

Individual flip-flop preset (terminals 2, 1a, 20, 20a and 23a)

For this purpose one S-input of each flip-flop in the register has been brought out.

| | | |
|---|---|---|
| Required direct current | $-I_{SD}$ = max. 1.95 mA | |
| Required transient charge when $V_S$ changes from 2/3 $V_P$ to 0.5 V in 1.5 $\mu$s | $-Q_{ST}$ = max. 2.8 nC | |

Gate input (G-terminals)

A d.c. voltage level is applied to terminal G.
A "positive low" voltage closes the gate, whilst a "positive high" voltage (between 2/3 $V_P$ and $V_P$) opens the gate.

| | | |
|---|---|---|
| Gate open | | |
| Voltage | $V_G$ = min. 2/3 $V_P$, max. $V_P$ | |
| Gate closed | | |
| Voltage | $V_G$ = min. 0 V, max. 0.3 V | |
| Required direct current | $-I_{GD}$ = max. 1.1 mA | |
| Required transient charge when $V_G$ changes from 2/3 $V_P$ to 0.5 V in 1.5 $\mu$s | $-Q_{GT}$ = max. 1.2 nC | |

* Section "Time definitions" of "Circuit blocks 10-Series".

Time data

| | | |
|---|---|---|
| Trigger gate setting time | $t_{gs}$ = min. 29 $\mu$s | See point 6 * |
| Trigger gate inhibiting time | $t_{gi}$ = min. 29 $\mu$s | See point 7 * |

Trigger input (T-terminals 4 and 13)

For forward counting or shifting the trigger pulses have to be applied to common trigger terminal 4. For reverse counting or shifting the trigger pulses have to be applied to common trigger terminal 13.

| | | | |
|---|---|---|---|
| Required direct current when $V_T$ = max. 0.3 V | $-I_{TD}$ = max. 5.5 | mA | |
| Required transient charge when $V_T$ changes from 2/3 $V_P$ to 0.5 V in 1.5 $\mu$s | $-Q_{TT}$ = max. 17 | nC | |
| Input noise level | $V_n$ = max. 1.2 | $V_{p-p}$ | |

Time data

| | | | |
|---|---|---|---|
| Fall time | $t_f$ = max. 1.5 | $\mu$s | See point 3 * |
| Pulse duration | $t_p$ = min. 2 | $\mu$s | |
| Trigger gate setting time | $t_{gs}$ = min. 29 | $\mu$s | |
| Time delay between T- and S-signals | $t_{ts}$ = min. 15 | $\mu$s | See point 5 * |

Base input (W-terminal)

Capacitance (wiring plus output of TG 13, TG 14 or TG 15) max. 80 pF

Note

The output capacitance of the trigger gates TG 13, TG 14 and TG 15 is max. 5 pF.

OUTPUT DATA (at $V_P$ = 11.4 V and $V_N$ = −12.6 V, unless specified differently)

The available output data of each flip-flop depend on the circuit configuration.

Reversible shift register

In excess of the internal load, represented by the circuit blocks, mounted on the printed-wiring board, the Q-outputs of each flip-flop in the shift register may furthermore be loaded as specified in the table on next page.

---

* Section "Time definitions" of "Circuit blocks 10-Series".

| flip-flop | FF 12-A | | FF 12-B | | FF 12-C | | FF 12-D | | FF 12-E | |
|---|---|---|---|---|---|---|---|---|---|---|
| output terminal | $\overline{Q}$ | Q | $\overline{Q}$ | Q | $\overline{Q}$ | Q | $\overline{Q}$ | Q | $\overline{Q}$ | Q |
| | 6 | 5 | 3a | 4a | 17 | 17a | 18 | 18a | 21a | 22a |
| available direct current: min. $I_{QD}$ in mA | 7.1 | 7.1 | 6 | 6 | 6 | 6 | 6 | 6 | 7.1 | 7.1 |
| available transient charge when $V_Q$ changes from 2/3 $V_P$ to 0.5 V in 1.5 $\mu$s: min. $Q_{QT}$ in nC | 25.8 | 25.8 | 24.6 | 24.6 | 24.6 | 24.6 | 24.6 | 24.6 | 25.8 | 25.8 |

For $T_{amb}$ = min. −25 °C the available direct current $I_{QD}$ has to be reduced with 1.6 mA and similarly the available transient charge $Q_{QT}$ with 5 nC.

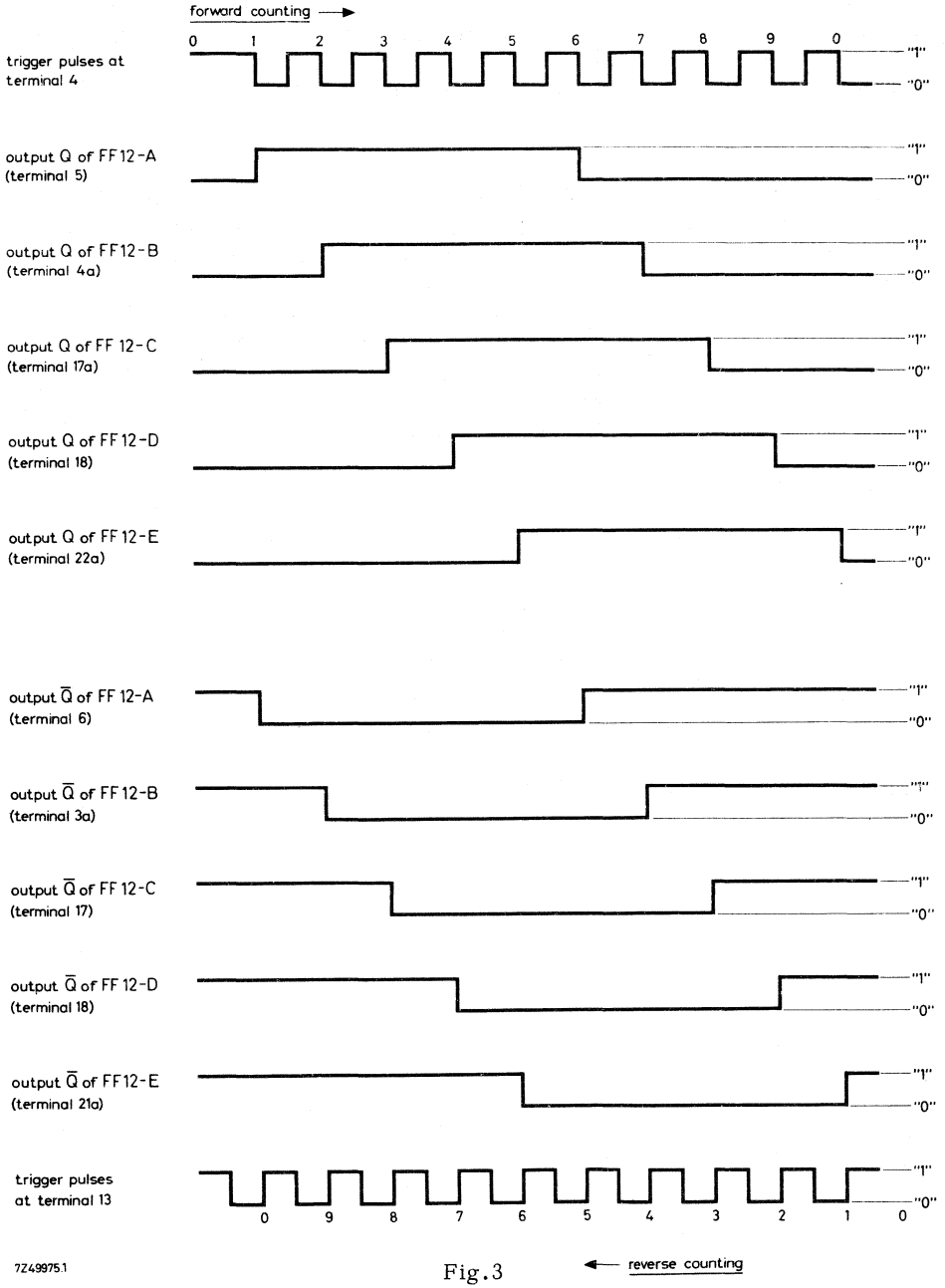
Reversible decade ring counter

In excess of the internal load (with feedback diodes on $k_1$, $k_2$, $k_3$ and $k_4$), represented by the circuit blocks mounted on the printed-wiring board, the Q-outputs of each flip-flop in the ring counter may furthermore be loaded as specified in the table below.

| flip-flop | FF 12-A | | FF 12-B | | FF 12-C | | FF 12-D | | FF 12-E | |
|---|---|---|---|---|---|---|---|---|---|---|
| output terminal | $\overline{Q}$ | Q | $\overline{Q}$ | Q | $\overline{Q}$ | Q | $\overline{Q}$ | Q | $\overline{Q}$ | Q |
| | 6 | 5 | 3a | 4a | 17 | 17a | 18 | 18a | 21a | 22a |
| available direct current: min. $I_{QD}$ in mA | 6 | 6 | 4.9 | 4.9 | 6 | 6 | 4.9 | 4.9 | 6 | 6 |
| available transient charge when $V_Q$ changes from 2/3 $V_P$ to 0.5 V in 1.5 $\mu$s: min. $Q_{QT}$ in nC | 24.6 | 24.6 | 23.4 | 23.4 | 24.6 | 24.6 | 23.4 | 23.4 | 24.6 | 24.6 |

For $T_{amb}$ = min. −25 °C the available direct current $I_{QD}$ has to be reduced with 1.6 mA and similarly the available transient charge $Q_{QT}$ with 5 nC.

Output levels of the flip-flops in a reversible decade ring counter configuration




7Z49975.1

Fig.3

Note that when a Q-output is at "0" level the corresponding $\overline{Q}$-output is at the "1" level and vice-versa. After 10 trigger (shift) pulses at the trigger input terminal 4 (13), the output terminal 22a (5) delivers one negative-going voltage step, whilst the ring counter has resumed its initial position, namely all Q-outputs being at "0" level.

One-directional shift register with additional inputs for parallel information shift

In excess of the internal load, represented by the circuit blocks mounted on the printed-wiring board, the Q-outputs of each flip-flop in the shift register may furthermore be loaded as specified in the table below.

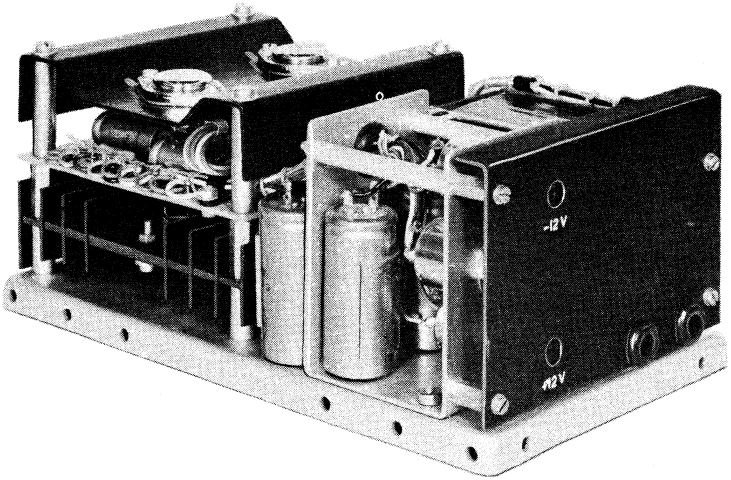
| flip-flop | FF 12-A | | FF 12-B | | FF 12-C | | FF 12-D | | FF 12-E | |
|---|---|---|---|---|---|---|---|---|---|---|
| output terminal | $\overline{Q}$ | Q | $\overline{Q}$ | Q | $\overline{Q}$ | Q | $\overline{Q}$ | Q | $\overline{Q}$ | Q |
| | 6 | 5 | 3a | 4a | 17 | 17a | 18 | 18a | 21a | 22a |
| available direct current: min. $I_{QD}$ in mA | 7.1 | 7.1 | 7.1 | 7.1 | 7.1 | 7.1 | 7.1 | 7.1 | 8.2 | 8.2 |
| available transient charge when $V_Q$ changes from 2/3 $V_P$ to 0.5 V in 1.5 $\mu$s: min. $Q_{QT}$ in nC | 25.8 | 25.8 | 25.8 | 25.8 | 25.8 | 25.8 | 25.8 | 25.8 | 27 | 27 |

For $T_{amb}$ = min. −25 °C the available direct current $I_{QD}$ has to be reduced with 1.6 mA and similarly the available transient charge $Q_{QT}$ with 5 nC.

Wiring capacitance at each Q-output max. 150 pF

# ACCESSORIES FOR CIRCUIT BLOCKS
# 10—SERIES

# POWER SUPPLY UNIT




W 10143/B

| | |
|---|---|
| Input voltage | 105 $V_{ac}$ to 120 $V_{ac}$ and<br>200 $V_{ac}$ to 240 $V_{ac}$ in steps of 5 V |
| Output voltage | +12 $V_{dc}$ and −12 $V_{dc}$ |

## APPLICATION

This power supply unit has been designed for use with the circuit blocks of the 10-series. However it is also suitable as a supply for other transistorised circuits.

## CONSTRUCTION

The unit is dimensioned for mounting in the 19" chassis 4322 026 38240.

The base plate of the unit functions as a side plate of this chassis, so that replacement of the side plate is made when the unit is mounted in the chassis. The power supply unit occupies the same space as five printed-wiring boards.

| | | |
|---|---|---|
| Dimensions | 214 x 123 x 91 | mm |
| Weight | 2.1 | kg |

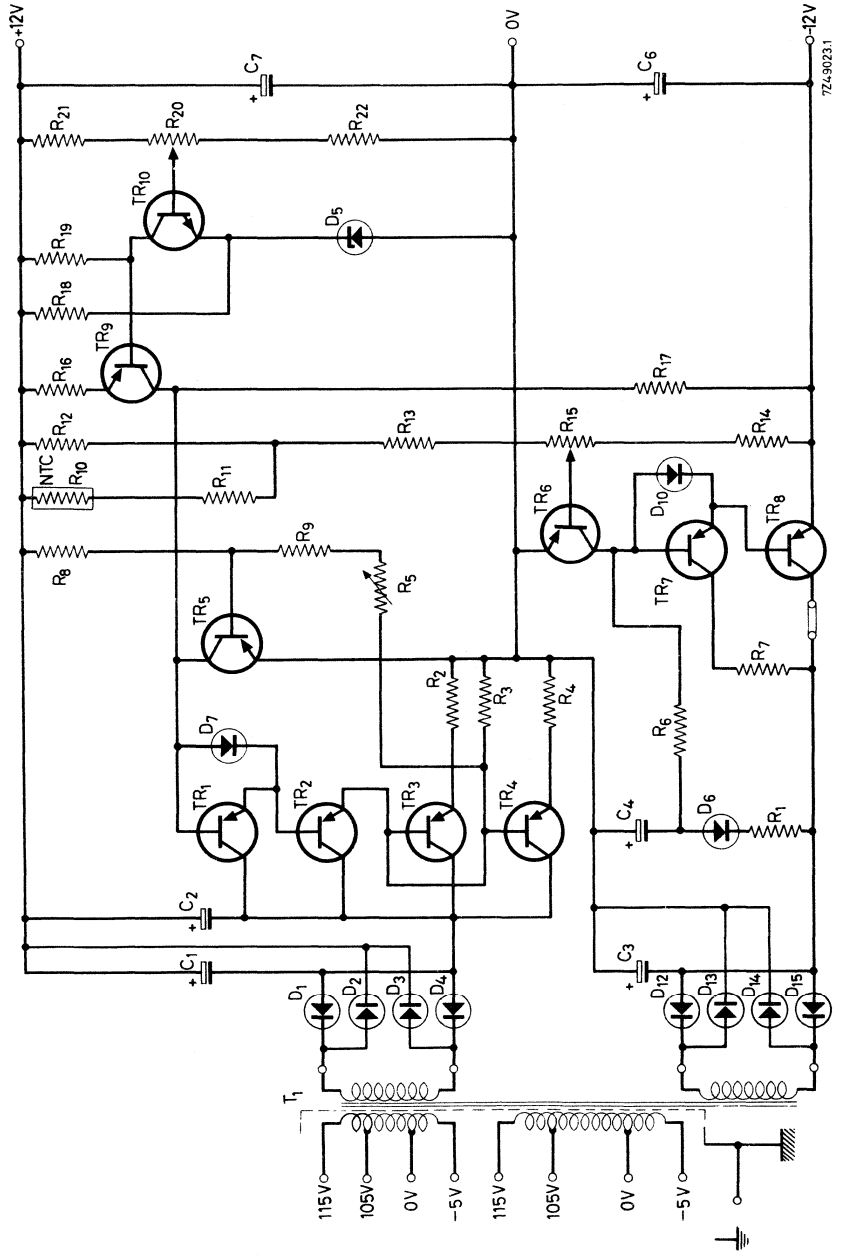
TECHNICAL PERFORMANCE

| | | |
|---|---|---|
| Input voltage | 105 to 120 $V_{ac}$, 200 to 240 $V_{ac}$ in steps of 5 V | |
| Frequency | 45 to 65 Hz | |
| **−12 V output [1])** | | |
| Output voltage | −12 V, adjustable ±10 % (R15, see diagram) | |
| Output current | 400 | mA |
| Stability ratio at 220 V | 350:1 | |
| Ripple voltage | 5 | $mV_{rms}$ |
| Output resistance | 0.4 | Ω |
| Output impedance at 10 kHz | 0.15 | Ω |
| Temperature coefficient | −1.2 | mV/deg C |
| **+12 V output [1])** | | |
| Output voltage | 12 V, adjustable ±10 % (R20, see diagram) | |
| Output current | 1000 | mA |
| Stability ratio at 220 V | 1000:1 | |
| Ripple voltage | 2 | $mV_{rms}$ |
| Output resistance | 0.08 | Ω |
| Output impedance at 10 kHz | 0.1 | Ω |
| Temperature coefficient | +1.2 | mV/deg C |
| Fusing | automatic | |
| Operating-temperature range | −20 to +55 | °C |
| Storage-temperature range | −20 to +75 | °C |

In systems requiring more than one power supply unit, the earth tags (marked "0 V") may be interconnected, the positive tags (marked "+12 V") and the negative tags (marked "−12 V") must remain strictly separated.

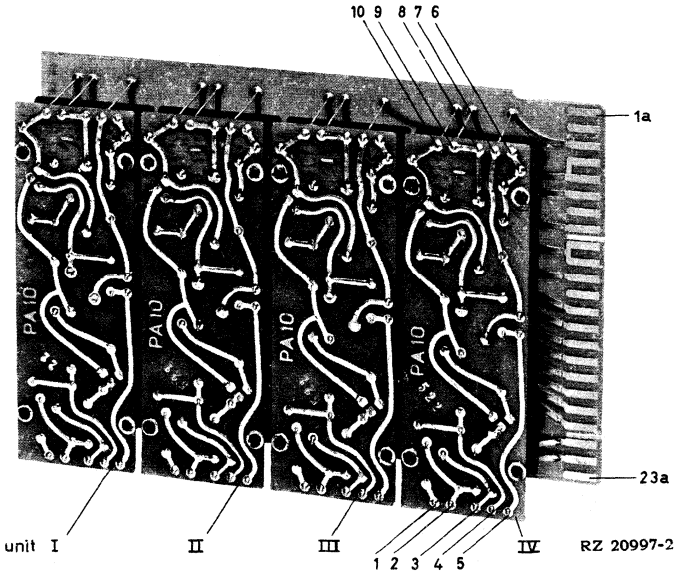
When a system is put into operation for the first time, the output voltages of the power supply units have to be adjusted to 12 V under nominal system load.

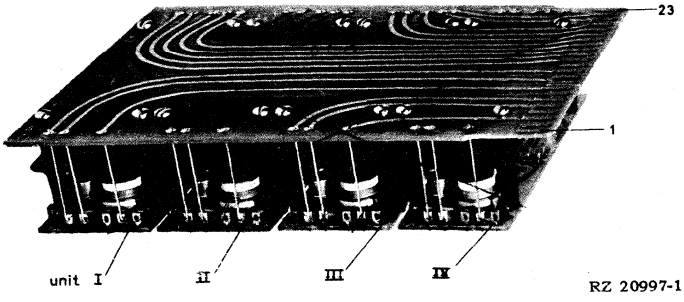
1) All values are given for full load.


+12V
0V
-12V
7Z49023.1
C7
C6
R21
R20
R22
TR10
D5
R19
R18
TR9
R16
R17
R12
R13
R15
R14
NTC
R10
R11
TR6
D10
TR8
TR7
R8
R9
R5
TR5
R2
R3
R4
R7
D7
R6
TR1
TR2
TR3
TR4
C4
D6
R1
C2
C1
C3
D1
D2
D3
D4
D12
D13
D14
D15
T1
115V
105V
0V
-5V
115V
105V
0V
-5V

# PRINTED—WIRING BOARD FOR FOUR UNITS PA 10

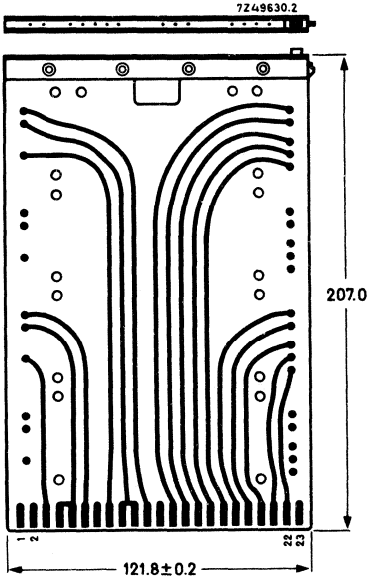
This printed-wiring board fits the mounting chassis 4322 026 38240. It can be used directly with the aid of the mating connector with double sided contacts 2422 020 52591. On this board up to four PA 10's can be mounted, the next position in the chassis being left empty.

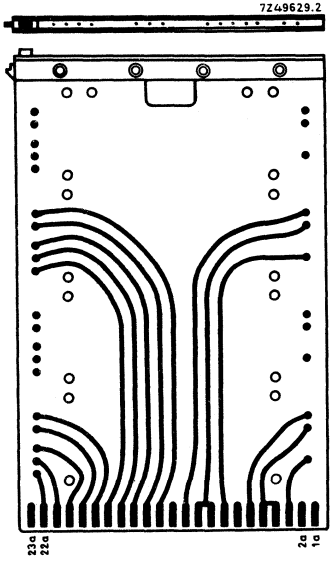


Terminal location:

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 1 | = not connected | | | 1a | = not connected | | |
| 2 | = not connected | | | 2a | = not connected | | |
| 3 | = $E_2$ = common supply 0 V | | | 3a | = $E_2$ = common supply 0 V | | |
| 4 | = $N_2$ | | unit nr. III | 4a | = $N_2$ | | unit nr. IV |
| 5 | = $N_21$ = supply max. 55 V | | | 5a | = $N_21$ = supply max. 55 V | | |
| 6 | = Q = output PA 10 | | | 6a | = Q = output PA 10 | | |
| 7 | = not connected | | | 7a | = not connected | | |
| 8 | = $E_2$ = common supply 0 V | | | 8a | = $E_2$ = common supply 0 V | | |
| 9 | = $N_2$ | | unit nr. I | 9a | = $N_2$ | | unit nr. II |
| 10 | = $N_21$ = supply max. 55 V | | | 10a | = $N_21$ = supply max. 55 V | | |
| 11 | = Q = output PA 10 | | | 11a | = Q = output PA 10 | | |
| 12 | = not connected | | | 12a | = not connected | | |
| 13 | = G = input PA 10 | | | 13a | = G = input PA 10 | | |
| 14 | = EG = extension input PA 10 | | unit nr. I | 14a | = EG = extension input PA 10 | | unit nr. II |
| 15 | = $N_1$ = supply −12 V | | | 15a | = $N_1$ = supply −12 V | | |
| 16 | = P = supply +12 V | | | 16a | = P = supply +12 V | | |
| 17 | = $E_1$ = common supply 0 V | | | 17a | = $E_1$ = common supply 0 V | | |
| 18 | = G = input PA 10 | | | 18a | = G = input PA 10 | | |
| 19 | = EG = extension input PA 10 | | unit nr. III | 19a | = EG = extension input PA 10 | | unit nr. IV |
| 20 | = $N_1$ = supply −12 V | | | 20a | = $N_1$ = supply −12 V | | |
| 21 | = P = supply +12 V | | | 21a | = P = supply +12 V | | |
| 22 | = $E_1$ = common supply 0 V | | | 22a | = $E_1$ = common supply 0 V | | |
| 23 | = not connected | | | 23a | = not connected | | |

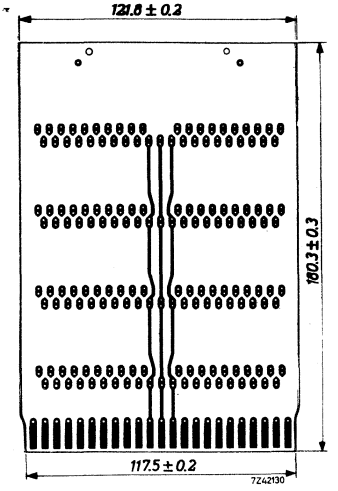



Material glass expoxy
Contacts 2x23, gold plated, pitch 0.2 inch

# PRINTED—WIRING BOARD

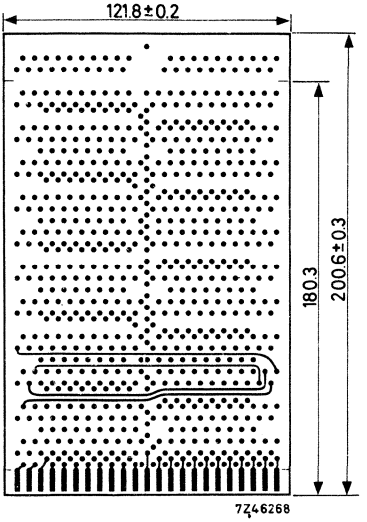
This printed-wiring board for 10-Series circuit blocks fits the mounting chassis 4322 026 38240.

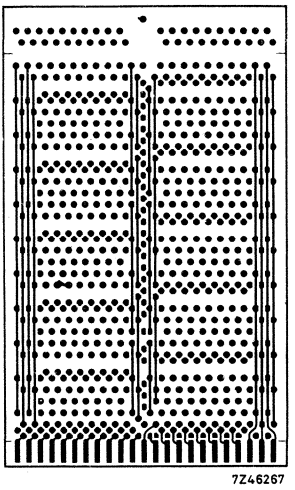



| | |
|---|---|
| Material | copper-clad phenolic resin bonded paper with plated-through holes |
| Hole diameter | 1.2 mm |
| Contacts | 1 x 23, gold plated, pitch 0.2 inch |

# EXPERIMENTERS' PRINTED—WIRING BOARD

This experimenters' printed-wiring board for 10-Series circuit blocks can accommodate a maximum of 10 blocks (low cases) or 8 blocks (high cases) mounted horizontally.
The board fits the mounting chassis 4322 026 38240.

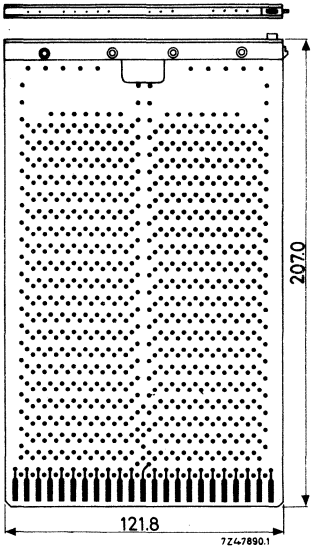


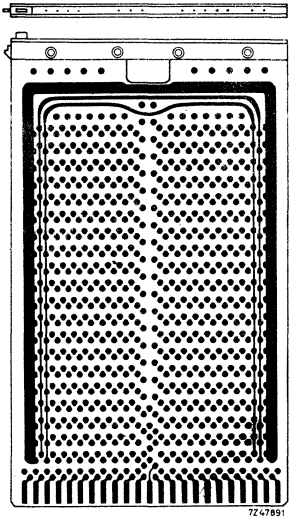




| | |
|---|---|
| Material | phenolic resin bonded paper with plated-through holes |
| Hole diameter | 1.2 mm |
| Contacts | 2x23, gold plated, pitch 0.2 inch |

# EXPERIMENTERS' PRINTED–WIRING BOARDS

These experimenters' printed-wiring boards (with extractor) for 10-Series circuit blocks can accommodate a maximum of 20 blocks mounted vertically or 6 to 12 blocks mounted horizontally at most (depending on how many of these are high and how many are low). The boards fit the mounting chassis 4322 026 38240.

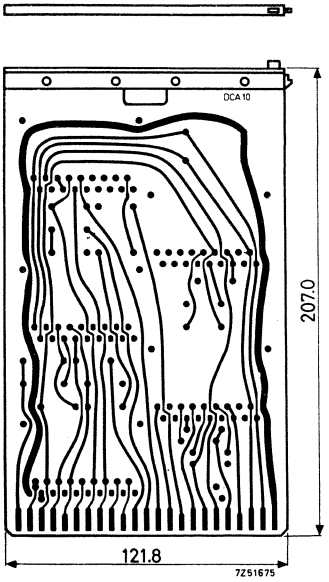


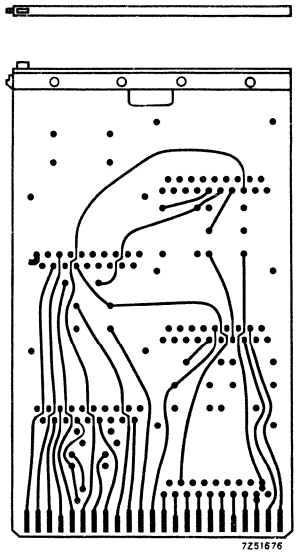




| | | |
|---|---|---|
| Catalogue number | 4322 026 38600 | 4322 026 38610 |
| Material | glass epoxy | phenolic resin bonded paper |
| Holes | plated-through; 1.2 mm diameter | |
| Contacts | 2 x 23, gold plated, pitch 0.2 inch | |

# PRINTED-WIRING BOARD OF DCA 10

This printed-wiring board (with extractor) of the assembly DCA 10 fits the mounting chassis 4322 026 38240.

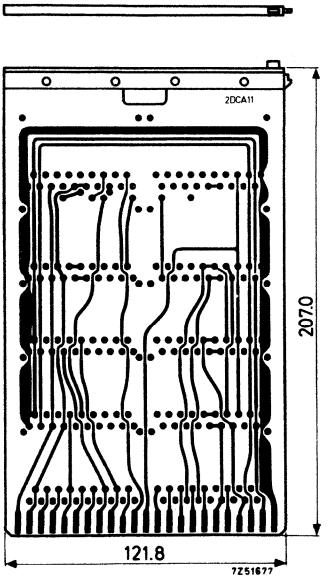


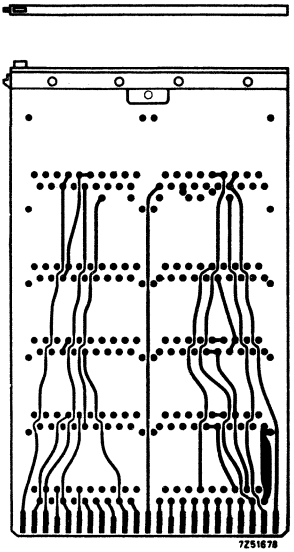




| | |
|---|---|
| Material | glass epoxy with plated-through holes |
| Contacts | 2 x 23, gold plated, pitch 0.2 inch |

# PRINTED-WIRING BOARD OF 2.DCA 11

This printed-wiring board (with extractor) of the assembly 2.DCA 11 fits the mounting chassis 4322 026 38240.

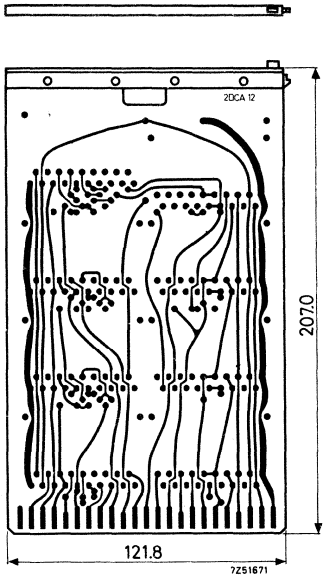


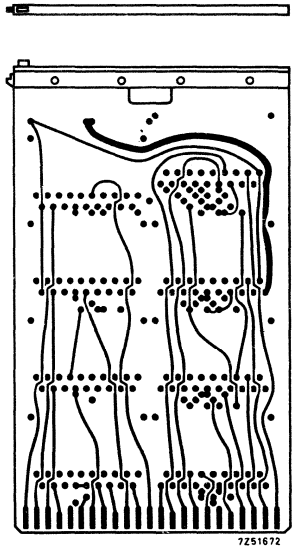




| | |
|---|---|
| Material | glass epoxy with plated-through holes |
| Contacts | 2 x 23, gold plated, pitch 0.2 inch |

# PRINTED-WIRING BOARD OF 2.DCA 12

This printed-wiring board (with extractor) of the assembly 2.DCA 12 fits the mounting chassis 4322 026 38240.

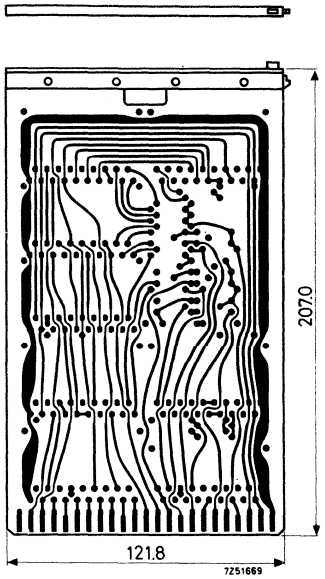


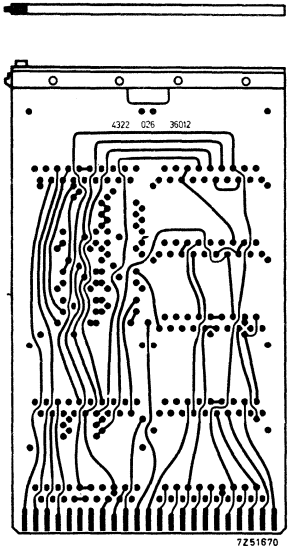




| | |
|---|---|
| Material | glass epoxy with plated-through holes |
| Contacts | 2 x 23, gold plated, pitch 0.2 inch |

# PRINTED-WIRING BOARD OF BCA 10

This printed-wiring board (with extractor) of the assembly BCA 10 fits the mounting chassis 4322 026 38240.

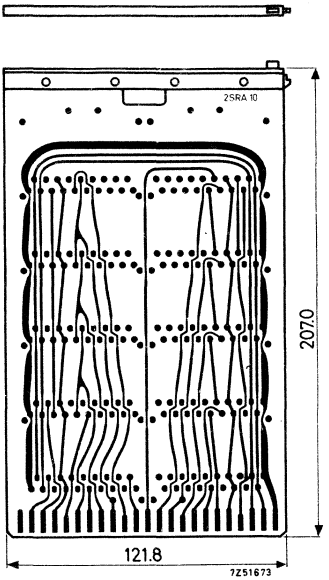


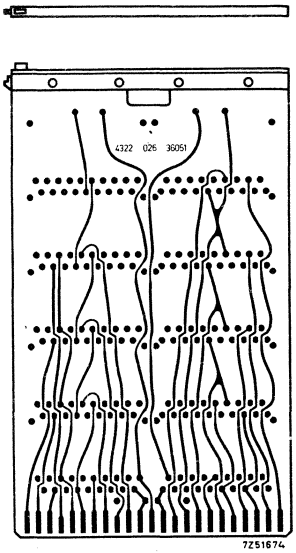




| | |
|---|---|
| Material | glass epoxy with plated-through holes |
| Contacts | 2 x 23, gold plated, pitch 0.2 inch |

# PRINTED-WIRING BOARD OF 2.SRA 10

This printed-wiring board (with extractor) of the assembly 2.SRA 10 fits the mounting chassis 4322 026 38240.

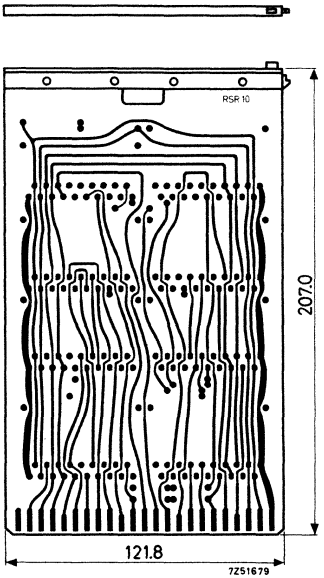


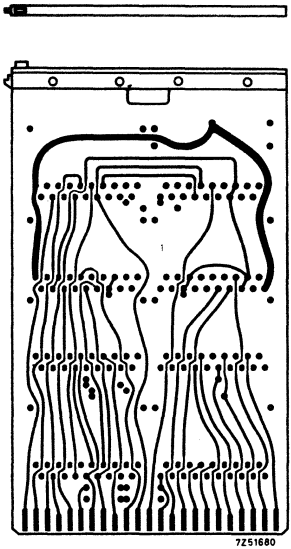




| | |
|---|---|
| Material | glass epoxy with plated-through holes |
| Contacts | 2 x 23, gold plated, pitch 0.2 inch |

# PRINTED-WIRING BOARD OF RSR 10

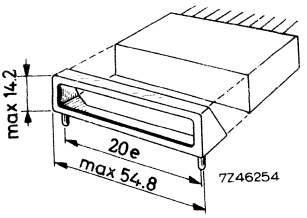
This printed-wiring board (with extractor) of the assembly RSR 10 fits the mounting chassis 4322 026 38240.




| | |
|---|---|
| Material | glass epoxy with plated-through holes |
| Contacts | 2 x 23, gold plated, pitch 0.2 inch |

# LOCKING CAP




For better securing 10-Series and 20-Series circuit blocks mounted parallel to a printed-wiring board (horizontal mounting), window-shaped locking caps are available. They fit the top of a circuit block.
The locking caps are provided with two holes and recesses to lodge two soldering tags, with which the caps can be secured to the board.

| description | catalog number |
|---|---|
| locking cap | 4322 026 32150 |
| soldering tag | 4322 026 32140 |

# STICKERS

These are drawing symbols of circuit blocks printed on self-adhesive, transparent material. They can be used for fast preparation of system drawings. The drawing symbols are as shown on the data sheets of the relevant circuit blocks.
The stickers are available in rolls, each containing 1000 drawing symbols of the same type of circuit block. Each sticker can be separately detached from the roll, without cutting.

| for circuit block of type | catalog number of a roll with 1000 stickers |
|---|---|
| FF 10 | 4322 026 07610 |
| FF 11 | 4322 026 07620 |
| FF 12 | 4322 026 07630 |
| 2.GI 10 | 4322 026 07640 |
| 2.GI 11 | 4322 026 07650 |
| 2.GI 12 | 4322 026 07660 |
| 2.TG 13 | 4322 026 30560 |
| 2.TG 14 | 4322 026 30570 |
| 4.TG 15 | 4322 026 34630 |
| PS 10 | 4322 026 07700 |
| OS 10 | 4322 026 07710 |
| OS 11 | 4322 026 36900 |
| PD 10 | 4322 026 07720 |
| PD 11 | 4322 026 36910 |
| GA 11 | 4322 026 34640 |
| TU 10 | 4322 026 07741 |
| PA 10 | 4322 026 07751 |
| RD 10 | 4322 026 07771 |
| RD 11 | 4322 026 36990 |
| ID 10 | 4322 026 36850 |

# CONTENTS

Accessories for circuit blocks 10-Series

A Circuit blocks 100 kHz Series

B Circuit blocks 1-Series

C Circuit blocks for ferrite core memory drive

D Circuit blocks 10-Series

Printed in The Netherlands

9399 261 17701